DATASHEET

VIRTUOSO ANALOG VOLTAGESTORM OPTION

The Cadence® Virtuoso® Analog VoltageStorm® Option adds IR drop and power rail electromigration to the Virtuoso custom design platform. This option to the Virtuoso Analog Design Environment extends the VoltageStorm family of power integrity products to analog designs, where power rail electromigration and IR drop on power and ground rails are increasing concerns for analog designers.

THE VIRTUOSO CUSTOM DESIGN PLATFORM

When design objectives dictate manipulating precise analog quantities—voltages, currents, charges, and continuous ratios of parameter values such as resistance and capacitance—companies turn to custom design. Full-custom design maximizes performance while minimizing area and power. However, it requires significant handcrafting by a select set of engineers with very high skill levels. In addition, custom analog circuits are more sensitive to physical effects, which are exacerbated at new, nanometer process nodes.

The Virtuoso custom design platform accelerates the design of custom ICs across various process nodes. By selectively automating aspects of custom analog design and providing advanced technologies integrated on a common database, it allows engineers to focus on precision crafting their designs—without sacrificing creativity to repetitive manual tasks.

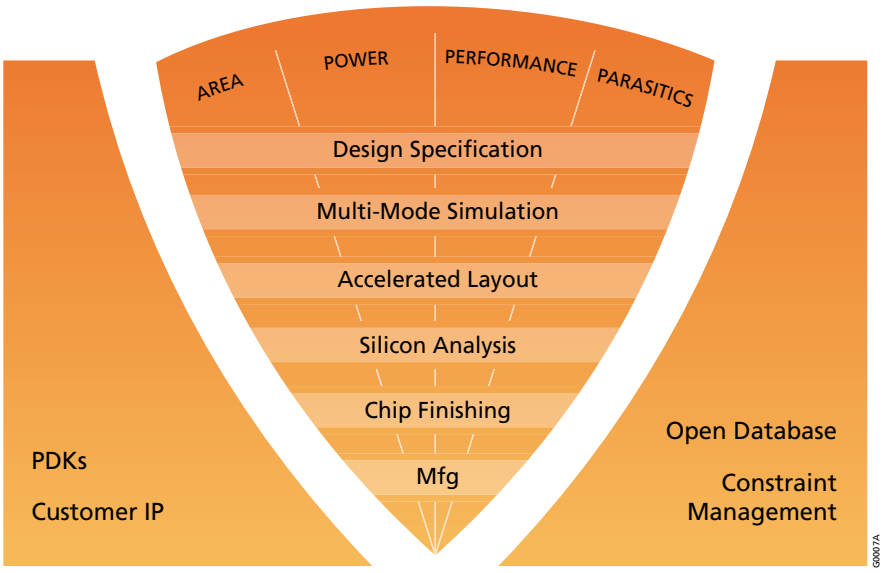

Figure 1: All components of the Virtuoso platform work together to support fast, silicon-accurate differentiated custom silicon

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VIRTUOSO ANALOG VOLTAGESTORM OPTION

Integrated tightly with the Virtuoso Analog Design Environment design creation product, the option performs IR drop and power rail electromigration verification for analog designs. The option combines with Assura® LVS, Assura RCX, and Virtuoso Spectre® Circuit Simulator to perform a full-chip circuit simulation specifically targeted for power integrity verification. Power rail electromigration is comprehensively checked for all interconnect segments and vias within the power networks. Thermal plots of IR drop and electromigration are directly displayed in the Virtuoso Analog Design Environment GUI, where you can easily address any identified issues or problems. The thermal plots are supported by a full textual report which contains details of the analysis results.

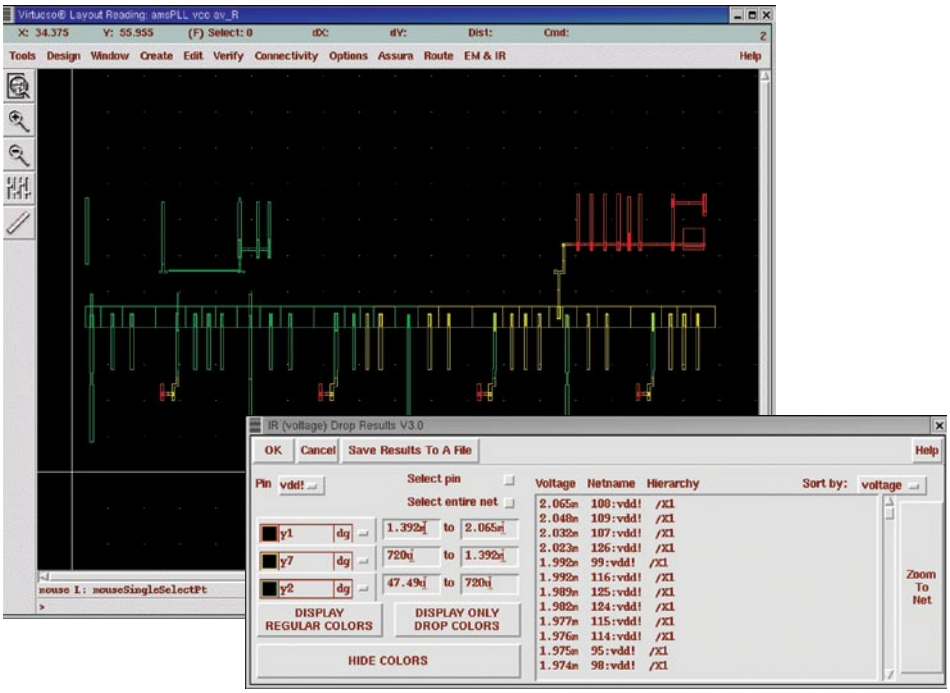

Figure 2: Virtuoso graphical display output showing filtered IR drop results for a VDD net

BENEFITS

- Reduces risk of tapeout failure due to IR drop and electromigration *(see Figure 2)*
- Improves understanding of power rail performance, under silicon-accurate conditions
- Maximizes user efficiency by displaying IR drop and electromigration results directly on the circuit layout
- Extends the value of existing extraction and simulation products
- Includes an easy-to-use menu-based interface to Virtuoso Analog Design Environment

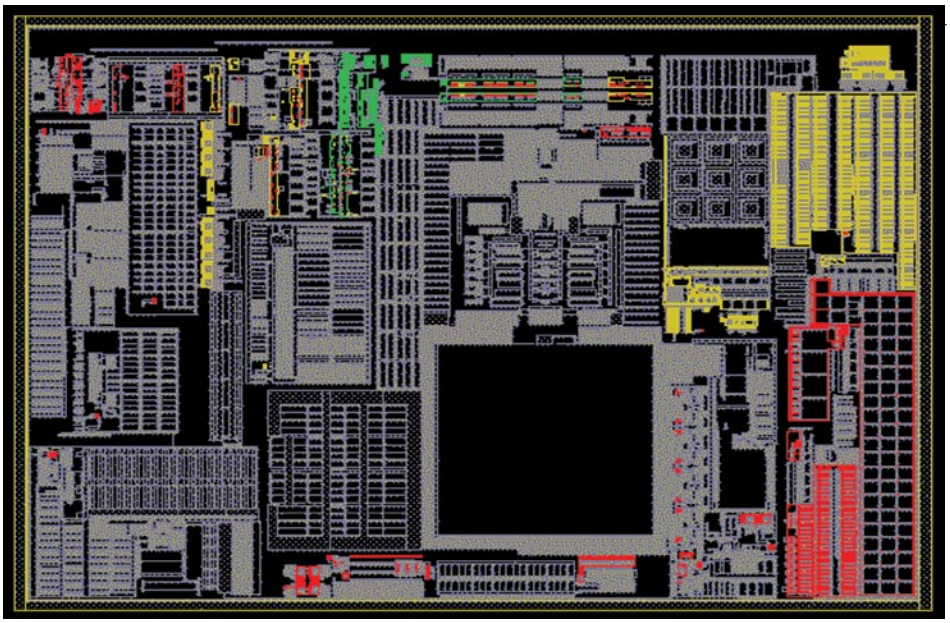

Figure 3: IR drop report form showing detailed results of an IR drop analysis

FEATURES

TIGHT INTEGRATION WITHIN VIRTUOSO ANALOG DESIGN ENVIRONMENT

Virtuoso Analog Design Environment is the market-leading solution for analog design creation. The option extends the value of Virtuoso Analog Design Environment by adding a direct and easy path to power integrity verification, necessary for most of today's complex designs. Using an additional pull-down menu option within the Virtuoso Analog Design Environment menu bar, your power nets can be rapidly analyzed for both IR (voltage) drop and electromigration. Results of the analysis are displayed directly on the layout within the Virtuoso Analog Design Environment GUI, which enables easy debugging of any power rail issues *(See Figure 3)*. An easy-to-use pop-up form displays the textual analysis results which can also be used to drive the debugging activity.

ACCURATE ELECTROMIGRATION ANALYSIS

Copper process technologies complicate electromigration analysis because the current density limits vary with the width of the metal interconnect. The Virtuoso Analog VoltageStorm Option enables you to enter multiple current density limits per interconnect layer, to allow you to

accurately set the electromigration limits. The temperature for the analysis is also user-definable, and a temperature scaling factor enables you to execute electromigration analysis at one temperature and scale the results for temperature corners using foundry-supplied factors.

STANDARD PRODUCTS UTILIZATION

The VoltageStorm option uses the most common parasitic extraction and circuit simulation tools within the Virtuoso Analog Design Environment—Assura LVS, Assura RCX, and Virtuoso Spectre simulation. This enables you to rapidly ramp up power integrity verification by using your existing control decks for these products, without having to learn new extraction or simulation engines.

DYNAMIC SIMULATION APPROACH

Since the power integrity solution executes a complete circuit simulation including the impact of IR drop on both power and ground rails, it increases confidence that your design will function correctly on silicon. For the highest confidence, power rail performance should be validated at multiple PVT corners.

SPECIFICATIONS

EASY SETUP

- Form-based setup for power integrity verification
- Supports via and wire electromigration limits
- Electromigration limits set per layer and per width
- Form-based reporting of IR drop results
- Form-based reporting of power electromigration results
- Goto next error capability for easy debug

POWER INTEGRITY RESULTS

- Thermal plots of IR drop results display directly on extracted cellview
- User controllable filters
- Form-based reporting of IR drop results
- Form-based reporting of power electromigration results
  - Clear identification of failures
  - Clear identification of required sizes to fix violations
  - Ordered listing (worst violators listed first)
- Reports RMS, maximum, or average results
- Goto next error capability for easy debug
- Temperature scaling factor adjusts results based on new temperature

PLATFORM/OS (all 32-bit)

- Sun/Solaris
- HP-UX
- Linux

CAPACITY

- 50,000 transistors
- 500K parasitic resistors

ASSOCIATED PRODUCTS

ASSURA DRC/LVS

- Tight integration with Virtuoso Layout Editor and Virtuoso Schematic Editor
- Full-featured batch and interactive verification tool
- Fast verification runtimes for highly repetitive and hierarchical designs
- Correctly verifies design connectivity regardless of layout methodology or hierarchy
- Automatically extracts devices formed across layout hierarchy
- Significantly reduces runtimes using multi-processing for device extraction
- Complete flexibility through user-defined device parameters and user-programmable rule files
- Supports all designs—analog, digital, RF, SiGe, and SOI designs

ASSURA RCX

- Accurate interconnect parasitic extraction
- Reduces cost-of-ownership with easy adoption into existing production flows
- Seamless integration with Virtuoso Analog Design Environment
- Supports industry-leading Si (0.13µm and below) and SiGe process technologies
- Advanced 3-D modeling capabilities
- Supports local interconnect, air gaps, conformal and multiple dielectric, copper effects

VIRTUOSO SPECTRE CIRCUIT SIMULATION

- Full integration with Virtuoso AMS Designer, Cadence Design Framework II, Incisive® Unified Simulator, and Virtuoso Analog Design Environment
- Advanced architecture supports large circuits containing more than 50,000 transistors
- Fully-integrated analog hardware description languages (AHDL) extend modeling capabilities, boosts simulation performance, and supports top-down design styles for rapid development of complex circuits and testbenches
- Comprehensive semiconductor model support combined with industry-leading foundry models
- Versatile analysis capability leads to increased designer confidence
- Superior simulation accuracy and performance for tough analog and mixed-signal circuits

CADENCE SERVICES AND SUPPORT

- Customer-focused solutions that increase ROI, reduce risk, and achieve your design goals faster
  - Collaborative approach and design infrastructure—virtual teaming
  - Proven methodology and flow tuned to your design environment
  - Design and EDA implementation expertise
- Product and flow training to fit your needs and preferred learning style
  - Over 80 instructor-led courses—certified instructors, real world experience
  - More than 25 Internet Learning Series (iLS) online courses
- Cadence customer support that keeps your design team productive
  - Cadence applications engineers provide technical assistance
  - SourceLink® online support gives you access to software updates, technical documentation, and more—24 hours a day, seven days a week

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