Virtuoso Custom Design Platform XL

The Cadence® Virtuoso® custom design platform XL family of products extends the L family to provide higher levels of design assistance to the end user. The platform includes Virtuoso Schematic Editor XL, Virtuoso Analog Design Environment XL, and Virtuoso Layout Suite XL.

Virtuoso Custom Design Platform XL

The Virtuoso custom design platform comprises several advanced products.

Virtuoso Schematic Editor XL

Virtuoso Schematic Editor XL delivers extended functionality through the addition of assistants that speed common tasks by as much as 5x over Virtuoso platform L methodologies.

To maintain design consistency throughout the custom design flow, the user can use design constraints. These constraints, which cover needs such as matching and symmetry, are added to the schematic by the designer to guide the implementation tools to maintain the designer's intent on critical pieces of the design.

Virtuoso Analog Design Environment XL

Virtuoso Analog Design Environment XL is the most advanced design and simulation environment for the Virtuoso platform. By supporting extensive exploration of multiple designs against their objective specifications, it sets the standard in fast and accurate design verification.

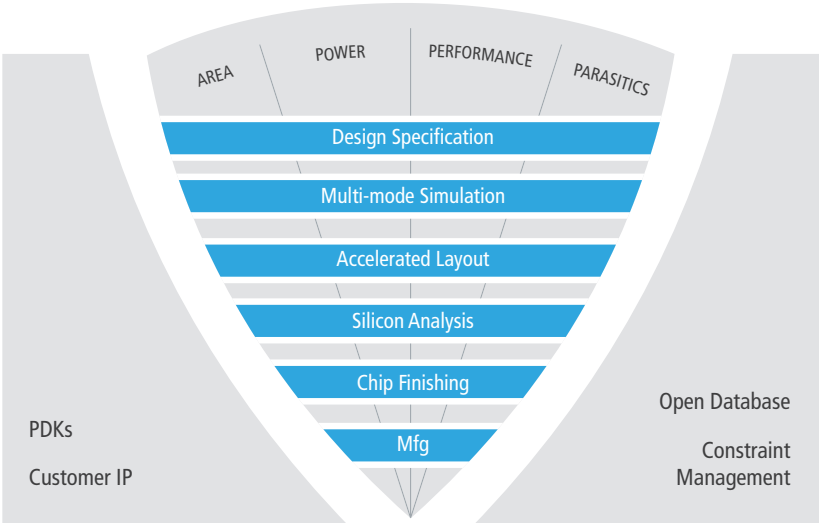

Figure 1: All components of the Virtuoso platform work together to support fast, silicon-accurate differentiated custom silicon

Virtuoso Layout Suite XL

Virtuoso Layout Suite XL is the high-end custom block authoring physical layout product of the Virtuoso platform. It supports both constraint- and schematic-driven physical implementation of custom-digital, mixed-signal, and analog designs at the device, cell, and block levels (see Figure 2).

As the design composition environment for the Virtuoso platform, Virtuoso Schematic Editor XL delivers an extensive set of tools for custom IC design entry. From architectural definition using industry-standard language representations (such as Verilog®, VHDL, and C) to final structural implementations at the transistor level, it helps engineers implement each stage in a design. The concept of "design constraints" is introduced at the XL level. These constraints allow design "intent" to be stored electronically and adhered to throughout all the different tool interactions that occur in later parts of the design cycle.

Virtuoso Analog Design Environment XL manages the exploration and verification of multiple designs in one easy-to-use tool. Throughout the design and verification process, any circuit can be monitored against its objective specifications with fast pass/fail feedback. In addition, all sweeps, corners, Monte Carlo statistics, and measurements are managed and stored in one location for fast and accurate verification of a design.

As a high-end custom block authoring physical layout tool, Virtuoso Layout Suite XL provides accelerated features beyond the basic polygon layout editing features of Virtuoso Layout Suite L. It supports custom-digital, mixed-signal, and analog designs at the device, cell, and block levels. These accelerated features provide advanced connectivity, constraint- and design-rule–driven functionality combined with advanced automation to accelerate custom block authoring. Included are device generation and editing with parameterized cell (Pcell) and SKILL programming support (see Figure 3).

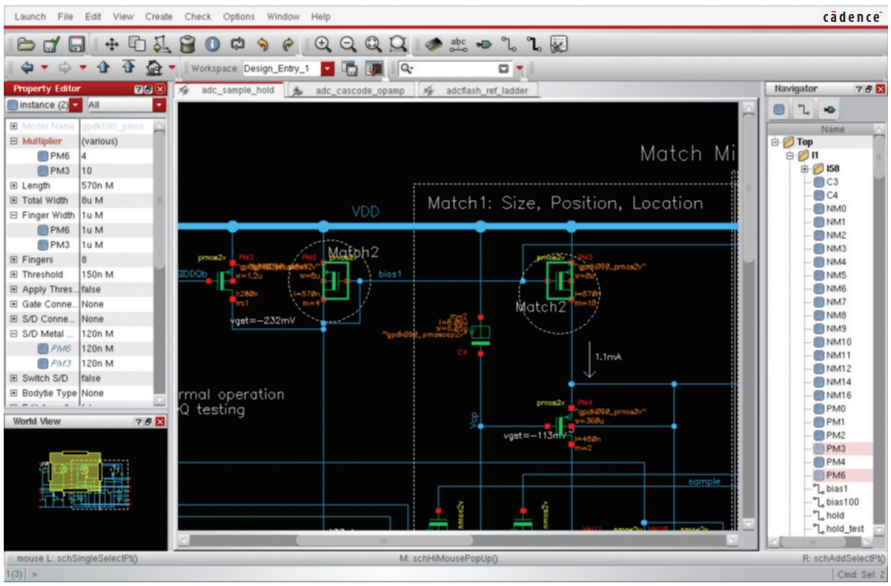

Figure 2: Virtuoso Schematic Editor XL

Benefits

- Maintains design integrity by using design constraints throughout the XL tool flow
- Provides easy visualization of large, complex designs using the Hierarchy Editor
- Enables early discovery of design problems with built-in design and language rule checking
- Rapidly executes commands with user-configurable bind keys and menus
- Reduces risk by maintaining agreement between design and specification as well as through managing validation of design, process, and spec changes
- Eases design reuse through capturing the design process as IP
- Improves verification throughput with simulation distribution and multi-test management
- Ensures quality through the standardization of design methodologies
- Provides constant visibility into the design status of multiple projects across multiple sites
- Simplifies design reviews through integral documentation, specifications, measurement results, and waveforms
- Accelerates block authoring via connectivity-driven features and flows—schematic or netlist—which promotes correct-by-construction LVS-correct layout to reduce verification iterations
- Increases productivity and design quality with constraint- and design-rule–driven features to automatically ensure design and process correctness in real time
- Simplifies and optimizes device generation using a new menu-driven QuickCell feature or standard SKILL-programmable Pcells
- Express Pcells capability reduces data load time and manipulation response time of large designs

Features

Fast and accurate design entry

Virtuoso Schematic Editor XL provides many features that facilitate fast and easy design entry. In addition to all the features offered in the L configuration, XL adds assistants for search, property editing, viewing, and traversing the design hierarchy. These assistants provide up to a 5x increase in productivity when performing these common tasks. The XL configuration also offers new capabilities such as tabs, configurable workspaces, and new menu structures to mirror

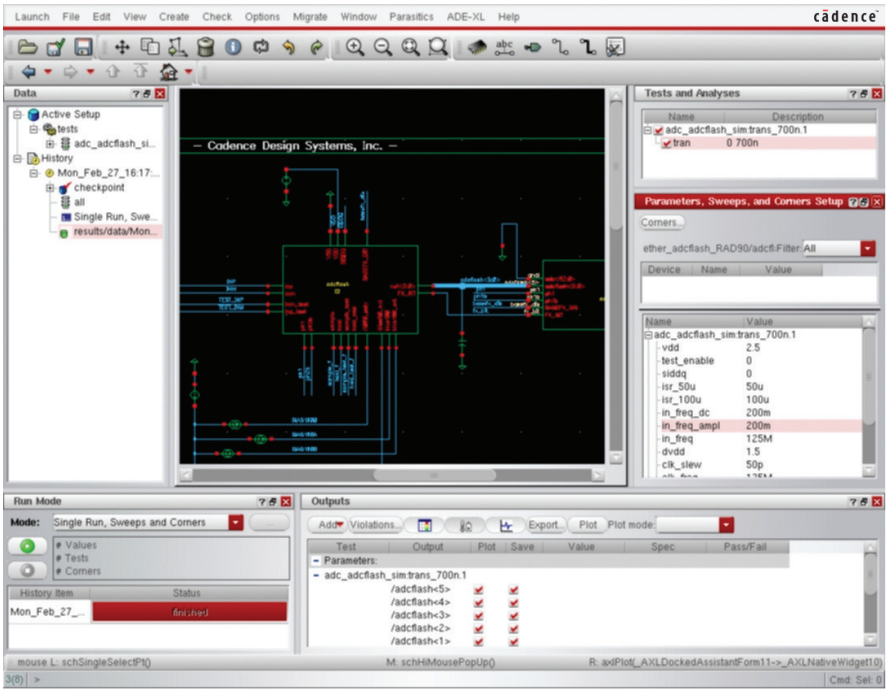

Figure 3: Virtuoso Analog Design Environment XL

common features in Web browsers. More advanced users can quickly execute commands using user-programmable bind keys and object-sensitive pop-up menus, which display relevant operations for objects under the cursor, anticipate user requirements, and present only pertinent choices.

Specification-driven design

To accelerate design verification, Virtuoso Analog Design Environment XL combines specification entry and design management into a single unified cockpit. A specification consists of multiple tests, which are formed by combining test harnesses with specific measurements. Virtuoso Schematic Editor XL eases the development of multiple tests over multiple conditions to validate a design's performance against the target specification. Once created, the tests and the complete specifications can be shared and managed across multiple design groups to set standards of testing for specific types of designs. The project level provides access to all the tests, sweeps, corners, scripts, and documentation needed to completely validate a design against the target specification.

An overview of all the tests within a project is available through the test assistant, which presents the status of all tests along with easy access to all the waveforms, measurements, and simulation files. From the assistant, all tests can be run individually or together for a complete design investigation and verification. The designer can use the parallel-processing options for efficient simulation management. In addition to standard SPICE and RF simulation analyses, Virtuoso Analog Design Environment XL supports sweeps, corners, and Monte Carlo analysis over one or more of the available tests. All results are automatically stored for validation against the objective specifications. Virtuoso Multi-Mode Simulation is fully integrated into the standard cockpit, as well as the majority of third-party simulation technologies.

Connectivity-driven functions and flow accelerate design completion

Virtuoso Layout Suite XL has set the standard in the industry and changed the way custom block authoring is done. Driven by a schematic connectivity source using Virtuoso Schematic Editor XL or a netlist source such as CDL or SPICE, designers can achieve an LVS-correct layout in real time. This approach promotes correct-by-construction layout, improves productivity, and reduces verification time. Additionally, it enables automation of tedious design tasks such as device generation, placement, and routing. Schematic and layout can be cross-probed to highlight instances and devices as well as to quickly identify unconnected nets (see Figure 4).

Constraint- and design-rule–driven functions for improved productivity

Virtuoso Layout Suite XL provides design constraint specification and management and design-rule–driven features that are automatically flagged when in violation or enforced in real time. This capability coupled with connectivity promotes correct-by-construction layout, improving productivity and reducing physical verification iterations and time. Device generation, placement, and routing function (both automatic and done manually with the wire editor) obey the constraints and all technology file process rules. All process nodes are supported, from classic analog at .25u all the way down to leading-edge 45nm processes.

Tight integration with the Virtuoso platform

All of these features are an integral part of the Virtuoso custom design platform, connecting to all the other features of the platform. This integration provides a single environment to create, analyze, and implement multi-domain designs, including ASICs, programmable ICs, multi-chip modules, and digital, analog and mixed-signal ICs. The Virtuoso platform supports the industry-standard OpenAccess (OA) database, as well as the Cadence SKILL programming language, which facilitates customization of the environment and the encapsulation of proprietary design tools.

Specifications

Design composition

- Complete design hierarchy support
- Simplified automatic generation of an HDL template
- Support of multi-sheet schematics

- User-configurable command bindkeys and label display
- Dynamic highlighting for easy design correction
- Automated interactive connection router
- User-configurable selection with filtering
- Comprehensive symbol creation and editing features
- User-configurable undo/redo levels
- Move, copy, stretch, rotate, and delete editing options
- Search and replace features
- Customizable tool environment using Cadence SKILL
- Online help using HTML formatted publications

Design Simulation and Analysis

- Design exploration with sweeps, corners, and Monte Carlo statistics
- Creation of specifications directly from simulation results
- Specifications sheets to compare design to design, design to model, or process to process
- Projects can be shared among multiple users and sites
- Distributed processing
- Parallel analysis of multiple tests
- Creation and tracking of dependencies among tests
- Calculator, Ocean, MDL, and MATLAB measurement strategies
- Tests overview window with specification checking
- Integrated with Virtuoso Multi-Mode Simulation
- Cross-probing and annotation to schematics
- Integrated Wavescan waveform display and waveform calculator for sophisticated analysis
- Integral documentation creation

Physical implementation

- Automated device editing, including abutment, pin permutation, folding, chaining, and cloning
- Menu-driven or programmable multi-part path (MPP) feature for guard rings, slotting, etc.
- Design-rule–driven editing with real-time notification or enforcement of process rules
- Dynamic measurement
- Constraint-driven specification, management, and real-time notification or enforcement
- Automatic constraint- and design-rule–driven placement of pins, devices, cells, and blocks
- Advanced shape-based constraint- and design-rule–driven interactive routing
- ECO support
- Legacy non-connectivity design importing and connectivity mapping
- Assura® physical verification support

Design inputs

- OpenAccess data objects
- Cadence proprietary languages: Ocean and MDL
- SPICE netlists
- EDIF 2 0 0 netlist
- Circuit design language (CDL)
- SPICE
- VHDL IEEE 1076-1993
- Verilog IEEE1364
- SKILL
- STREAM format
- CDL and SPICE netlist format
- Verilog and VHDL AMS languages

Design outputs (Virtuoso Schematic Editor XL)

- EDIF 2 0 0 netlist
- CDL
- SPICE
- OpenAccess
- SKILL
- STREAM format

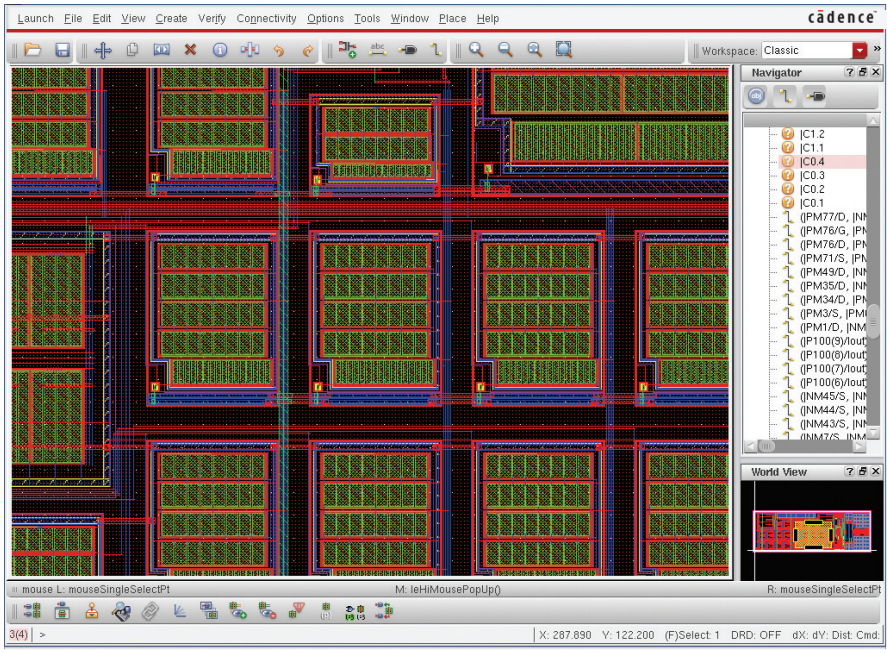

Figure 4: Virtuoso Layout Suite XL

Design outputs (Virtuoso Analog Design Environment XL)

- PSF waveform format
- SST2 waveform format
- Perl scripts
- PLATFORM/OS
- Sun/Solaris
- HP-UX
- Linux
- IBM AIX

Third-party support

- Access to other third-party simulators from Synopsys, Mentor Graphics, Silvaco, Magma, Berkeley Design Associates, and in-house proprietary simulators are supported through the Virtuoso Analog Design Environment interface
- Supports MATLAB from Mathworks for additional measurements and visualization

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

Virtuoso Custom Design Platform XL Features

	Virtuoso Schematic Editor XL	Virtuoso Analog Design Environment XL	Virtuoso Layout Suite XL
New Common Cockpit	X	X	X
New Icon Style	X	X	X
Multi-tab Support	X	X	X
Bookmarks & History	X	X	X
Updated Pulldown Menus	X	X	X
Window Config Support	X	X	X
World View Assistant	X		X
Search Assistant	X		X
Property Editor Assistant	X		X
Navigator Assistant	X		X
Constraint Browser	X		X
Design Explorer	X		X
Simple Test-bench		X	
Simple Parametric Analysis		X	
Device Checking		X	
Global Variable Support		X	
Updated Wavescan		X	
New Calculator		X	
Simulation Support: Virtuoso Multi-mode Simulation, HSPICE		X	
Basic Polygon Editing			X
Q-Cells			X
DRD Editing			X
Constraint Browser			X
Search Assistant			X
Property Editor Assistant			X

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