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Automatic Placement for Custom Layout in Virtuoso Layout Suite GXL

The Cadence® Virtuoso® custom design platform is best known as the de facto standard for custom chip creation, owing primarily to its interactive and assisted design techniques. A lesser-known fact is that the platform also offers significant automatic design techniques. Virtuoso Layout Suite GXL delivers many capabilities for automatic placement of custom designs. Cadence defines a common terminology for placement in the platform and design space, and provides detailed recommendations for automatic placement capabilities.

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Introduction

The Cadence Virtuoso custom design platform is well known throughout the industry as the long-standing de facto standard for custom design. The vast majority of users create layout with the platform at the purely manual shape-based editing level (Virtuoso Layout Suite L), or the assisted connectivity-based editing level (Virtuoso Layout Suite XL). However, Virtuoso Layout Suite XL and GXL products also offer many assisted and automatic capabilities. In this paper we consider the placement[1] capabilities of these products. First, we define the addressed design space and a common set of terminology for placement in the custom design platform. Then we will describe in detail the capabilities of three of the automatic placement tools: the Analog Placer, the Custom Digital Placer, and the Floorplanning Block Placer.

Common Terminology

We begin by defining the design space served by the Virtuoso platform. A wide variety of designs in a wide variety of technologies are created using the platform. One usable definition of the design space is all designs done on chips, rather than on PCBs or with discrete components, which are not created using big digital synthesis/placement/routing tools such as the Cadence Encounter®[2] platform. This can encompass design areas as varied as MEMS[3] on GaAs substrate to an RF design on SiGe to common analog designs in a typical CMOS process. For the purpose of defining the primary design space focus of custom design we will concentrate on three basic areas: Analog Design, Custom Digital Design, and Chip-level assembly of mixed-signal designs. For the purpose of this paper, we will refer to these areas as the custom design space. Although there are many other types of designs implemented by users with the Virtuoso platform, these areas comprise the majority of our users.

Now we turn to the definition of placement in the custom design space. At the most basic level (Virtuoso Layout Suite L), placement means the user creating individual polygons on particular layers which are arranged to create transistors, resistors, capacitors, routing and pins. There certainly are designs

and designers for whom this is the lowest cost path to the highest performance layout. But given the continuous need for higher productivity, and more designs in the custom space, for most users it makes sense to move to a slightly higher level of abstraction, which is referred to as a connectivity-driven design flow. Virtuoso Layout Suite XL—which is typically used in the Analog Design flow—provides the capabilities for this connectivity-driven design flow. In this flow, devices such as transistors, resistors, capacitors, etc. are represented by Parameterized Cells (Pcells) specified in the technology library. Pins are defined programmatically in the tool, and routing connectivity is automatically determined from a connectivity source such as a netlist or schematic. This then simplifies the placement problem to finding a coordinate/transform (X, Y, orientation) for each Pcell and Pin, and optionally creating other associated geometry to allow proper functioning of those instances, such as guard rings or well geometry. The routing step then completes the layout by creating vias and path segments such that all necessary connectivity is completed. This flow contrasts with the Cadence Encounter design space primarily in the level of layout building-block abstraction applied to the problem. In those "big digital" designs, placement typically refers to assigning final transformation to standard cells or macro/IP abstracts on the chip's surface. Utilizing this level of abstraction also allows many of the details of chip-level implementation (wells, guard rings, flexible cell size and pin locations) to be avoided in big digital design, leading to correspondingly higher capacity. All of these detailed implementation complexities are decided during the standard cell design phase, which is typically done in the Virtuoso platform, falling into the custom design category. In addition the Virtuoso platform can cater to mixed-signal design space at chip and block level with medium-sized designs for the chip-level assembly flow. The basic flow of design can also be repeated at a number of levels of hierarchy to incrementally build the whole chip from the top down. Various flows like Analog on Top (AOT) have been developed specifically to generate and place hierarchical layouts in the custom design space as compared to a big flat abstract design methodology of the Cadence Encounter platform.

From the discussion above, we see the common characteristics of placement in the custom design space as: device-level rather than gate/cell level, and detail-geometric-oriented rather than abstracted. Due to the wide variety of user preference on the fully manual to automated continuum we find a variety of different types of placement tasks. Within the Virtuoso platform, we refer to three basic types of placement tasks: Initial, Assisted Sub-block, and Automatic.

Initial placement

In a connectivity-driven design flow, the connectivity, pins and many of the parameters controlling the creation of the instances have been specified on the netlist or schematic, typically for simulation purposes as well as driving layout. Utilizing this information, Virtuoso Layout Suite XL provides the user with initial placement capabilities as an alternative to complete manual creation of instances and pins. The most commonly used is known as Generate from Source (GFS)[4] as it creates all of the instances and pins from the connectivity source. They are placed in a somewhat arbitrary manner, but are then available on the layout canvas to be interactively placed by the user. Users can make use of the re-initialize engine[5] to do an initial segregated placement based on cell type of instances. It places IOs on top, Macros on the left, Standard cells on the right and Custom layouts at the bottom of the design boundary; this gives the user a better idea of the types of blocks and their number, which helps in choosing available placement options. Many users also want the option to have that initial placement roughly follow the placement of the symbols in the schematic. This feature is typically known as Place as Schematic (PAS)[6], and is available as an option to GFS or as a separate command. In addition, if the user is not interested in having all instances created in a batch manner, the Pick from Schematic (PFS)[7] command allows the user to interactively select instances from the schematic and create them at targeted locations in the layout. GFS, PAS and PFS provide utilities for users to assist their interactive layout process; they provide little automation for the full placement process.

Assisted sub-block placement

Once the initial instances are created, many designers utilize common layout patterns for sub-blocks. Features in Virtuoso Layout Suite XL and GXL have been developed to assist in the layout of these common sub-block patterns. These tools and techniques are distinguished by their ability to assist with final layout of a sub-section/sub-block of the full design. So for a particular part of the layout, they may help in getting that part of the design to 100% complete with lower effort, but it is only part of the layout. Tool capabilities in this category include Chaining[8], Synchronous Clones[9], and Modgens[10]. Chaining gives an automatic way to take a set of transistors and abut them together into a single row quickly and easily. Synchronous Clones lets the designer specify that a layout pattern will be replicated and just design it once and have the rest of the layout automatically mimic the design. With Modgens the designer can specify an arrayed-instance-based layout very quickly for typical interdigitated analog circuit sub-blocks like differential pairs, current mirrors, etc. In addition, there are various tool accelerators available

to improve layout productivity for the whole layout design, such as Constraint-Aware Editing (CAE), Design-Rule Driven (DRD) editing, and interactive device abutment. All of these tools allow the layout designer to continue the practice of custom and interactive design of the layout, while at the same time accelerating their activities and enforcing design rules, constraints, and correct abutment more automatically.

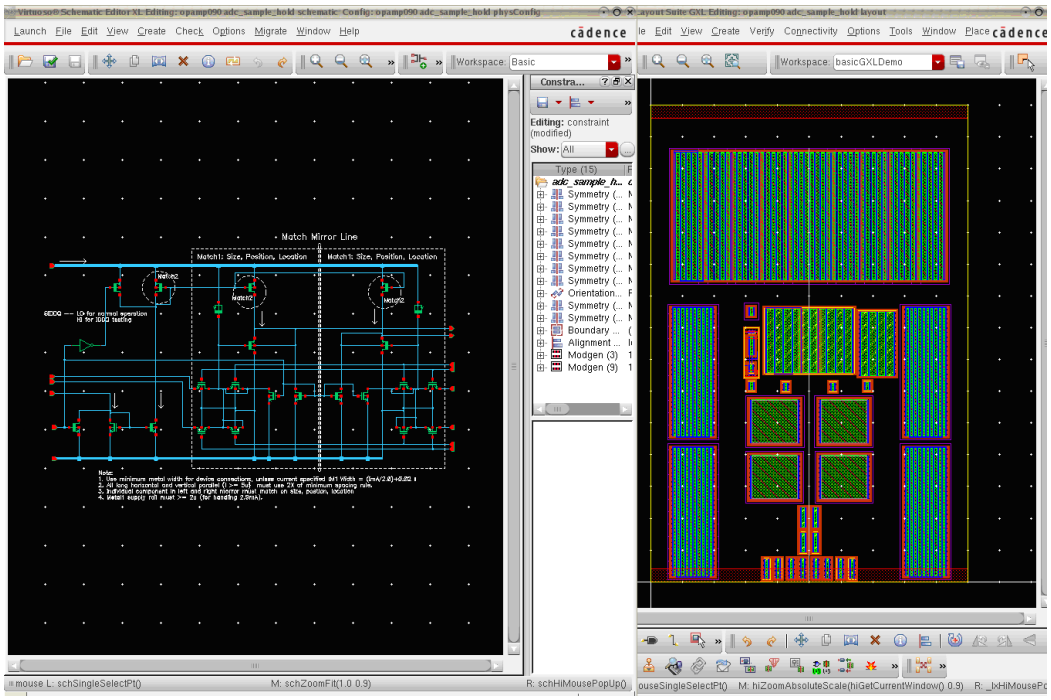

Figure 1. Basic Analog Placement design

Automatic placement

Finally we reach the full automatic placement tools. These perform fully automatic placement on all of the instances and pins in our current design. The results produced may not be the 100% complete layout, but it takes the designer to the 80% solution with much greater productivity than the manual/assisted design flow. In the following section we will look in detail at the capabilities for each of these automatic placement features for Virtuoso Layout Suite GXL: Analog Placement, Custom Digital Placement, and Floorplanning Block Placement.

Automatic Placement Capabilities

Here we provide a detailed view of the specific design space the automatic placement capability supports, and the flows that best utilize these tools.

Analog placement[12]

The Analog Placer is designed primarily to address analog circuits with sizes of 10 – 200 placeable instances. These placeable instances may map one-to-one with the actual transistors in the design, or groups of instances may be built into sub-blocks using the techniques discussed in 2.2. It performs flat transistor-level placement, primarily driven by constraints such as Symmetry, Alignment, Clusters, and Matching and connectivity to minimize wire length. It has the capability to automatically create well and guard ring geometry around appropriate groups of instances. The primary goal of the Analog Placer is to obey all specified constraints, then optimize for area and wirelength.

Three analog design flows that use the Analog Placer most successfully are Basic Analog Placement, Analog Placement for Chip Planning and Rapid Analog Prototyping.

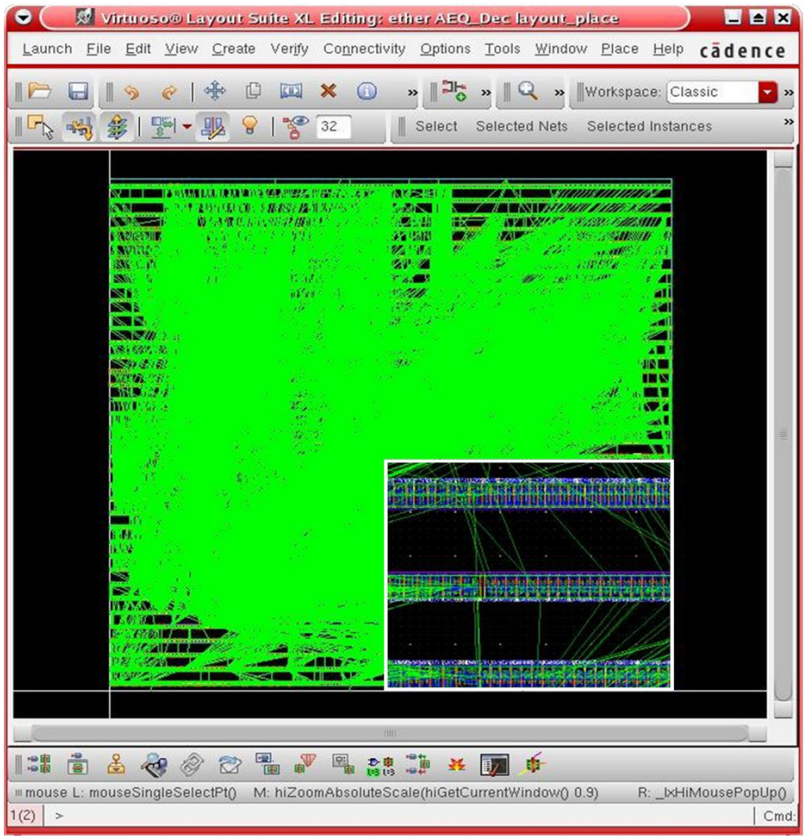

Figure 2. Standard Cell Placement

Basic Analog Placement uses the Analog Placer to create the 80% complete layout for typical analog circuits like Cascode OpAmps, Comparators and the like. In this type of flow the circuit designer or layout designer may spend slightly more time creating and tuning constraints on the design, to get the best placement. This has the benefit of capturing this knowledge of the critical constraints (characteristics) of the layout design to be re-used in the future. An example design that has utilized the Analog Placer for the layout can be seen in Figure 1. This design took 9.1 seconds for placement on a Linux machine with an Intel Core™ CPU running at 2.13 GHz.

Next, looking at the Analog Placement for Chip Planning flow, Cadence has users who are successfully employing the Analog Placer as an 'area-estimate' tool. In this flow, the designer uses the Circuit Prospector[11] to automatically create reasonable constraints and then runs the Analog Placer in a scripted fashion, and collects results on the

typical area, aspect ratio and pin locations and uses those for the top-down floorplanning flow. These placements can then either be used as a starting point, or only used to create the template (PRBoundary and Pin Positions) used by the layout engineer.

And lastly we have our Rapid Analog Prototyping flow. In this case our circuit designers want early feedback on device and wiring parasitics without doing detailed layout design. So they might use the Analog Placer as part of an automated flow to do automatic placement and routing, and extract parasitics and then re-simulate their design with these parasitics in place. Here the process of adding constraints, especially such as Modgen constraints, can greatly aid the process, as it will ensure that the important parasitics are consistent between the prototype layout and the final layout.

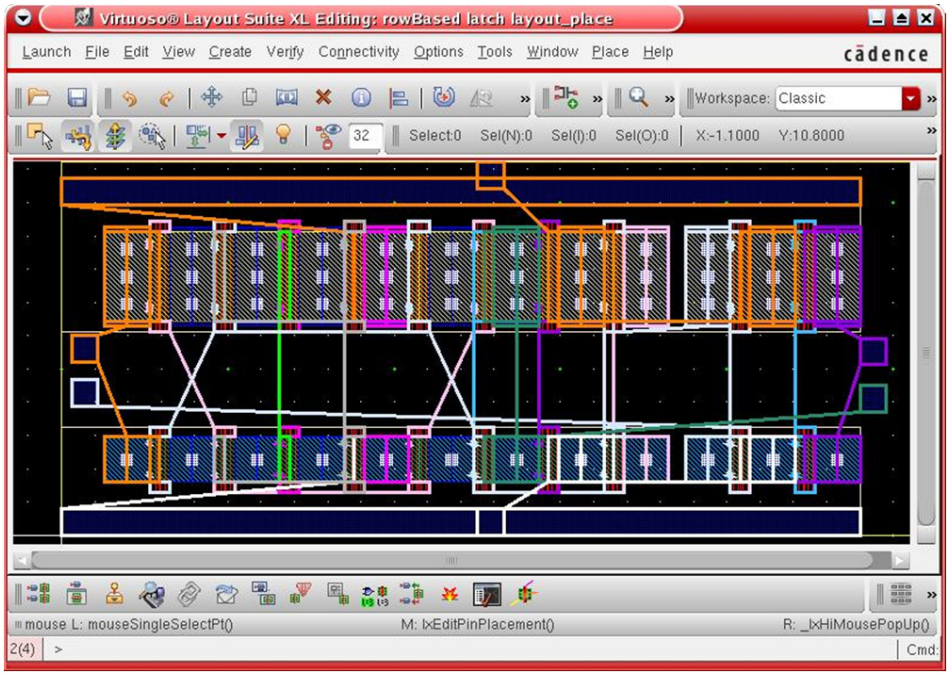

Figure 3. Transistor Level Placement

Custom digital placement[13]

The Custom Digital Placer is used to implement small digital designs with several thousand placeable components. These components are standard cells, transistor-level devices and pins. The placer has three placement options; global placement, optimized placement and ECO mode. The placement can be run on a selected set or the entire design. The Custom Digital Placer requires user-created rows and component types. For a design with 10,000 standard cells the placer takes approximately 18 minutes to complete global and optimized placement on Sun-Fire-V440. The Custom Digital Placer can also be driven by constraints that include Fixed, Alignment, Distance, and Cluster.

The placement of standard cells includes an option to perform row compaction and has an internal global routing estimate, which minimizes area and wirelength. Additionally it has the capability to create filler cells to complete power and ground paths by filling spaces and also create standard cell substrate contacts.

The Custom Digital Placer can also be used to place transistor-level devices for the creation of standard cells and macro cells. In this mode, the placer can perform abutment of components to maximize device sharing by forming chains of abutted components, which minimizes area and wirelength. For smaller standard cells the XL chaining command may produce better results.

Floorplanning block placement[14]

The Block Placer is designed to place macros of both hard and soft blocks to address placement problem in a design space, which caters to mixed-signal and pure analog chips. In the Analog on Top (AOT) flow, a design having a few thousands of components is partitioned into a few hard and soft blocks, which can then be developed independently in Virtuoso and Encounter platforms. To place these blocks, users start with an IO placement if the design is a mixed-signal die and then run the block placer to place the analog and digital blocks. The results are best when the number of blocks is within 16 to 20. This can be achieved with good top-level partitioning; creating too many partitions generally defeats the top down floorplanning methodology. The block placement is connectivity aware, with well connected blocks staying together; this reduces the net length and improves the efficiency of the final layout. Users give additional costs like no overlaps—within boundary, net criticality, etc.—to further fine-tune the results.

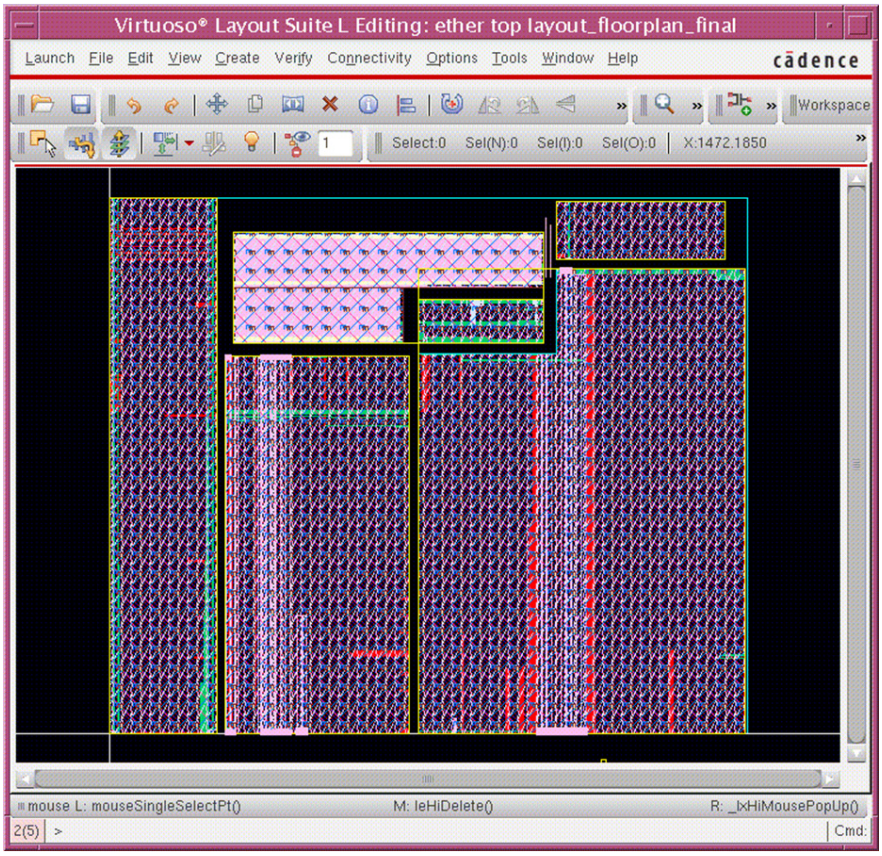

Figure 4. Floorplanning Block Placer

The block placement technology is well integrated with the Virtuoso Space-based Global Router15 and can use the congestion data generated by it to improve placement results incrementally.

The front end constraints provided by the schematic designer—like alignment, boundary area, distance between noisy digital and victim analog blocks and clustering—are respected faithfully by the block placer, which is well integrated with the Constraint Infrastructure[16] used for visualization, transfer and modification of constraints.

The custom design user utilizes the block placer because it understands the mixed-signal design space: e.g., the features of snapping origin and soft edges to manufacturing grid, automatic soft block re-size, and rectilinear blocks support to optimize space. It can place digital and analog macro layouts with equal ease to generate data that is hierarchical and perfectly interoperable with the Encounter platform. This complements the Encounter platform solution, which is used to place millions of same-sized, rectangular standard cell abstracts. So for a medium-sized mixed-signal design with irregular space availability, a low-cost path to place blocks is available, and is popular with many users for Analog on Top and Mixed-Signal on Top design flows.

Conclusion

A common terminology for types of placement technology in the custom design space has been presented and defined, among the areas of initial placement, assisted sub-block placement, and automatic placement. This common vocabulary for types of placement will aid in our discussion inside Cadence and with users. The current state of Virtuoso Layout Suite GXL Automatic Placement capabilities was also presented in Section 3. Clear understanding of these capabilities will assist in mapping the areas to promote adoption of automatic placement. It also gives us a common starting point for identifying areas of focus for future innovation and improvement. The descriptions of the automatic placement tools and flows presented in this paper helps our whole community better understand the capabilities and potential of the Virtuoso Layout Suite products.

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