cadence®

Teradyne and Cadence

"Virtuoso Multi-Mode Simulation has improved our ability to implement complex analog/mixed-signal designs, ultimately helping us introduce higher-quality end products to the market faster."

Dominic Wong, Engineering Tools Strategy Manager, Teradyne, Inc.

The Customer

Based in North Reading, Massachusetts, Teradyne has been a leader in providing automatic test equipment (ATE) to component manufacturers since 1960. Today, the company manufactures ATE systems for virtually every type of electronics, semiconductor, and communications application for companies worldwide.

The Challenge

Each of these systems is designed with advanced custom chip sets. Teradyne wanted to implement a single, flexible methodology for use in its design and verification of complex mixed-signal systems on chip (SoCs), and across a wide range of other integrated circuits (ICs). Key considerations for Teradyne were simulation capacity for very complex analog mixed-signal designs and the ability to dynamically adapt to changing design priorities.

The Solution

Cadence answered Teradyne's substantial system-level requirements with comprehensive Cadence® Virtuoso® Multi-Mode Simulation technology. Virtuoso simulation technology provides designers with a complete design and verification environment for analog, radio frequency (RF), mixed-signal, memory, and SoC designs. It combines the industry's leading SPICE, FastSPICE, RF, and analog/mixed-signal simulators in a unique shared-licensing package.

Business Challenge

- Improve productivity and quality of silicon

Design Challenges

- Complex analog and mixed-signal SoC simulations
- Wide variety of applications and test priorities

Cadence Solutions

- Virtuoso Multi-Mode Simulation
  - Virtuoso UltraSim Full-Chip Simulator
  - Virtuoso Spectre Circuit Simulator
  - Virtuoso AMS Designer

Results

- Token-based licensing model for flexible simulation solutions over a wide range of design verification requirements
- Increased speed to market from a single testbench configuration directly integrated to the design process

Teradyne has already used this platform to successfully develop an extremely complex mixed-signal SoC. The functional verification of this design required numerous individual simulations, building into a single complex full-chip simulation. Teradyne used Virtuoso Spectre® Circuit Simulator and Virtuoso UltraSim Full-Chip Simulator to design the analog blocks, allowing the team to implement a command-line mixed-signal verification flow with Virtuoso AMS Designer based on the same underlying analog solvers used during the analog block design. The transition from analog block design to mixed-signal verification was made easier by using the same underlying technology and model files as well as consistent results that were used during the block design and verification phase.

"Virtuoso Multi-Mode Simulation has helped us make our design flow more efficient by allowing us to use the simulator that we need, when we need it, ultimately leading to a shorter design cycle and better quality of silicon."

In order to manage the large number of complex, mixed-signal simulations required to verify this class of designs, Teradyne developed a logic verification design flow through top-level Verilog test benches. This change in perspective and methodology has provided a significant positive impact on development schedules and final silicon quality.

"We have an extremely complex mixed-signal SoC requiring a lot of mixed-signal simulations for functional verification of the design," says Dominic Wong, Engineering Tools Strategy Manager at Teradyne. "Virtuoso Multi-Mode Simulation has helped us make our design flow more efficient by allowing us to use the simulator that we need, when we need it, ultimately leading to a shorter design cycle and better quality of silicon."

Cadence flexible token-based licensing allows Teradyne to use whatever subset of simulation technology it wants at any given time, and change the mix whenever its needs change—without having to purchase the entire set of fixed licenses. This gives Teradyne a flexible advantage by allowing a shift in design simulation priorities dynamically. Leveraging the token-based model together with the capability that Virtuoso Multi-Mode Simulation provides to switch seamlessly between simulation engines allows the company to achieve shorter time to market with higher-quality silicon and an optimized investment.

Summary

"Virtuoso Multi-Mode Simulation's combination of superior simulation technology and the flexible token-based licensing model increased the efficiency of our design flow, and maximized our return on investment," Wong says. "This enables us to build complex mixed-signal SoCs not only faster, but with higher quality as well."

The greatest impact that the adoption of the Virtuoso Multi-Mode Simulation package has had on Teradyne's design effort is not a single successful chip, but a fundamental change in the design and verification workflow, simulation capacity and overall methodology. Virtuoso Multi-Mode Simulation provides the complete solution for design and verification of analog mixed-signal SoCs in a consistent technology platform. By providing the complete solution, Cadence reduces the design cycle and rework costs.

That is why Teradyne has made Virtuoso Multi-Mode Simulation the core of their current major chip development projects. This kind of confidence comes from successful experience.