

# ***Full-chip electro-thermal simulation***

***using loosely coupled  
electrical and thermal simulators***



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**Session: 9.9**

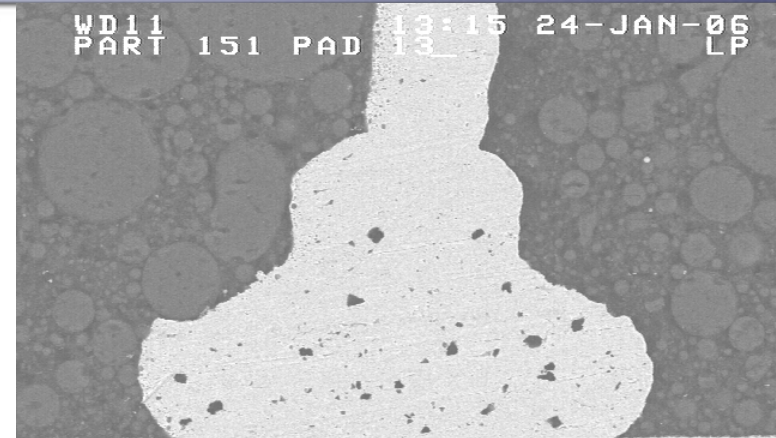
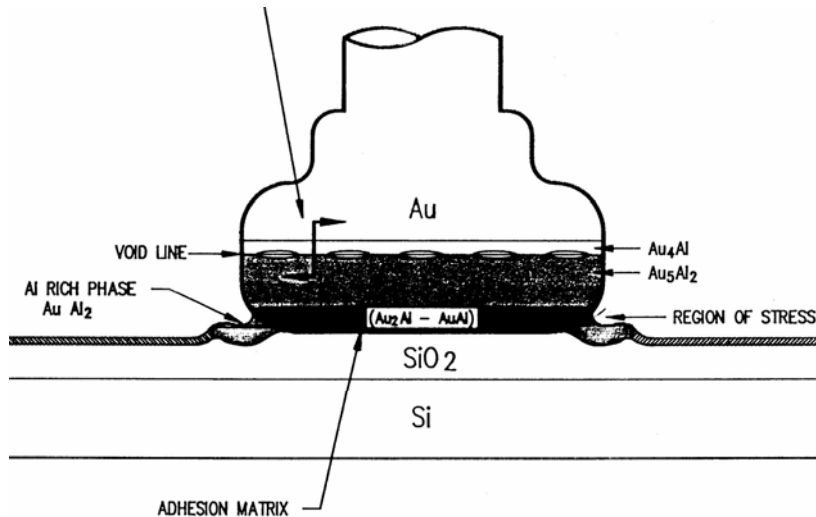
# ***Drivers for 3D dynamic ETH sims***

- ***Application profiles require higher temperature***
- ***Temperature head-room reduces (operating closer to max. temperatures)***
  - Thermal SOA (energy capability)
  - Bondwire / package reliability
- ***Power density goes up with improvement in performance of the technology***
- ***Higher integration levels place power components on-chip closer to sensitive analogue circuitry***

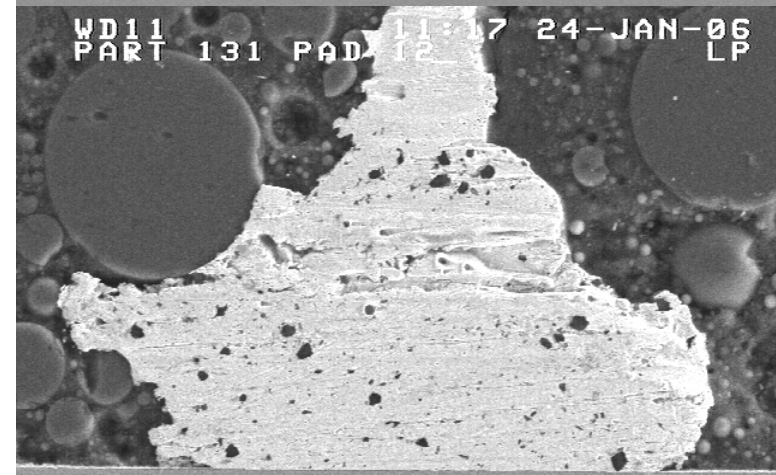
# Temperature headroom reduces

- **Package reliability**

- Molding compound degrades above a critical temperature :
- Accelerated degradation of wire-bonds :



Normal (fresh) molding compound



Decomposed after 225C bake

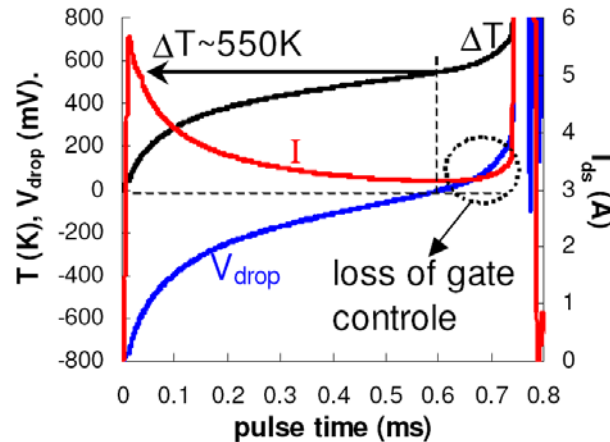
AMIS 15.0kV x1.00K 30.0µm

# Temperature headroom reduces

## ● Transistor Reliability

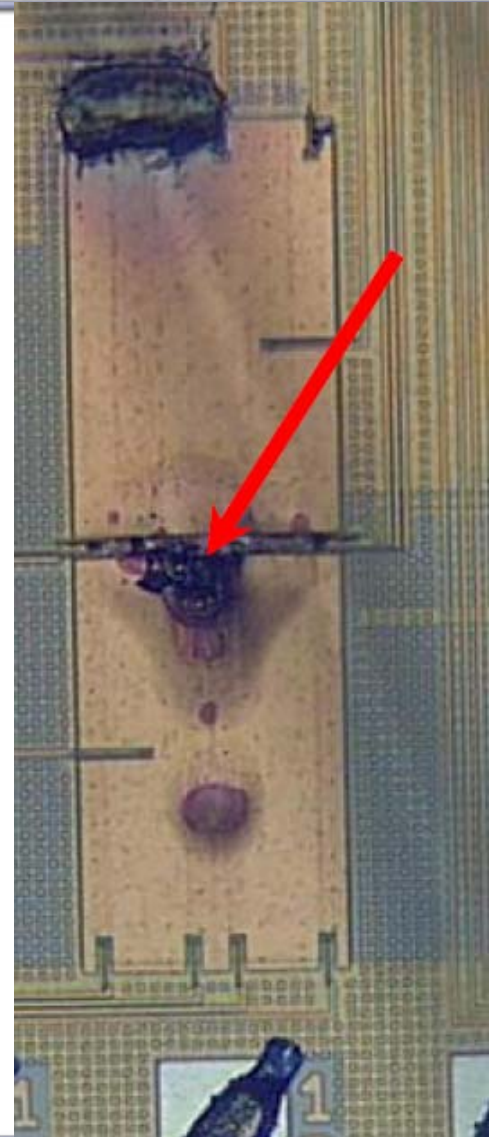
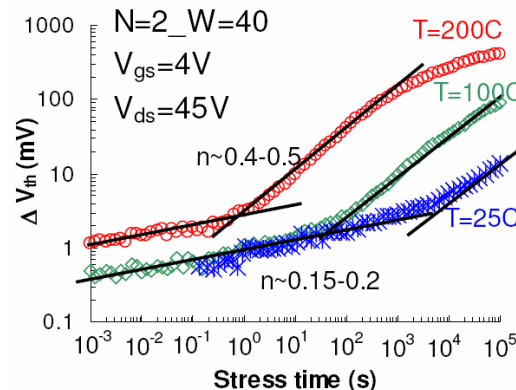
### ● Energy capability of power drivers

- Self-heating + activation of parasitic BJT
- **Destructive !**



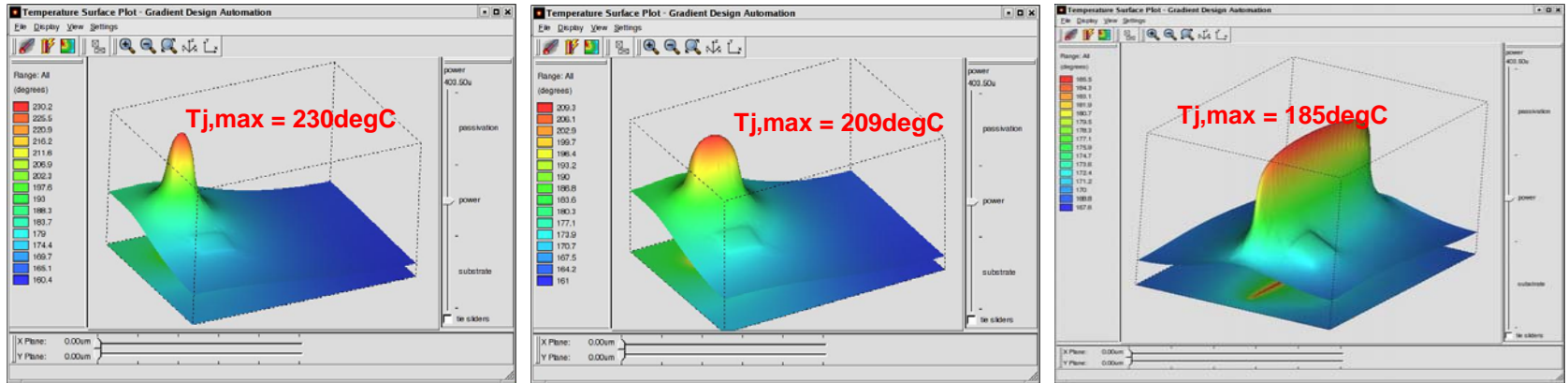
### ● Bias-temperature instability

- $V_T$  shifts over time at high temperature
- Both for LV as HV MOST's

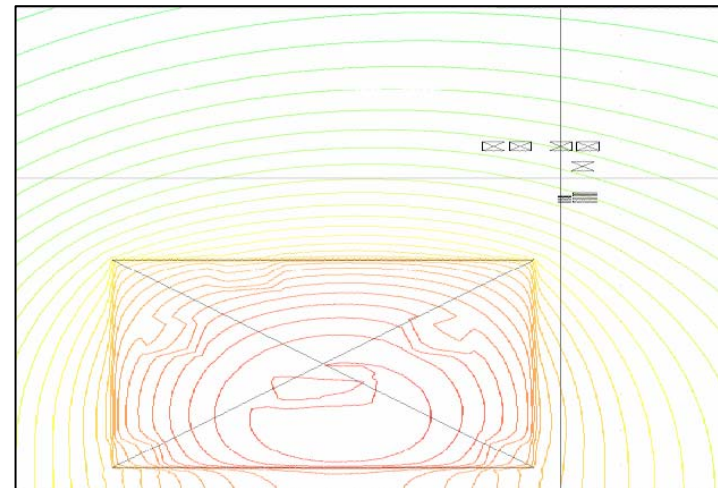


# AMIS usage of the tool

## ● Layout optimization for lowest $T_{Rise}$



## ● Positioning of blocks

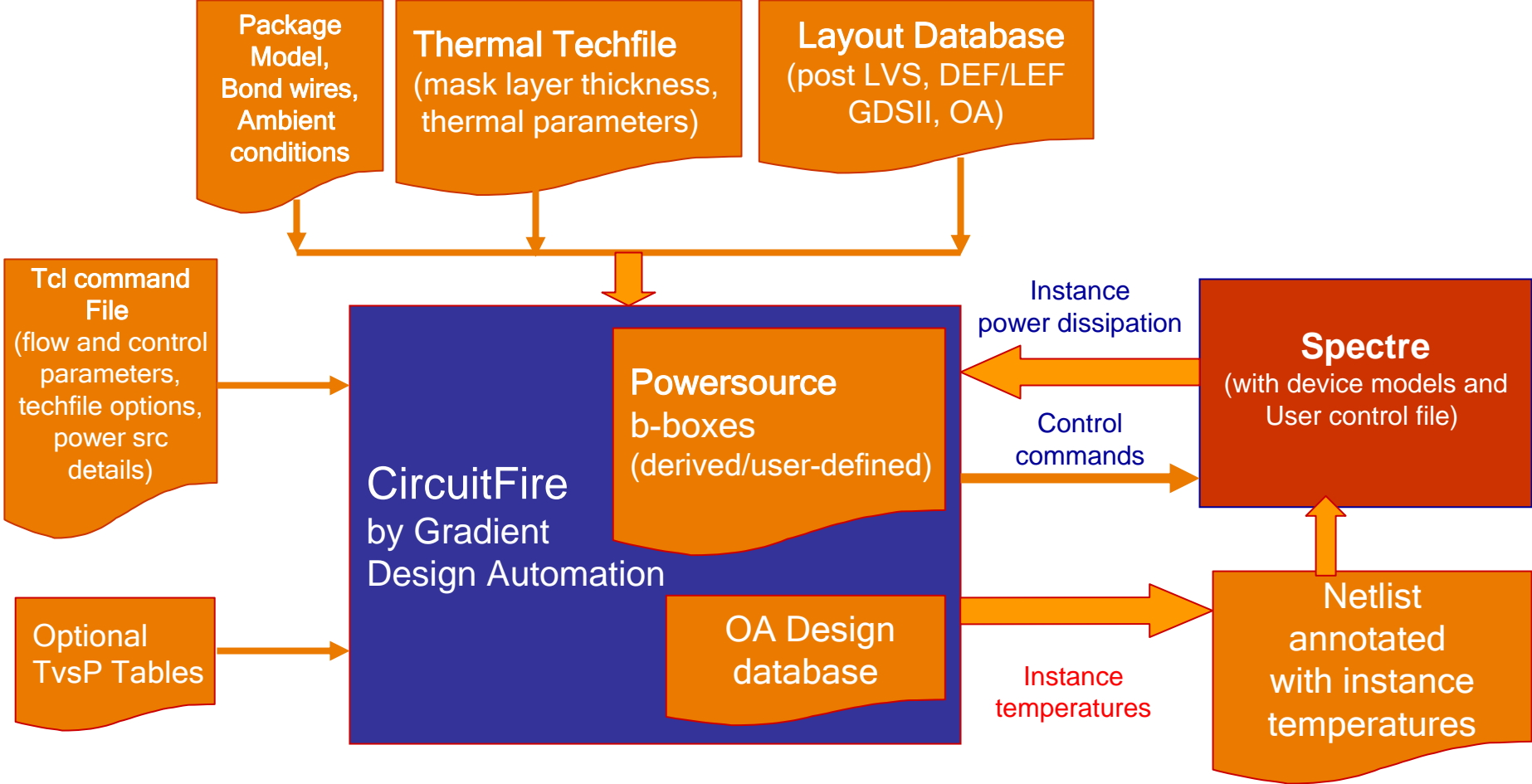


# ***ETH simulation tool specs***

- ***Annotate temperature at instance level***
- ***Automatic capturing of power dissipation from instances***
- ***Dynamic thermal response***
- ***Including electro-thermal feedback loops (power dissipation depends on the hotspot temperature)***
- ***Time-span of interest for the dynamic simulations***
- ***Impact of package, bondwires on temperature distributions***
- ***Evaluate alternative process options (thick metals)***
- ***Fast enough to simulate complete functional blocks***

# Architecture of the Gradient solutions

- **Static tool flow**



# Architecture of the Gradient solutions

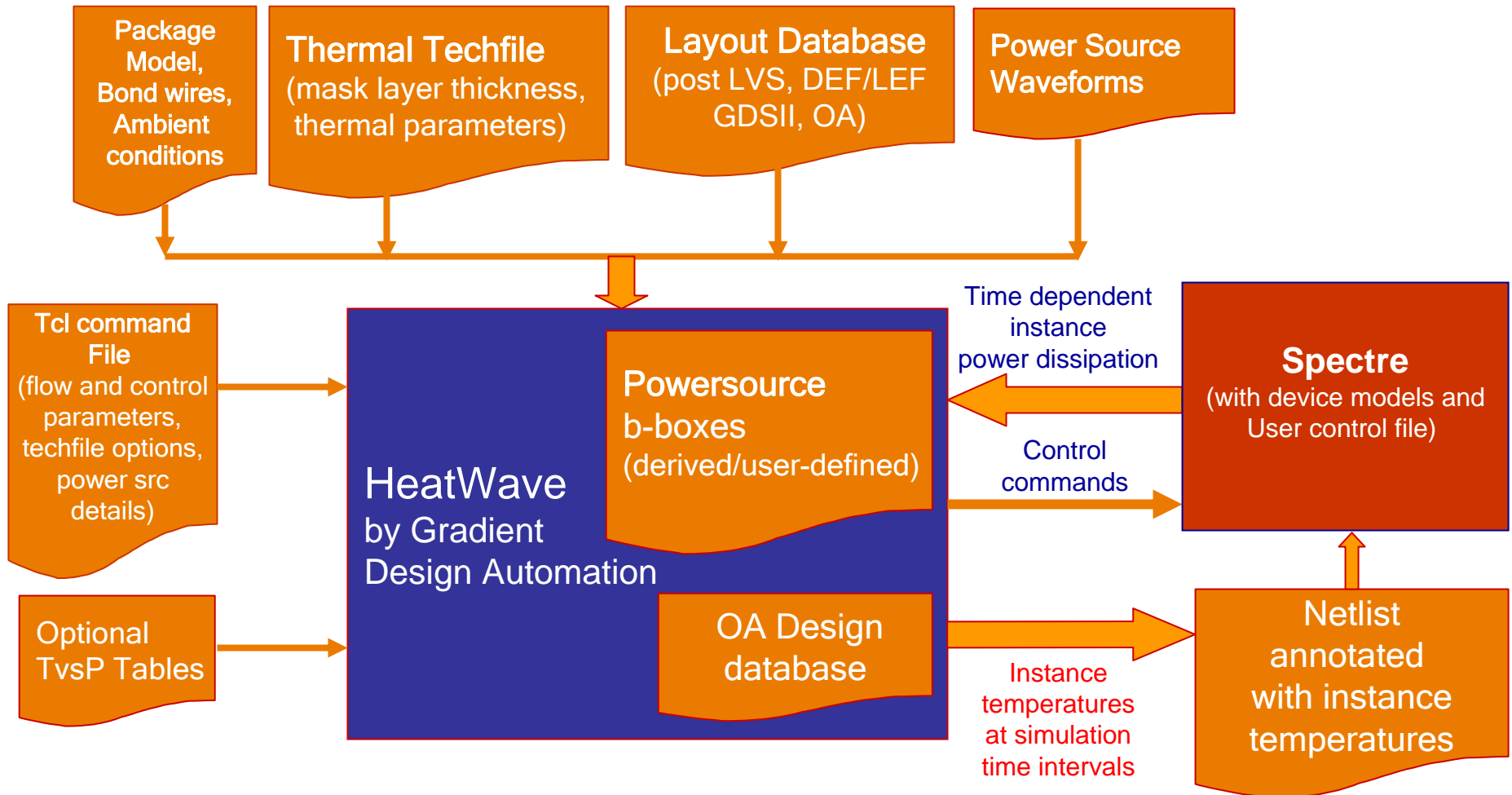
## ● **Static tool analysis modes**

- *Analysis modes support early stage design evaluation and detailed thermal analysis through:*
  - *Text based input for pre- and partial layout analysis*
  - *Full chip layout database for detailed, accurate analysis*
  - *Package interface compatible with  $\theta_{jA}$  and ambient conditions*
  - *Control parameters for runtime/accuracy tradeoff*
  - *Instance specific and wire shape temperatures for annotation to electrical analysis tools; Full 3D visual GUI analysis*
- *Goal: Detect and avoid thermal hazards and reliability failures early in the design flow!!*



# Architecture of the Gradient solutions

## ● Dynamic tool

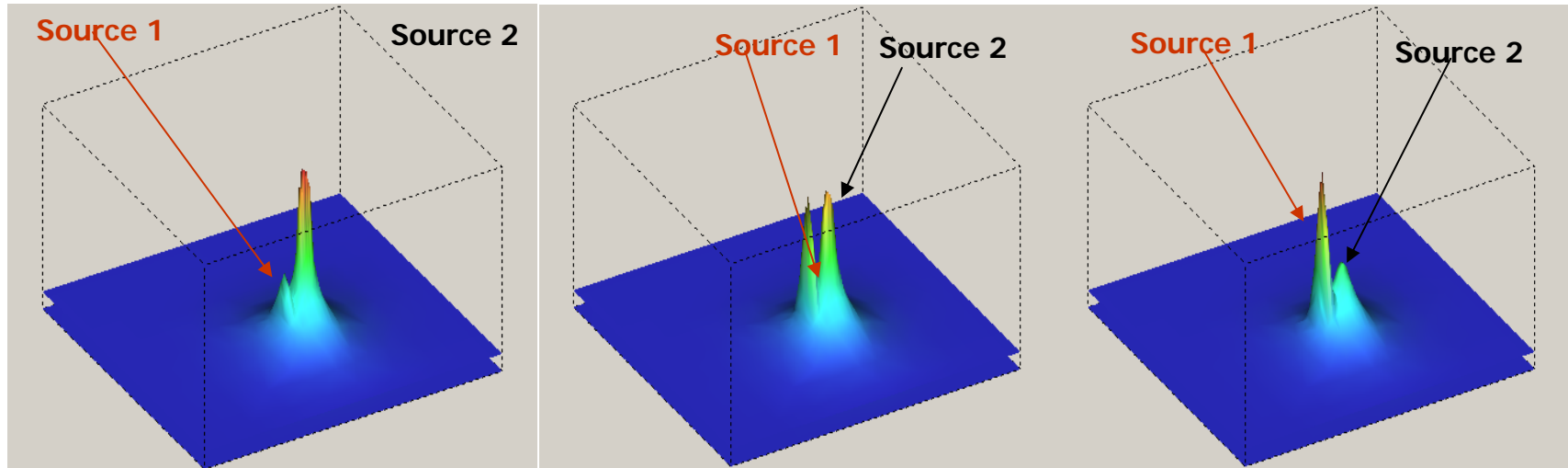


# Architecture of the Gradient solutions

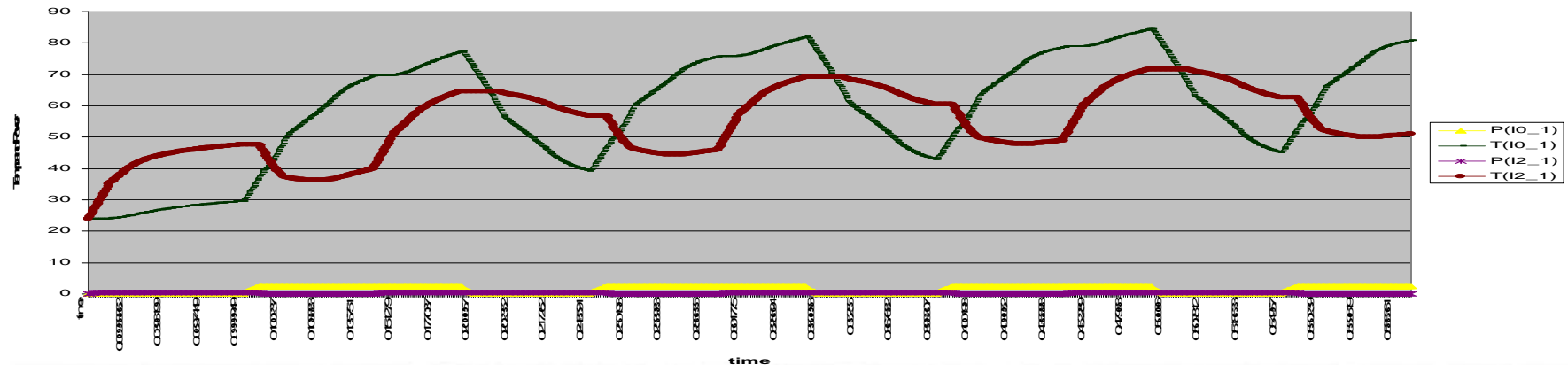
- **Dynamic tool analysis modes**
  - *Thermal hazard analysis due to transient temperature propagation during floorplan and post-layout stages with*
    - *Synchronized thermal simulation with user's electrical simulator*
    - *Adaptive time step control based on thermal parameters*
    - *Monitoring of min/max instance temperatures and temperature differences between instances as a function of time*
    - *Automatic reporting of temperature violations*
    - *User defined control parameters for speed vs. accuracy*
    - *Uses same design database as steady state*
    - *Interface with transient package models in progress*
    - *Visual GUI with pause and playback features for insight into transient thermal effects*

# Architecture of the Gradient solutions

## ● Dynamic analysis : surface plots & waveform



Two Transistor Power Sources



# Architecture of the Gradient solutions

The image displays two windows from the Virtuoso EDA tool. The left window, titled "Virtuoso® Schematic Editing: OPAMP opamp\_test schematic", shows a circuit schematic for an operational amplifier. The schematic includes an opamp component with input nodes labeled VN\_I and VP\_I, and an output node VO\_I. It features several voltage sources (vdc) and a frequency source (freq=2.5M). A context menu is open over the schematic, listing options such as "Setup Thermal Analysis...", "Extract Power Sources...", "Setup Simulator...", "Run Thermal Analysis...", and "About...". The right window, titled "Layout Editing: OPAMP opamp layout", shows the physical layout of the same circuit, with various components and connections rendered in a detailed, multi-colored style. A similar context menu is open over the layout. The status bars at the bottom of both windows show mouse coordinates and actions like "schSingleSelectPt()", "schHiMousePopUp()", "hiDisplayForm(gdaCreate", "leHiMousePopUp()", and "hiZoomIn()".

# ***Benefit of the loosely coupled scheme***

- ***Allows interface between HeatWave and existing electrical simulators***
  - Allows fast feedback of electrical power values
- ***Provides significant performance improvement***
  - Thermal network node count is orders of magnitude larger than electrical network
  - Low overhead of thermal simulator allows fast temperature updates to electrical simulation models
  - Compared with direct coupled simulation orders of magnitude speed-up!!
- ***Thermal simulation control parameters allow for speed-accuracy trade-off independent of electrical simulator***

# Conclusion & future work

## ● **Conclusions**

- We implemented a full-chip electro-thermal simulation flow
- Loose coupling between the electrical and the thermal simulators provides a more advantageous speed trade-off

## ● **Future work :**

- Package thermal model  
(transient successor to Delphi models)
- Incorporation SIP / APD flows (?)



# CONNECT: IDEAS

**CDNLive! 2007 Silicon Valley**