Use of AMS Verification Flow for Battery Management Design Simulations

Sundaram Sangameswaran, suam@ti.com
Daniel Pickens, pickens@ti.com
Texas Instruments

Session : #6.2

Objectives

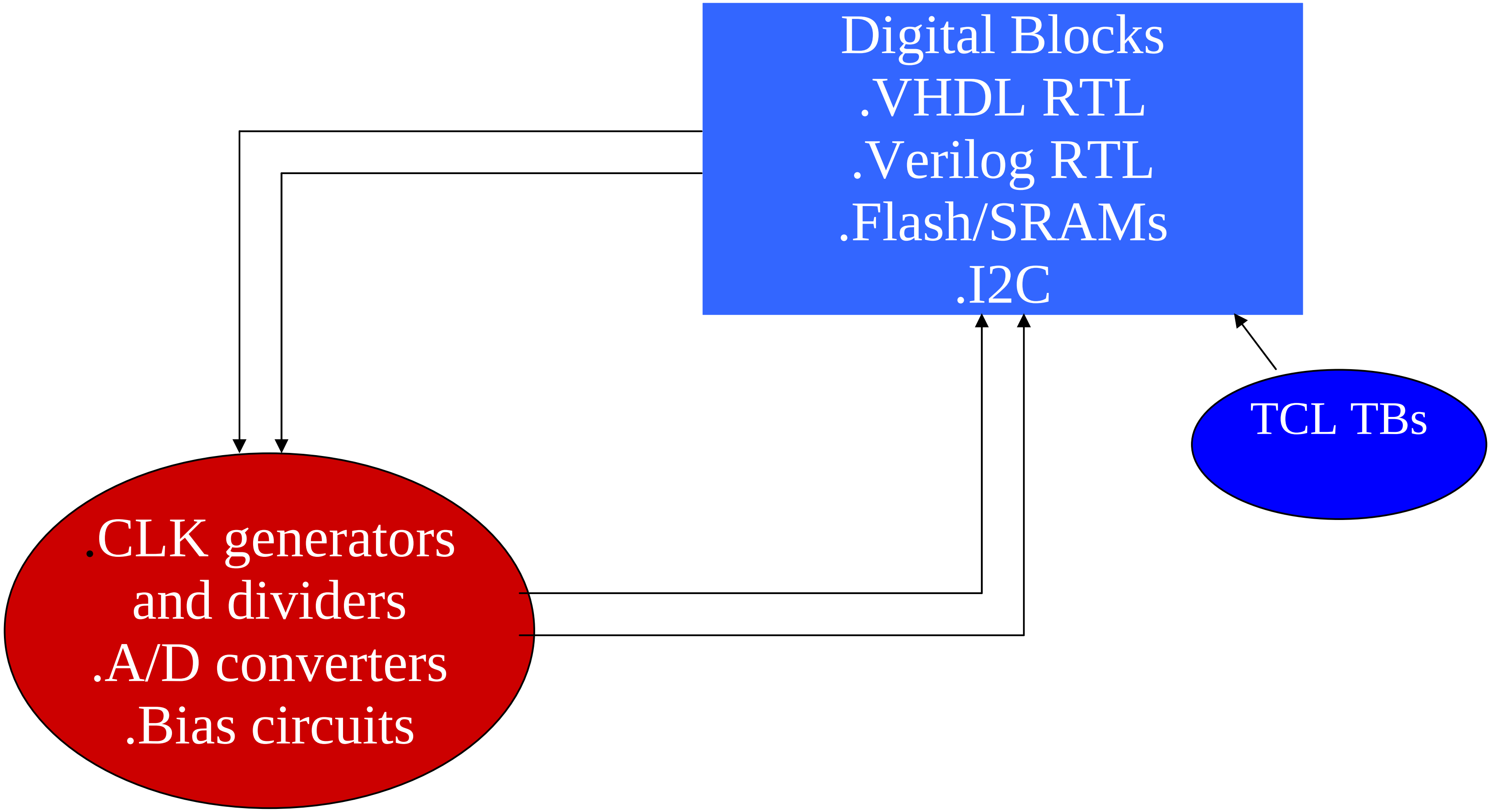
- Techniques for reducing top simulation time

4 days → ¼ day

Outline

- Top Level Design in Brief
- AMS Verification Flow
- Simulation of CLK generators
- Speeding up the simulation
- Checking A/D functionality
- Conclusions
- Acknowledgements

Design Details in Brief



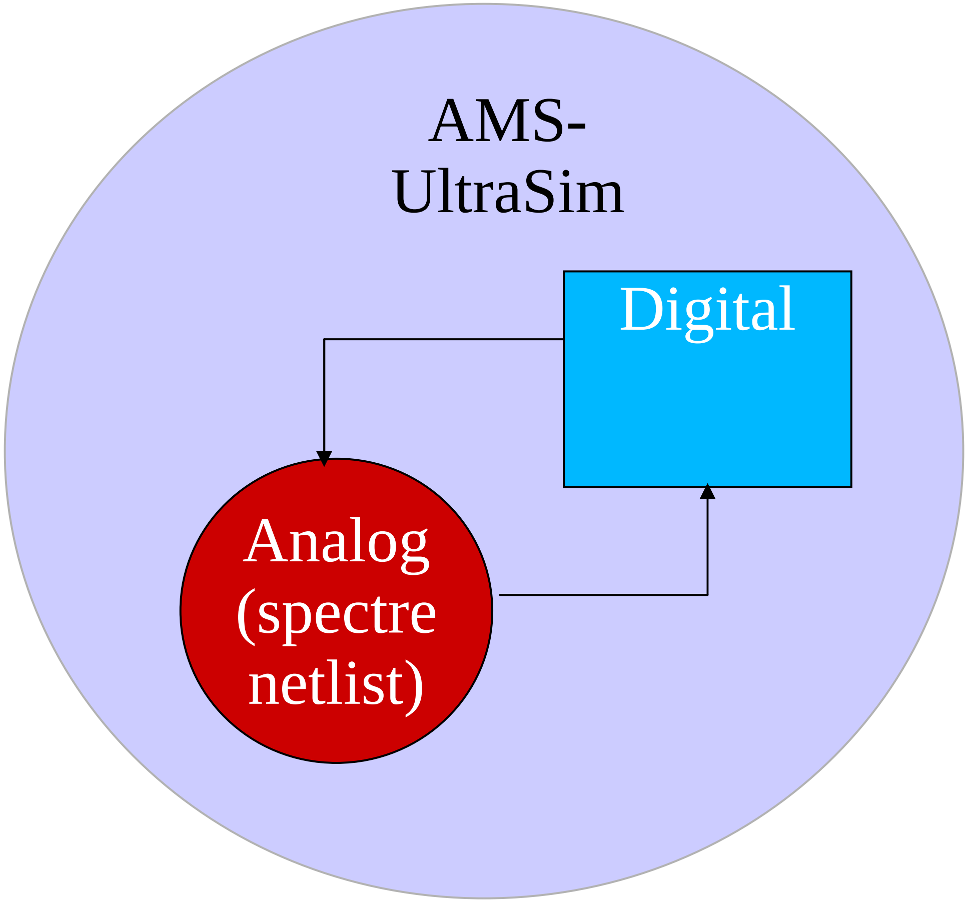
Digital Blocks
.VHDL RTL
.Verilog RTL
.Flash/SRAMs
.I2C

TCL TBs

.CLK generators and dividers
.A/D converters
.Bias circuits

AMS Verification Flow

- AMS verification flow uses AMS-Ultra from command line
- prop.cfg file reference the spectre files and connection properties
- -amsfastspice argument used during elaboration to invoke AMS-Ultra
- -propspath argument during elaboration points to prop.cfg file path



AMS Verification Flow

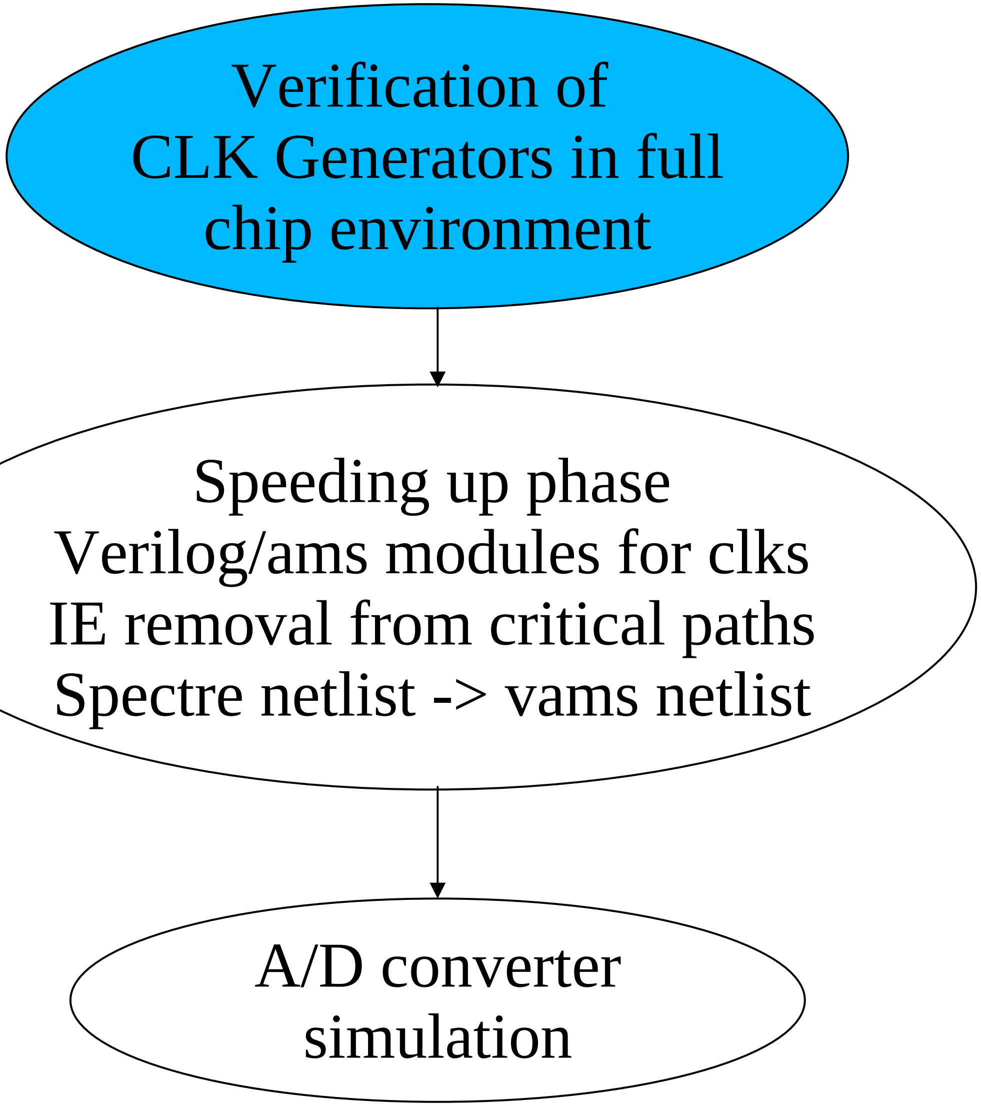
- ncelab command

```
ncelab –amsfastspice -propspath prop_sim.cfg
    <rest of the arguments>
```

- prop.cfg file contents

```
cell atop
  {
    string prop sourcefile="models/atop.scs";
    string prop sourcefile_opts="-auto_bus -input spectre -
     bus_delim {}";
  }
default
 {
   string prop hdl_cell="all_clocks, clocks, mux ";
 }
```

Design Verification Flow diagram



Verification of CLK Generators in full chip environment

Speeding up phase
Verilog/ams modules for clks
IE removal from critical paths
Spectre netlist -> vams netlist

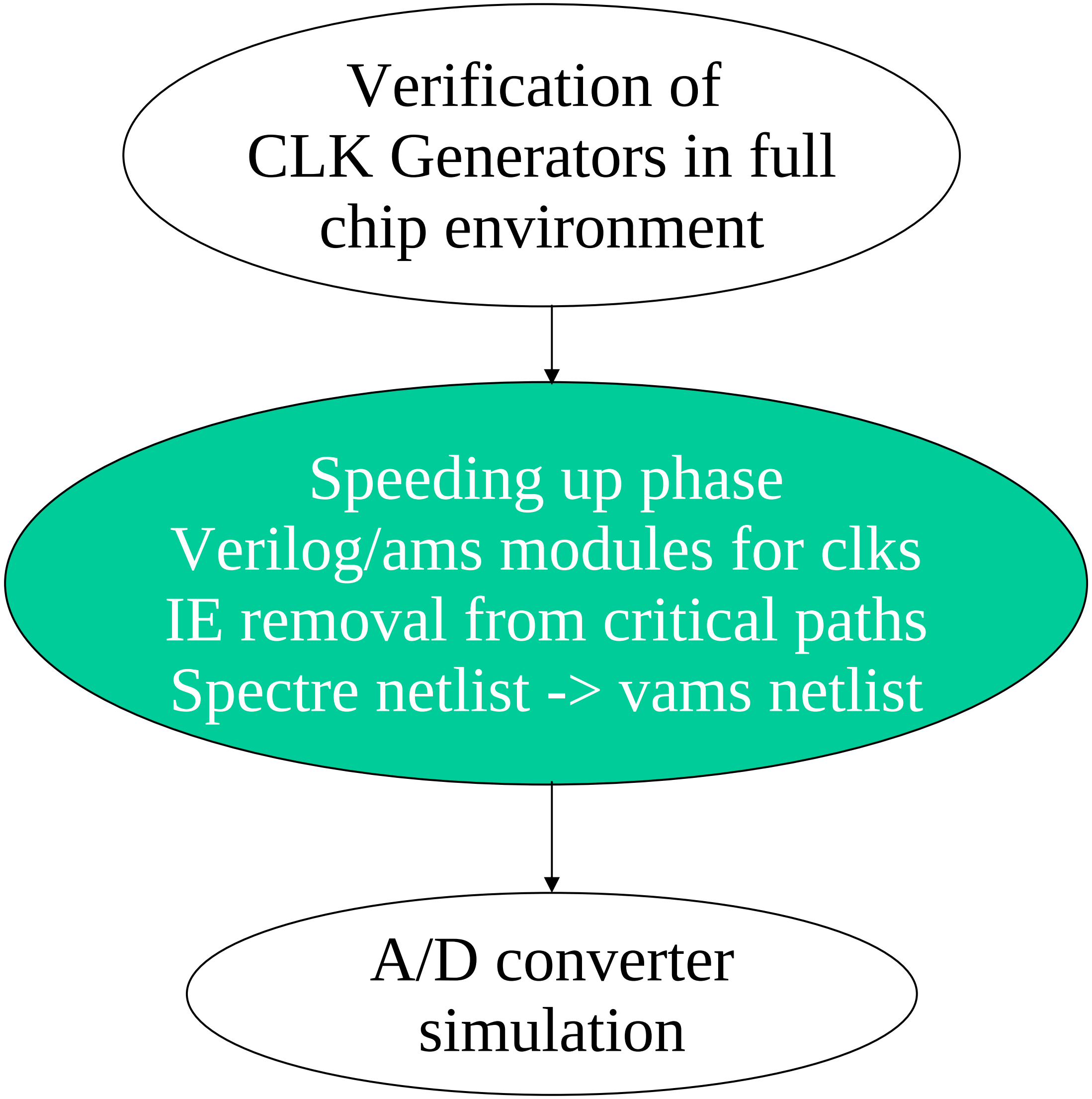
A/D converter simulation

21ms in 27 hrs

CLK Generators verification: Challenges & Solutions

- IUS 5.7_s005 & CIC 5.1.41.1.16
- Issues and Challenges
  - Missing pulses in A2D translation using cadence Interface Elements
  - Pins mismatch between spectre netlist and instantiation of module from verilog test bench
  - Clock used by communication engine had a hold off of approx. 4ms. Resulted in x propagation
  - 21ms simulation took 27 hrs to finish
  - Synchronization of simulators using run –sync in TCL scripts
- Solutions
  - UltraSim option changes resolved missing pulses issue
  - Realistic simulation required 4.2 ms setting for clock stabilization

Verification Flow diagram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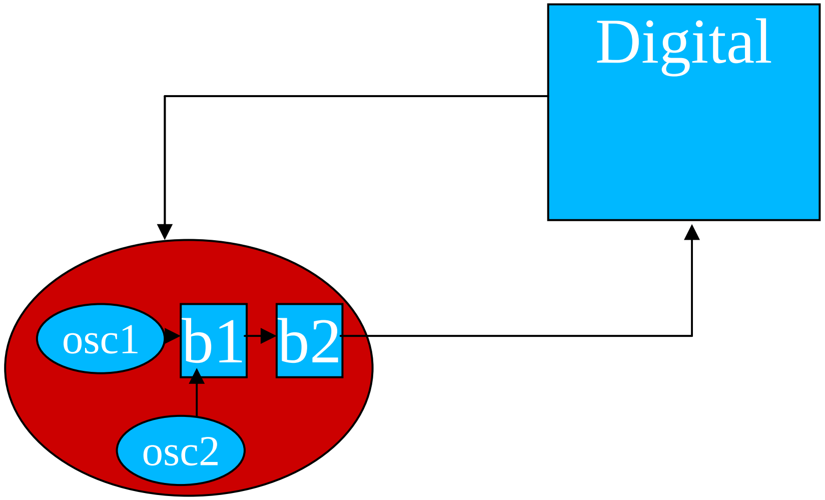
21ms in 18 mts

Speeding up Simulation

- Bind osc1 and osc2 to verilog model

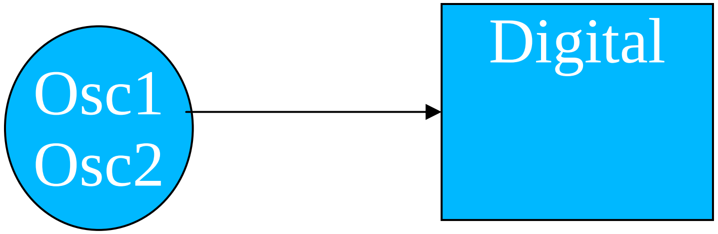


- Various UltraSim options

sim_mode, speed, analog and cell based settings. No dramatic speedup
default (ms, sp 5) --- functionality lost
global(ms, sp 5), osc(ms,sp 3) -- 25 hrs
Bias ckts and ref blocks using analogLib components --- ~11hrs

Speeding up Simulation

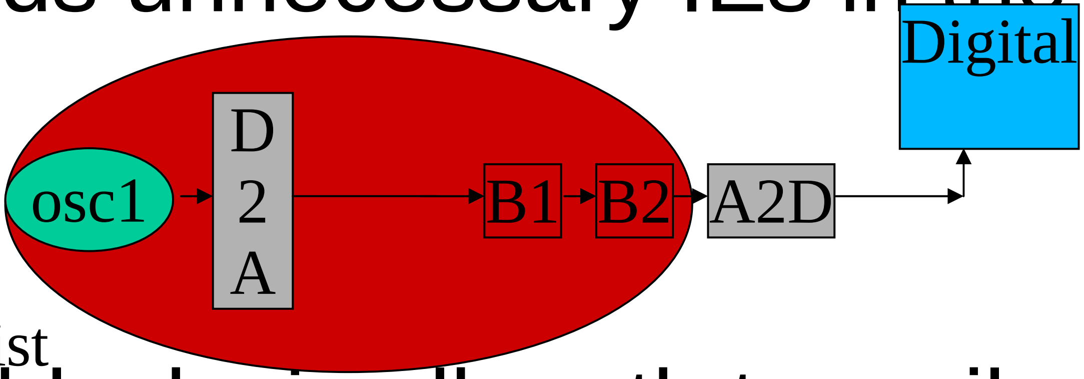
- osc1 and osc2 to verilog model, run all digital



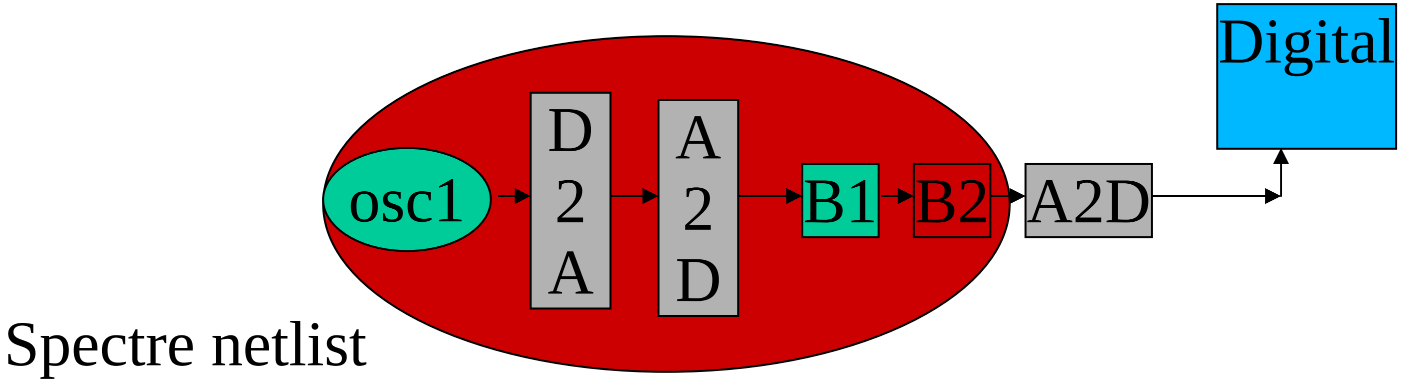
- Digital Simulation took just ~ 5 minutes
- Dummy analog blocks or simple schematics (using analogLib components) with verilog model for oscillators, did not provide dramatic speed up.
- What is the core issue in speeding up ?

Speeding up Simulation

- Verilog model oscillators in spectre netlist adds unnecessary IEs in the path



- Replace blocks in clk path to verilog models resulted in back to back IEs

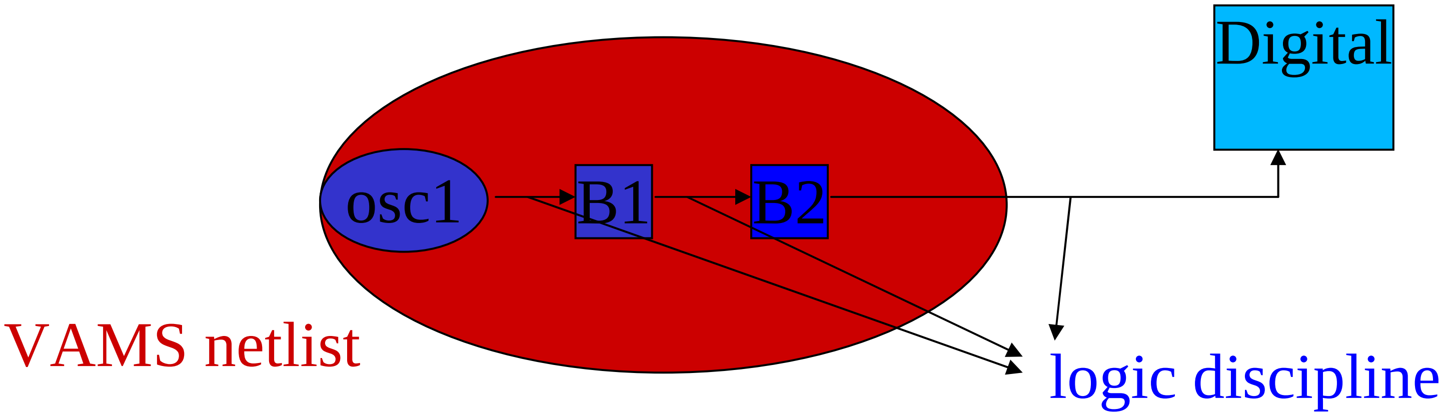


Speeding up Simulation

- sim_stub entry in prop.cfg does not work, manual edits performed to stub out subcircuits.
- hdl_cell property supports cell based bindings, instance based verilog binding not supported (PCR 924688)
- No proper documentation on prop.cfg file constructs for AMS verification flow

Speeding up Simulation

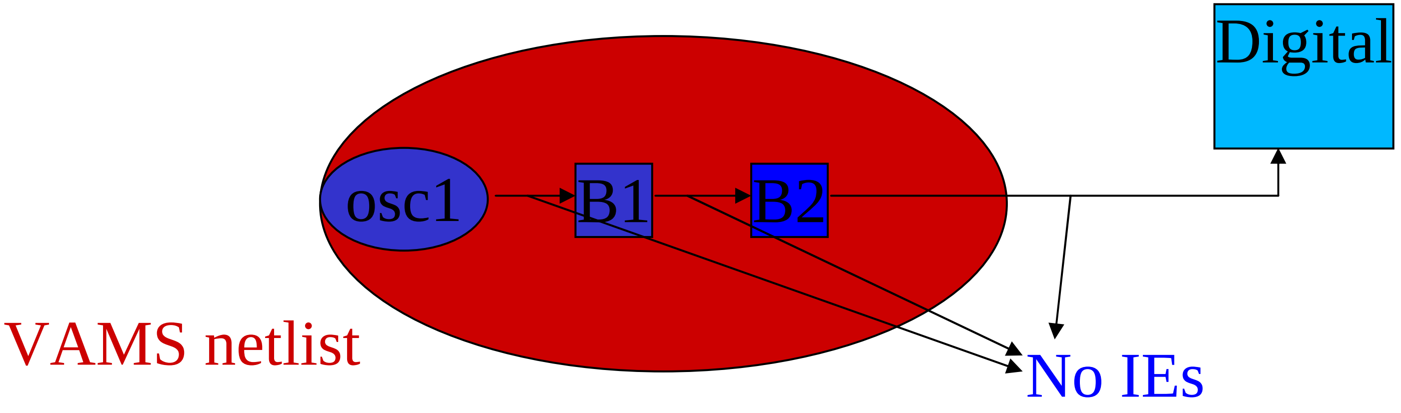
- To get better control on IE reduction, spectre netlist was replaced with VAMS netlist for analog blocks



- Selective structural VAMS netlist were edited to instantiate verilog or verilog ams modules

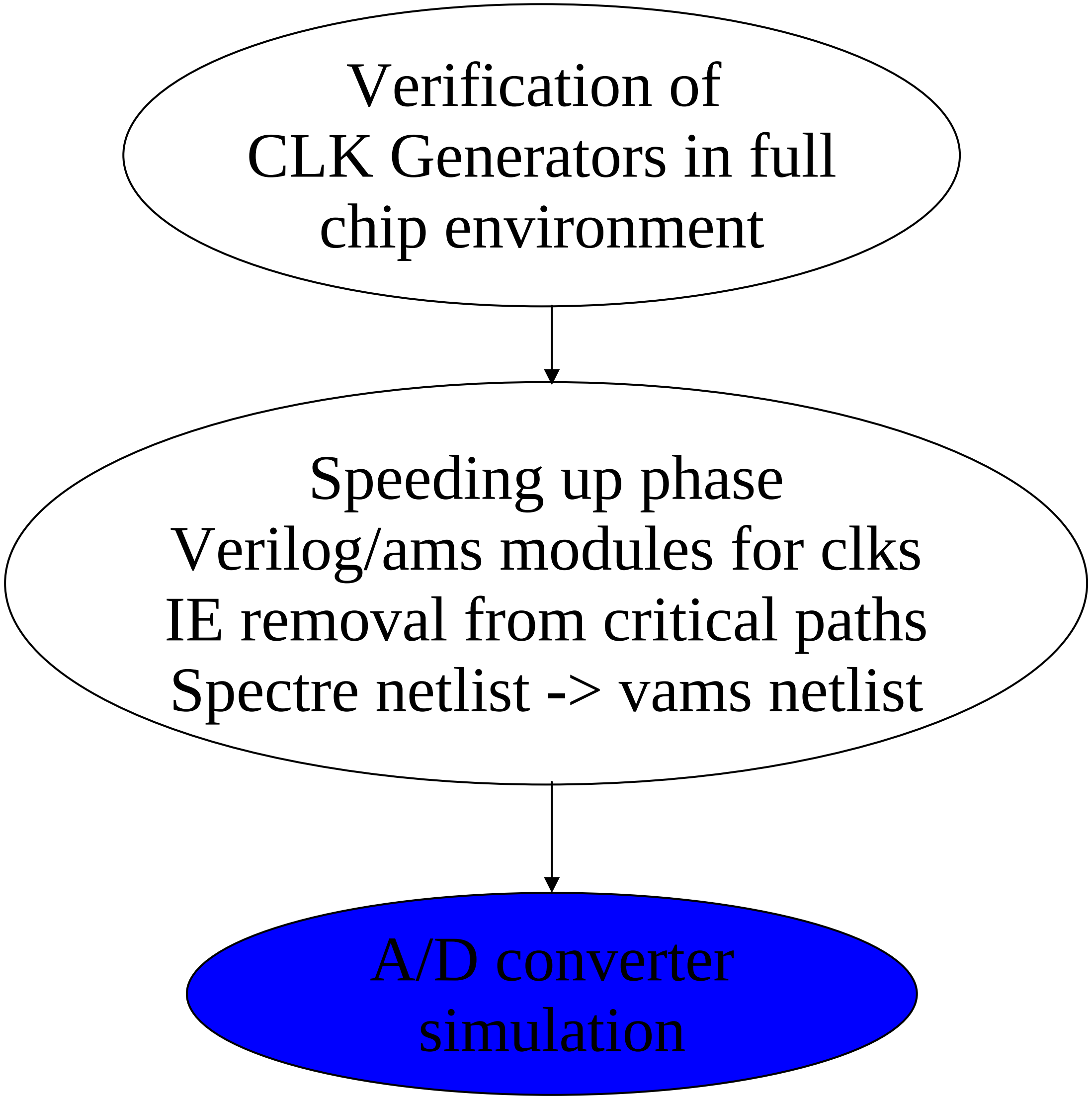
Speeding up Simulation

- Got rid off all the IEs in the critical CLK paths



- 21ms simulation took just ~19 minutes to finish

Verification Flow diagram



Verification of CLK Generators in full chip environment

21ms in 27 hrs

Speeding up phase
Verilog/ams modules for clks
IE removal from critical paths
Spectre netlist -> vams netlist

21ms in 18 mts

A/D converter simulation

83ms in 7 hrs

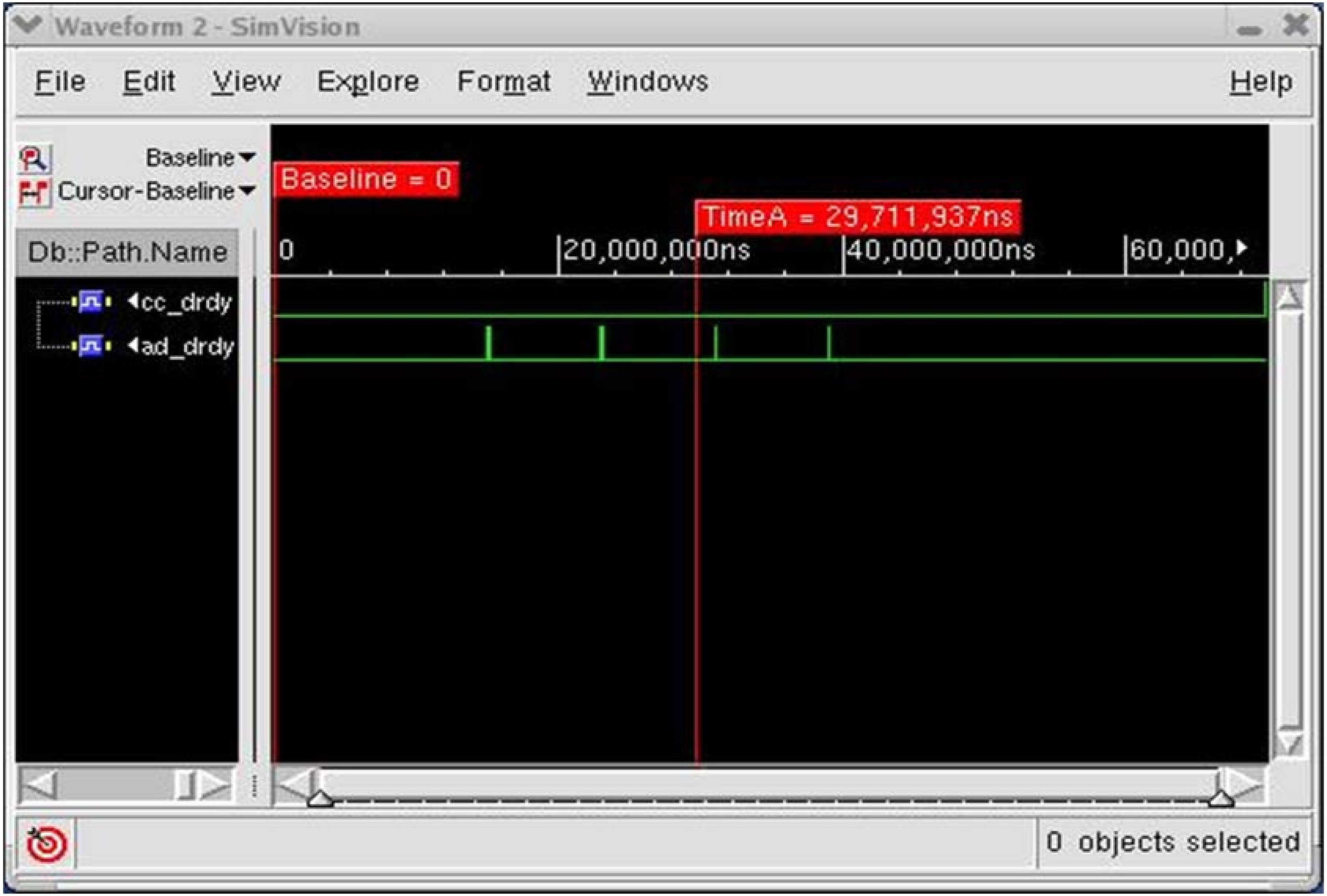
A/D Converters Simulation

- UltraSim Options

```
.usim_opt sim_mode=ms speed=6
.usim_opt progress_p=1 progress_t=10 dump_step = 25 u
.usim_opt sim_mode=df speed=8 #wkclk #admod_log #all_clocks
.usim_opt sim_mode=4 #hfo
.usim_opt sim_mode=ms speed=5 #rc_osc #muxed_dsm #dsm_cc
.usim_opt rshort=10m rvshort=10m
```

- 83 ms simulation run took just ~7 hrs on a 32 bit linux machine

A/D outputs of 83 ms run



Conclusions

- AMS Verification flow is easy to use flow for digital designers compared to ADE and EDEN flows
- IE reduction required moving to verilogAMS based AMS-Ultra flow
- Prop.cfg needs constructs for instance based settings and better documentation
- IE insertion in spectre netlist needs to improve and back to back IE placement is not good
- Better IE event deduction schemes in solvers, or better IE modelling to avoid missing pulses
- AMS usage in general is on the increase at TI, and able to perform number of top level simulations before tapeout

Acknowledgements

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  - Dallas team: Prashanth Konda
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- Battery Management Design team

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