

Cadence Encounter Digital Implementation System

The fastest, most deterministic path to power, performance, and area realization

Cadence® Encounter® Digital Implementation (EDI) System provides the most effective methodology to maximize performance, and minimize power and area for high-performance, 100M+ instance, and power-efficient designs. Integration with the Cadence Virtuoso® custom design environment ensures seamless data transfer and increases productivity for mixed-signal designs. EDI System also supports advanced 20/22nm and 14/16nm FinFET process technologies, and system-in-package/3D-IC design. With these capabilities, EDI System delivers the most comprehensive and deterministic solution for physical implementation and design closure of today's most demanding chip designs.

Overview

EDI System gives you an early, accurate view of design feasibility and allows you to progress immediately to full-scale, signoff-correlated implementation—without ever leaving the implementation environment.

EDI System combines early and rapid design exploration and accurate chip feasibility analysis (using unique and patented abstraction technology); automated floorplan synthesis; state-of-the-art clock tree and clock mesh synthesis; advanced nanometer routing; full-chip virtual prototyping; and full-chip digital implementation in a single environment. EDI System supports the implementation of high-performance, 100M+ instance, and mixed-signal designs. The solution also addresses the design scale, complexity, and manufacturing requirements with full support for a double-patterning methodology, FinFET technologies, and design for manufacturing and 3DIC/silicon-in-package capabilities. It also offers integrated, statistical analysis and optimization. With these capabilities, EDI System helps you achieve the best power, performance, and area within the most aggressive project timelines.

Benefits

Predictability and convergence

- Provides full-chip implementation in a single environment
- Enables design exploration and accurate chip feasibility analysis, including automated floorplan synthesis and ranking, as well as hierarchical budgeting and planning for convergent hierarchical implementation results
- Multithreaded GigaOpt optimization technology offers significant improvement in total negative and worst negative slack while delivering multifold improvement in turnaround time
- GigaOpt and CCOpt engines synergistically deliver better power, performance, and area results for high-performance designs at advanced nodes, allowing block implementation to meet and exceed aggressive design targets
- Achieves faster, more convergent timing closure by using same extraction engine during in-design and signoff

- Supports comprehensive multi-mode/multi-corner analysis and optimization in all steps throughout the flow
- Supports location-based on-chip-variation technologies and the latest methodologies for statistical timing and leakage analysis and optimization

Productivity and faster time to market

- Supports hierarchical methodologies including bottom-up block-based flows, top-down black-box flows, and hybrid flows with partitioning and time budgeting
- Key technology adapts to growing capacity requirements while still retaining the relevant timing, placement, and congestion information to accurately plan and implement 100M+ instance designs
- FlexModels provide up to 90% netlist compression and an optimized interface for accurate design exploration and planning, resulting in faster turnaround time and one-pass implementation handoff

- FlexILMs enable concurrent top- and block-level implementation for hierarchical designs; more transparent hierarchical abstraction; and fewer iterations during top-level optimization
- Supports a constraint-driven mixed-signal environment through the OpenAccess database, allowing for concurrent custom/digital design methodologies with smoother transitions between Virtuoso and Encounter environments
- Performs fast and accurate optimization and analysis in the flat physical implementation flow by leveraging the new multi-CPU/multi-threaded single-step timing and signal integrity delay calculation
- Delivers signoff-correlated design implementation including signoff ECO, as well as intuitive visual features for global timing, power, signal integrity, clock tree diagnostics, and performance scalability

Performance scalability

- Delivers industry-leading performance and capacity for 100M+ instance, complex chips
- Offers a complete, end-to-end, multi-core parallel processing backplane and infrastructure
- Provides best-in-class, efficient multi-corner functionality to significantly improve turnaround time

Differentiated product development with lower production costs

- Includes comprehensive support for 14/16 FinFET and 20/22nm designs to handle design scale and complexity as well as new DFM requirements
- Supports signoff-correlated double-patterning physical implementation , from design planning to placement and routing
- Enables concurrent chip/package co-design and optimization with integrated capabilities such as automatic area and peripheral I/O placement and flip-chip RDL routing

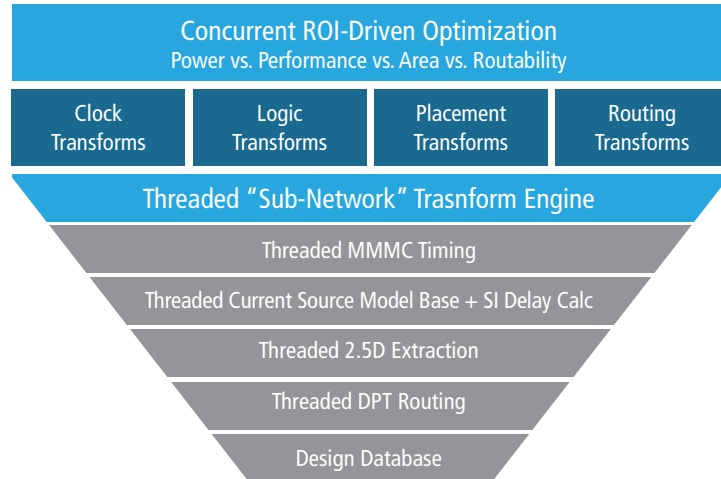


Figure-1: GigaOpt—built on a strong foundation of comprehensive transforms and multithreaded optimization technologies

- Allows floorplanning, implementation, and analysis of 3D stacked-die designs with through-silicon-via (TSV) connectivity for optimization of heterogeneous processes/dies, ensuring fewer iterations and faster convergence with in-design 3D-IC signoff extraction and timing/power analysis across multiple dies

Features

High-performance design

At smaller process geometries, designing a SoC for the next-generation server, smartphone, tablet computer, gaming console, or high-end wireless device requires implementing several complex subsystems (including high-performance CPU, GPU, DSP, video and image processing compute engines) and high-speed interconnect fabric. These designs are difficult to implement in silicon, especially with the aggressive performance targets at very low-power budgets. Customers in the consumer, mobile computing, wireless, and networking markets are moving ahead with 20/22nm and 14/16nm FinFET process nodes while pushing the envelope on power, performance, and area (PPA) metrics.

Key underlying technologies—such as the GigaOpt and natively integrated clock concurrent optimization (CCOpt)—help meet such overwhelming demands on

PPA targets at advanced nodes. These capabilities enable SoC implementers to differentiate their products without significantly escalating the costs of getting leading-edge designs to market.

GigaOpt

GigaOpt is an ultra-fast and multi-threaded/highly scalable optimization technology that provides better quality of results (QoR) with faster runtime. Delivering up to 3x runtime speed up, GigaOpt is the default optimization engine throughout the entire implementation flow, from pre-route optimization to post-route closure.

GigaOpt provides fast feasibility analysis to look at multiple floorplan what-if scenarios to accurately predict post-placement optimization results in a fraction of the full optimization time. It also includes critical path replacement transforms for path balancing and compaction; route-driven optimization taking advantage of lower resistance in upper layers of metal for timing gain; and better AOCV support for increased accuracy. These provide significant improvement in worst negative slack (WNS), total negative slack (TNS), and density while simultaneously reducing dynamic and leakage power across the board.

CCOpt

Clocking is the backbone of modern SoC designs, and clock tree synthesis (CTS) is an essential capability that distributes clock signals to the data registers. Implementing a design's complex clock system is an inherent part of designing a high-performance SoC. In today's SoC physical design flows, CTS is separate from physical optimization. While this approach has generally worked down to the 40nm node, it has broken down at advanced nodes because on-chip variation, low-power demands, and complexity are causing a significant "timing gap" between the ideal clocks used pre-CTS and the propagated clocks used post-CTS.

Cadence clock concurrent optimization (CCOpt) is a unique approach to timing optimization that holistically addresses this timing gap. CCOpt brings the realm of physical optimization into CTS, optimizes the clock insertion as well as logic delays simultaneously, and eliminates post-CTS optimization steps. Observed results have included significant clock-tree power reduction, clock-tree area reductions, and chip performance improvements. No manual tweaking of clock trees and skew balancing is necessary. CCOpt performs multi-threaded concurrent useful-skew and datapath optimization with the powerful GigaOpt optimizer, as well as time borrowing for faster timing closure, leading to significant productivity improvements. Additional benefits include reduction in IR drop (because registers and RAMs are triggered at different times) and a skew profile that reduces peak current without any impact on timing.

CCOpt and GigaOpt combine to provide unprecedented improvements to power, performance, and area, and to turnaround times for today's high-performance designs at advanced nodes. Bringing these technologies together, Cadence has jointly developed state-of-the-art RTL-to-signoff foundation flows with industry-leading silicon IP vendors for high-performance 64- and 32-bit micro-

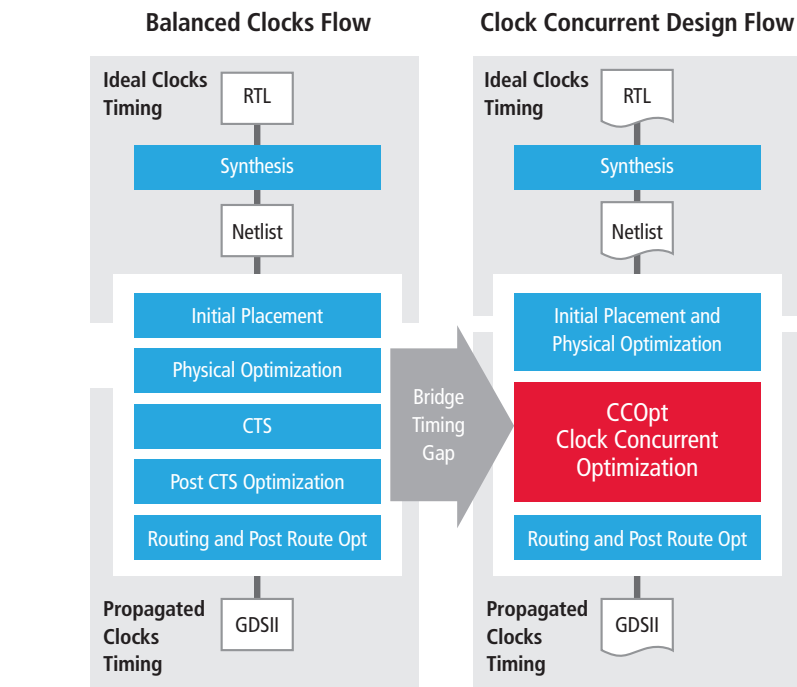


Figure 2: CCOpt offers improved clock design for high-performance and low-power designs

processor-based designs. These flows help you achieve optimal PPA with reduced effort and increased productivity.

Power management

EDI System is an integral part of the Cadence Low-Power Solution. This comprehensive methodology supports the Common Power Format (CPF), which captures all power-specific design intent, from power-aware design planning to signoff-correlated final implementation. The underlying infrastructure of EDI System automates the daunting task of managing power intent, reducing leakage power, and optimizing power consumption simultaneously during physical implementation without degradation in design performance and area. Driven by CPF, EDI System low-power flow makes designing with multi-VT, multi-power-domains, power shutoff, dynamic voltage and frequency scaling, and substrate biasing a lot easier and faster, from floorplanning to placement, to clock tree synthesis and signoff-correlated routing optimization.

Today's low-power designs also have to work seamlessly in a hierarchical flow and leverage the abstraction advantages of integrating IP models from other sources. To ensure a seamless hierarchical flow and IP integration, Cadence offers hierarchical low-power macro modeling of black boxes. This helps you take advantage of hierarchical abstraction as well as the scalability of integrating IP in low-power designs.

Advanced global debug and diagnostics

Debug and diagnosis challenges often come late in the design cycle, along the critical path to final tapeout. EDI System provides timing, power, signal integrity (SI), and clock debug and diagnostics capabilities that allow you to quickly locate and visualize interdependent timing, clock, SI delay and glitch, and power issues, and then quickly resolve those using powerful "what-if" analysis techniques. These results can be immediately implemented in physical design.

100M+ instance hierarchical design

With design sizes increasing toward the 100M+ instance range, it's critical for systems to handle designs of such scale. Key technology greatly expands the system's capacity to handle designs of 100M+, helping you achieve full-chip design prototyping goals; uncover potential issues earlier; and meet timing and SI requirements on multiple extraction corners and up to 100 multi-mode/multicorner (MMMC) timing views, allowing you to produce the most optimal design floorplan. Concurrent top- and block-level hierarchical implementation reduces iterations and total design cycle time for such large designs. In addition, signoff engineering change order (ECO) capability leverages a multi-CPU and multi-threaded backplane with fast and accurate extraction to enable fully automated, physically aware, high-capacity timing ECOs applicable at the full-chip level.

Early design exploration

Today's physical design teams start physical implementation and design planning very early in the design cycle—with early and multiple versions of the design netlist—to determine design feasibility. EDI System closes the gap between architecture and implementation, addressing questions such as whether the design can be implemented in the required area, and if it will operate at the desired speed.

- Key technologies extend patented FlexModels to provide necessary netlist compression with the accuracy and fast turnaround time needed to handle 100M+ instance designs
- Production-proven automated floorplan synthesis couples timing, power, area, and congestion-aware placement with fast global routing and in-place optimization, so you can quickly generate prototype floorplans
- Automatic macro placement capability generates macro placement results that are convergent with implementation

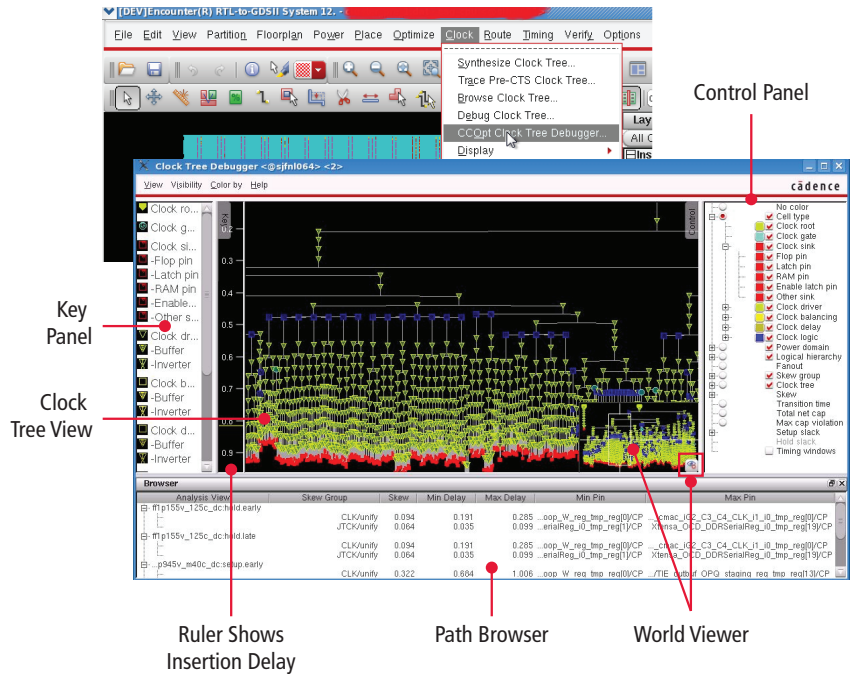


Figure 3: Interactive CCOpt clock-tree debugger

- Built-in editing capabilities such as relative floorplan (specifying relationships for pre-routes, resizable objects, multiple relations, datapath stacking, integrated analysis tools) and resize floorplan help you quickly and accurately reach an optimal final floorplan
- A floorplan ranking system automatically generates multiple floorplan scenarios in parallel and analyzes them based on pre-defined QoR criteria; you can explore as much of the physical solution space as possible and make the most informed tradeoffs
- System designers can link into EDI System from Cadence Chip Planning System to bring physical predictability into their estimations

Silicon virtual prototyping and hierarchical support

Full-chip flat prototyping delivers complete physical, timing, clock, and power data, eliminating the guesswork associated with traditional block-based approaches. Hierarchical support helps physical designers assess how best to partition the logical hierarchy into physical modules. You can analyze the optimal pin assignments, budget time quickly, predict

the clock distribution networks accurately, analyze the power grids, and generate complete timing and physical constraints for each of the physical modules.

Hierarchical implementation and closure

FlexILMs technology enables concurrent top- and block-level optimization and hierarchical implementation. With FlexILMs, EDI System can optimize the top-level design concurrently with interface logic of block-level partitions, resulting in fewer iterations and a faster path to accurate budgeting and hierarchical convergence. This reduces the number of iterations taken to close top-level timing with block-level timing, resulting in a significantly shorter overall design turnaround time.

Signoff ECO

Signoff ECO provides a fully automated, physically aware timing ECO capability applicable to the full-chip level. Using a highly efficient multi-CPU backplane coupled with a fast and accurate parasitic extraction engine, this signoff-driven timing ECO capability automates static timing analysis, optimization, and retiming of all timing views in the design. It is based on timing-critical paths reported by

the unified timing signoff engine, leveraging the same engine to perform timing ECOs in order to fix remaining violations. This high-capacity signoff ECO solution is optimized for execution on up to 100 timing views and has the performance to handle giga-scale designs at the full-chip level, greatly reducing the effort, the number of ECO iterations, and the closure time required for post-route design closure on timing ECOs.

Support for mixed-signal design

The amount of analog circuitry on SoCs is multiplying, and at the same time, the use of digital control logic inside analog blocks is growing. This results in mixed-signal designs with “analog” and “digital” components. The Cadence Mixed-Signal Solution, utilizing OpenAccess as a single design database, enables analog and digital designers to retain their own preferred design environments while increasing implementation efficiency through easy and seamless data transfer between Virtuoso and Encounter design platforms. Both analog and digital teams can easily see the complete design and any changes that might have been implemented by their peers, enabling efficient full-chip optimizations that were previously unobtainable.

This additional interoperability has proven extremely valuable during design stages when both analog and digital design teams need to carefully coordinate and agree on potential modifications, and where simply saving the database allows everyone on the design team to see the latest status in their own environment. ECOs can be managed more easily since they no longer require the generation of LEF/DEF/GDSII files to communicate the changes.

Comprehensive full-chip static timing analysis has always been challenging for mixed-signal designs, typically because the custom/analog designers had to manually create Liberty (.lib) files for their completed mixed-signal blocks. EDI System has a unique ability to perform comprehensive static timing analysis by transcending the analog hierarchy and abstracting the digital logic and paths.

Today, power efficiency in mixed-signal SoCs is a must for a wide range of end applications. EDI System supports Cadence interoperable mixed-signal solutions. It enables designers to effectively implement complex power distribution across analog and digital logic while managing overall design constraints to meet timing and area requirements.

The Cadence comprehensive mixed-signal implementation solution combines all of the strengths of EDI System—including design closure, signoff analysis, advanced node design, and low-power design—with the industry-standard Virtuoso design platform for custom/analog design, accelerating mixed-signal design success.

Digital implementation methodology for advanced node design

The PPA benefits of 22/20nm and 16/14nm process nodes enable you to produce differentiated products that are faster, more integrated, smaller, and with more functionality. However, these new process technology nodes must address new requirements such as double-patterning and FinFET device structures, while handling a significant increase in design rules.

EDI System introduces signoff-correlated design implementation with correct-by-construction double patterning support. These double patterning capabilities span floorplanning, placement, optimization, routing, parasitic extraction, and signoff for timing, power, and physical verification of designs with double patterning.

Other key EDI System features include:

- FinFET support in all EDI System placement, optimization, and routing steps
- Optimized cell placement for double-patterning requirements, leading to better area efficiency
- NanoRoute® Advanced Digital Router with FlexColor technology, which routes in a correct-by-construction manner; metal is routed to be DRC- and double patterning-correct using a built-in physical verification engine during all stages of routing

- Cadence QRC Extraction, which produces multi-value SPEF files required for mask-misalignment modeling. Cadence Encounter Timing System utilizes minimum and maximum capacitance values on early and late launch and capture clock paths for setup and hold timing analysis. Cadence Encounter Power System has enhanced analysis capabilities for power and signal electromigration analyses
- Consideration of intrinsic waveform effects by Encounter Timing System during signoff timing analysis, including back-miller current effect that acts as an aggressor to affect timing delay
- Cadence Physical Verification System, which provides in-design signoff for DRC and double-patterning conflict checks

Advanced process variation support

In addition to providing foundry-supported signoff technologies for timing, SI, and power during implementation, EDI System employs advanced on-chip variation (AOCV), which uses logic level and physical location to select the optimal de-rating factor. AOCV eliminates the excessive guard-banding associated with traditional de-rating, improves timing closure, and is available for timing analysis and optimization.

EDI System also supplements traditional single- and multi-corner-based methods with powerful and accurate statistical static timing analysis (SSTA) that accurately accounts for variability of process parameters in a single run. Using effective current source models (ECSMs), EDI System identifies cells and nets on both clock and data paths that are sensitive to variations, and then determines the probability of timing failures over the full scope of the process window. This reduces pessimism and limits guard banding, which in turn reduces both area and power consumption while improving chip performance.

SSTA and statistical leakage analysis and optimization capabilities further reduce design cycles by eliminating the need for multiple analysis runs. You can tape out with the confidence of using a foundry-

endorsed statistical solution to achieve and improve your timing and power goals in silicon.

Design for manufacturing

Design for manufacturing (DFM) is a mandatory step in the IC design flow for advanced nodes. Traditional methods of addressing DFM variability issues at signoff are impractical; they cannot handle increasing design complexity and they have long turnaround times. Advanced node design requires starting with the end in mind; it requires in-design DFM to scale diverse design needs from blocks and IP to large SoCs.

Encounter in-design DFM focuses on maintaining designer intent and leveraging accurate abstraction of manufacturing issues to deliver fast silicon convergence for DFM variability hotspots. Production-proven, silicon-accurate signoff DFM technologies are integrated with EDI System to minimize the risk of yield-limiting DFM hotspots and reduce the electrical variability impact early in the digital implementation flow.

EDI System users can leverage the Encounter DFM advanced analysis capability, in which silicon failures or variability hotspots are abstracted into patterns while maintaining the original design intent. This accurate abstraction reduces the turnaround time for DFM check analysis during digital implementation with EDI System by 100x, saving several days of DFM error iteration cycle time from the signoff stage.

Other features include:

- Context-driven placement, which takes layout electrical effects into account during implementation, resulting in better chip performance
- Wire spreading, wire widening, double-cut via insertion, and single via reduction and optimization
- Critical area analysis and optimization

- True lithography distortion prevention and optimization, and CMP-aware metal fill
- A rich set of random and systematic visual analysis and text-based reporting vehicles

3D stacked-die support

Today, vertical chip packaging schemes are being extended to the system level. A 3D stacked-die design environment enables companies to use a heterogeneous process while achieving even smaller silicon and package footprint sizes and higher performance for interconnect-intensive designs. EDI System fully supports the design, verification, and implementation of 3D stacked-die designs using:

- A consistent, unified environment that leverages 3D-IC intent (configuration file) to drive creation, implementation, and verification of 3D stacked-die designs across digital, full-custom, and packaging domains
- A 3D stacked-die chip/package/test abstraction and methodology that provides the speed and scalability to optimize heterogeneous processes/dies
- In-design 3D-IC signoff extraction, timing, power, and thermal analysis across multiple dies to ensure fewer iterations and faster convergence

Concurrent chip/package co-design with flip-chip support

Proven through multiple customer tapeouts, EDI System flip-chip floorplanning and implementation technologies enable the concurrent design of chip and package by including package constraints and parasitic effects while designing the IC. With support for multiple I/O methodologies, concurrent optimization of area and peripheral I/Os with core instances, automatic RDL routing with 45-degree support, and accounting for RDL layers during signal/

power routing, EDI System eliminates the traditional manual steps in I/O placement and optimization.

Platforms

- Inx86: Linux (x86 and x86_64) 32/64-bit
- sun4v: Solaris (ultraSparc 64-bit)
- ibmrs: AIX (power) 64-bit

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more



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