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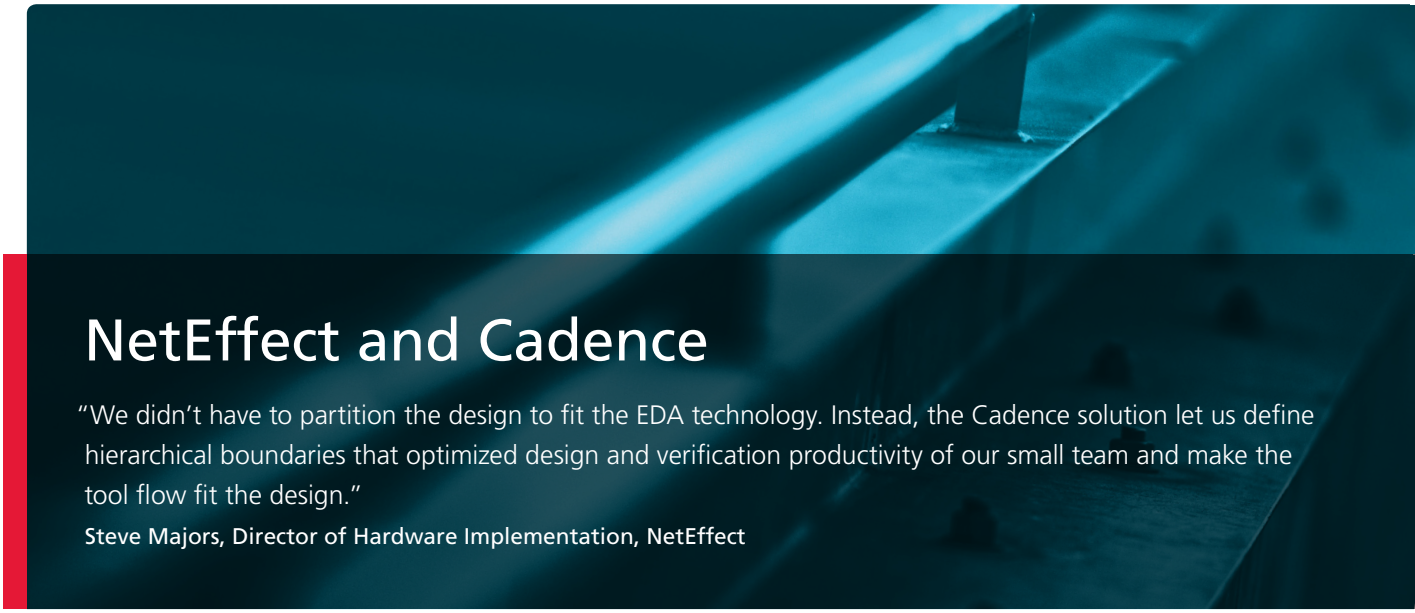

NetEffect and Cadence

"We didn't have to partition the design to fit the EDA technology. Instead, the Cadence solution let us define hierarchical boundaries that optimized design and verification productivity of our small team and make the tool flow fit the design."

Steve Majors, Director of Hardware Implementation, NetEffect

The Customer

Ethernet has served as the backbone of the datacenter network for the past quarter of a century. With network speed increasing tenfold every five years, its traditional protocol has been strained to the limit in the quest for 10Gbps capacity. This is partly because Ethernet manages all transactions through the central processor—an approach that, in high-traffic situations on current networks, can slow down the CPU by as much as 40%. Moving to the next generation of 10Gbps solutions requires offloading network overhead from the CPU to a separate chip.

NetEffect, based in Austin, Texas, has its engineering firmly rooted in these next-generation network speed and management issues. NetEffect also recognizes the opportunity 10Gbps Ethernet offers for network convergence in the datacenter by bringing clustering, networking, and storage traffic through a single network infrastructure. But supercomputer clusters and network storage systems use Remote Direct Memory Access (RDMA) to—unlike Ethernet—bypass the operating system bottleneck. An industry consortium set out to bridge these differences with a new standard—the Internet Wide Area RDMA Protocol (iWARP).

The Challenge

The key challenges for NetEffect were to offload the communications management task from the CPU, reduce memory bandwidth utilization and latency, and implement direct access standards without disrupting the host software stack. Despite these changes, the chip still supports legacy standards.

The size of the chip required hierarchical partitioning of the design to allow the flexibility to make tradeoffs at the end of the design process, rather than restrict options to simplify the design

Business Challenges

- Deliver the world's first full implementation of the iWARP standard in a single chip to enable converged networks
- Leverage outsourcing to augment a small in-house team

Design Challenges

- First full ASIC implementation of a 9M+-gate design
- Conflicting requirements for die size, timing closure, and low power

Cadence Solutions

- Encounter RTL Compiler with global synthesis technology
- Encounter Conformal Equivalence Checker
- Encounter Timing System
- Encounter Test
- Incisive Design Team Simulator
- QRC Extraction

Results

- World's first full implementation of iWARP standard in a single chip
- Converged network capabilities

flow. This enabled a very small team to use a divide-and-conquer approach—i.e., working on each of the blocks individually, rather than having to work on large numbers of blocks in parallel. It also enabled the team to isolate and spend more time on the blocks that were more challenging.

The Solution

Cadence software had a major impact on the NetEffect team's productivity by allowing them to focus on difficult areas, and minimized the probability of having to re-spin the chip at the end.

Facing the prospect of a completely new architecture and the need to design from scratch, NetEffect looked at all of its options, outsourcing as much as possible, yet keeping control of the key areas. The company had a very experienced team, but did not have the resources in-house to cover all the steps to tape out.

"We were able to maintain the maximum amount of control over the design, without necessarily taking on a lot of risk or investment in internal infrastructure… It was a very good fit for us."

The NetEffect project leaders had worked with Cadence in the past with good results. Cadence offered the flexibility to get what they really needed without having to make any tradeoffs. Each side could focus on the areas in which it excelled. NetEffect had the added security that, in case of any surprises, it could rely on the complementary design capability of Cadence Services to keep its project on schedule.

"We were able to maintain the maximum amount of control over the design, without necessarily taking on a lot of risk or investment in internal infrastructure," says Steve Majors, Director of Hardware Implementation, NetEffect. "It was a very good fit for us."

Critical Steps to Meet Area and Timing Goals

NetEffect used a complete Cadence flow and augmented the flow with services for areas of expertise not staffed on its team. The NetEffect designers used Cadence® Incisive® Design Team Simulator, Cadence Encounter® RTL Compiler with global synthesis technology, and Encounter Conformal® Equivalence Checker for front-end design and verification tasks, and they used the full Encounter suite for floorplanning, physical synthesis, clock tree synthesis, routing, extraction, timing analysis, and noise analysis. Cadence Services used Encounter Test and Cadence VoltageStorm® technology for power analysis and design for test (DFT). Cadence also provided full services for mask verification including DRC, LVS, and antenna checks.

Encounter Conformal Equivalence Checker was used at each step of the design flow where the netlist was automatically or manually modified to verify the integrity of the design.

The team felt that Encounter RTL Compiler with global synthesis delivered a significant number of benefits to the project. The first impact was the capacity of the software. Its higher synthesis capacity enabled optimal partitioning of the design. Larger chunks in each synthesis run, along with the ability to do incremental compiles, allowed the team to optimize better across a greater number of functional units. This resulted in fewer iterations and produced better area and timing optimizations overall. NetEffect was able to reuse generic RTL modules, and Encounter RTL Compiler with global synthesis would automatically and intelligently prune out unused logic, saving time while also meeting area goals.

"When we initially tried to compile the design with other tools, it was too large and congested to fit within the area budget," Majors says. "The efficiency of the adaptive approach in RTL Compiler combined with the flexibility of the pruning options enabled us to route the design without compromising any of the design goals."

"The tool features are definitely better than other products we've tried in terms of the post-route quality of results," Majors continues. "Another significant benefit was that Encounter RTL Compiler synthesis minimized the logic in a way that the formal verification software could understand without having to waste effort defining hint files."

This capability was critical to achieving NetEffect's design goals. Extra design functionality had to be added to the original floorplan late in the design cycle. The synthesis engine's ability to drive efficient area utilization made these additions possible without having to increase the die size.

Timing was just as difficult. The depth of logic was very aggressive for the given clock period of the design. Encounter RTL Compiler was able to find the solutions necessary to meet timing goals in spite of these challenges. At the same time, the tool was able to meet low power constraints applied to the library and design.

The end result was that greater compiler capacity and a faster synthesis engine led to fewer iterations for tapeout. The NetEffect team estimates that Encounter RTL Compiler shaved at least one month off the schedule to close die size, timing, and power goals including full-scan DFT.

Unsurpassed Performance

Principal Engineer Chih-Shun Ding compared Cadence to others: "In the past couple of years that we've been working with Encounter RTL Compiler and other leading synthesis tools, we have seen the Cadence solution consistently giving us results that are 5-10% better in timing, area reductions, and logic capacity," he says.

When asked about usability, Ding says, "Encounter RTL Compiler has newer data structures that are more intuitive. In terms of ease of use and productivity, I would say that Encounter RTL Complier has the edge."

"Once the compile scripts are optimized for the design environment, Encounter RTL Compiler tends to work consistently well across most design blocks," he adds. "Other tools tend to require a wider variety of custom scripts for different blocks on the chip."

There were other key components of the solution. Ding sums it up: "The combination of Cadence NanoRoute® noise avoidance and Cadence CeltIC® noise analysis stands out for its ability to reduce the number of false noise violations that we had to review and repair. This is very beneficial at the end of the design process, when there is extreme time pressure to tape-out the design and get it into manufacturing. Often the noise fixes have an impact on timing. The timing and noise analyses are well integrated within the Encounter system enabling fast and easy convergence."

For the signoff extraction, the team used Cadence QRC Extraction and produced accurate results that were later exercised in the timing and signal-integrity flows. Its seamless integration with the Encounter platform offers an easy-to-use solution for rapid analysis to achieve faster timing closure and higher quality of silicon.

The team also liked the easy-to-use TCL interface and seamless integration with the rest of the Encounter platform. The ability to access the database in a single environment and automate the process was a big advantage.

Timing analysis was another area in which the Encounter platform performed exceptionally well. NetEffect also had Primetime licenses for signoff static timing analysis (STA), and the correlation was within 1% on all modes and corners.

"Just as Encounter RTL Compiler synthesis has achieved full parity with Design Compiler, Cadence has now reached the same stage with timing analysis," Ding says.

Services Complete the Team

NetEffect also wanted to work with a vendor that could offer both software and services. They found that Cadence could not only provide the needed expertise in design for test and physical verification, but also had the staffing flexibility within Cadence Services to apply unplanned resources to new tasks if internal resources had to be reassigned or became unavailable.

NetEffect felt that its engineers and the Cadence Services team worked as one team on the project.

"Cadence Services were very collaborative and proactive," Ding says. "They pushed us as hard as we pushed them."

The division of labor along lines of expertise was not only an efficient way to fill in staff, but the result was always smoothly integrated into the NetEffect work flow.

"Cadence Services did a fabulous job with design for test and automatic test pattern generation, using Encounter Test," Ding says. "The test patterns are fully verified on the tester. We are now augmenting the flow with on-chip PLL-driven transition fault vectors to enable at-speed testing in order to address small delay defects."

The contribution from the Cadence Services team was also essential to the success of their aggressive schedule.

"Cadence Services delivered on everything they were asked to do, without any impact to NetEffect's schedule," Ding concludes. "This high level of performance is pretty rare. They always met the schedule that we agreed to, and the deliverables always met our expectations."

Summary

Using Cadence products and services, NetEffect achieved its goal—the world's first full implementation of the iWARP standard in a single chip that enables converged network capabilities.