Mixed Signal Verification Methodology Using AMS-Ultra

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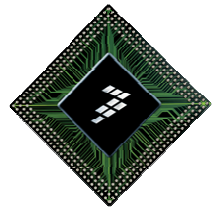


Challenges of Wireless Design

High Speed & Compact Design

- Nanometer technology

C65 Low Power Design

- Dynamic Voltage Frequency Scaling
- Power Gating (SRPG/S&R PG)
- Various Voltage Islands

Reduced Time to Market, Production Cost

- First pass Functional Silicon
- High yield results

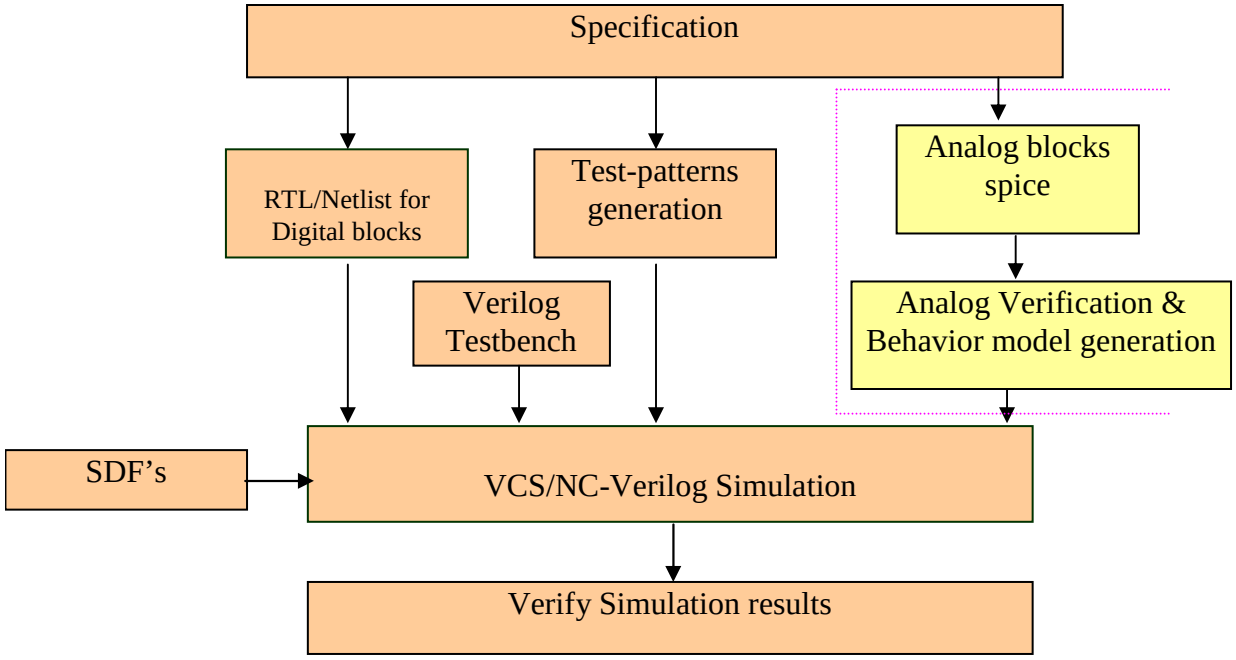
Impact

- Interface between Analog and Digital design becomes critical
- Interface between various voltage Islands are most critical
- Interfacing between Global power controller and power gating switches

Agenda

- Traditional Verification Flow
- AMS-Ultra Verification Flow
- Objective of AMS-Ultra flow
- Results
- Methods Adopted to speed-up simulation
- Design flaws detected with AMS-Ultra
- Bugs Reported in AMS-Ultra
- Enhancements required in AMS-Ultra
- Conclusion
- Acknowledgement

Traditional Verification Flow



Issue 1.

Don't mimic full functionality

Impact

- Probable Timing, Functional failures
- Inappropriate Voltage levels

Issue 3.

Missing Interface timing between Digital & Analog block

Analog Verification`

Digital Verification

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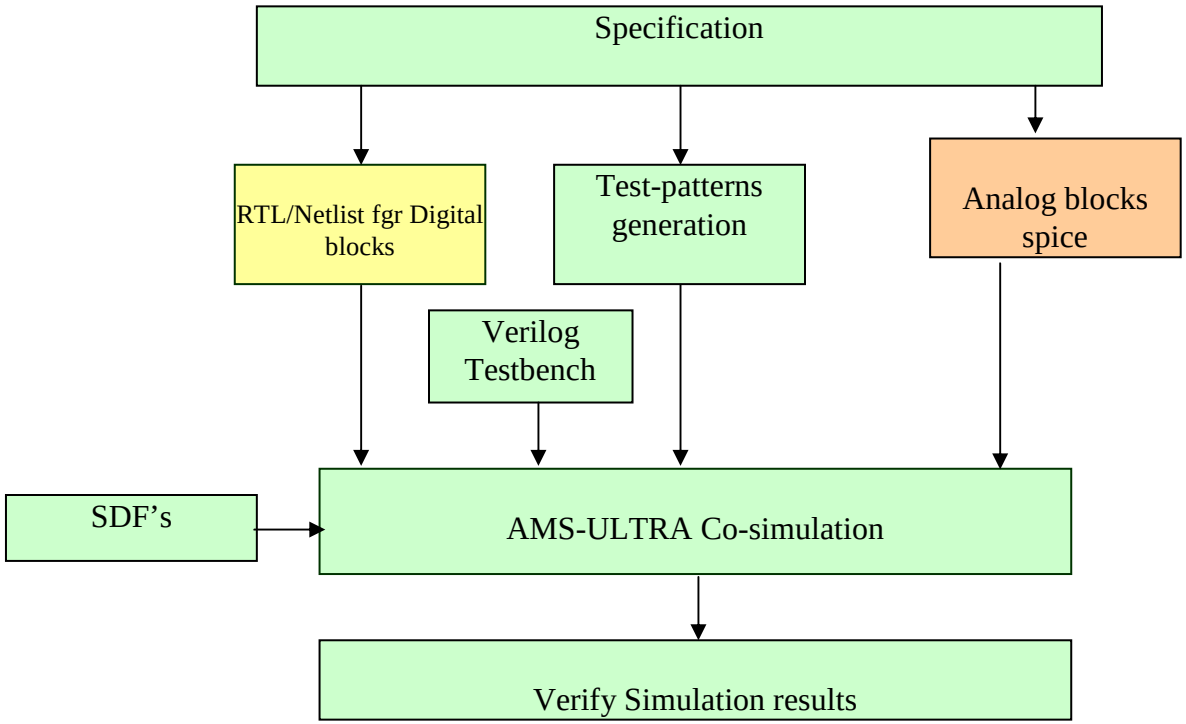
AMS-ULTRA Verification Flow

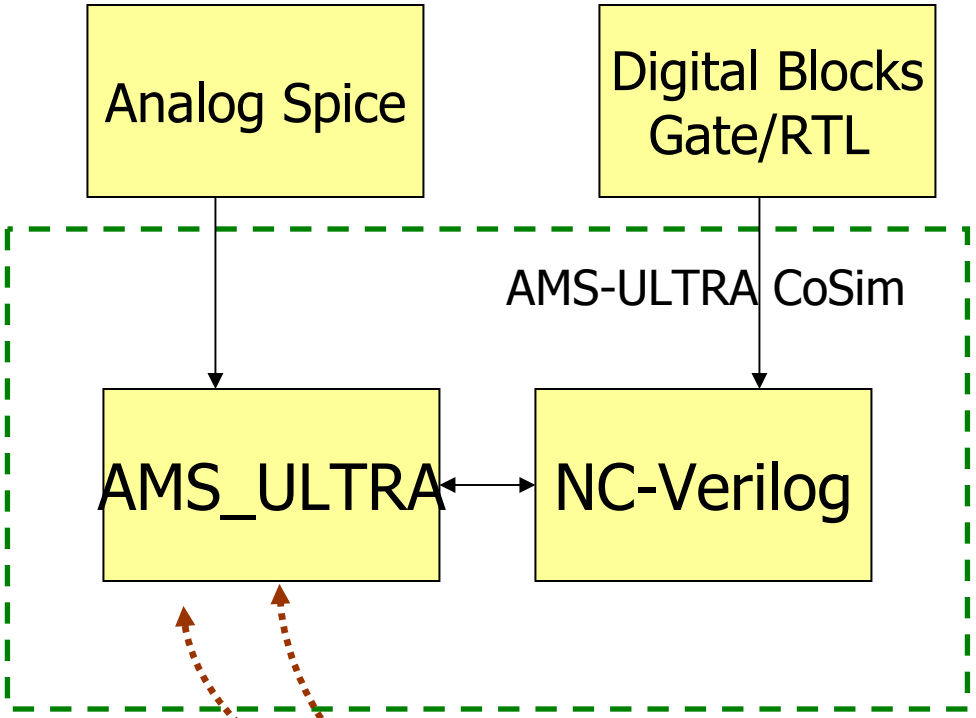


Mixed Design verification

Analog Verification`

Digital Verification

AMS-ULTRA Co-sim



prop.cfg File

```
cell arlsph512x8
{
string prop sourcefile=
"arlsph512x8.sp";
string prop sourcefile_opts="
-auto_bus -bus_delim _
-case_map keep
-in_port ADR
-in_port CLK
-in_port ME";
}
```

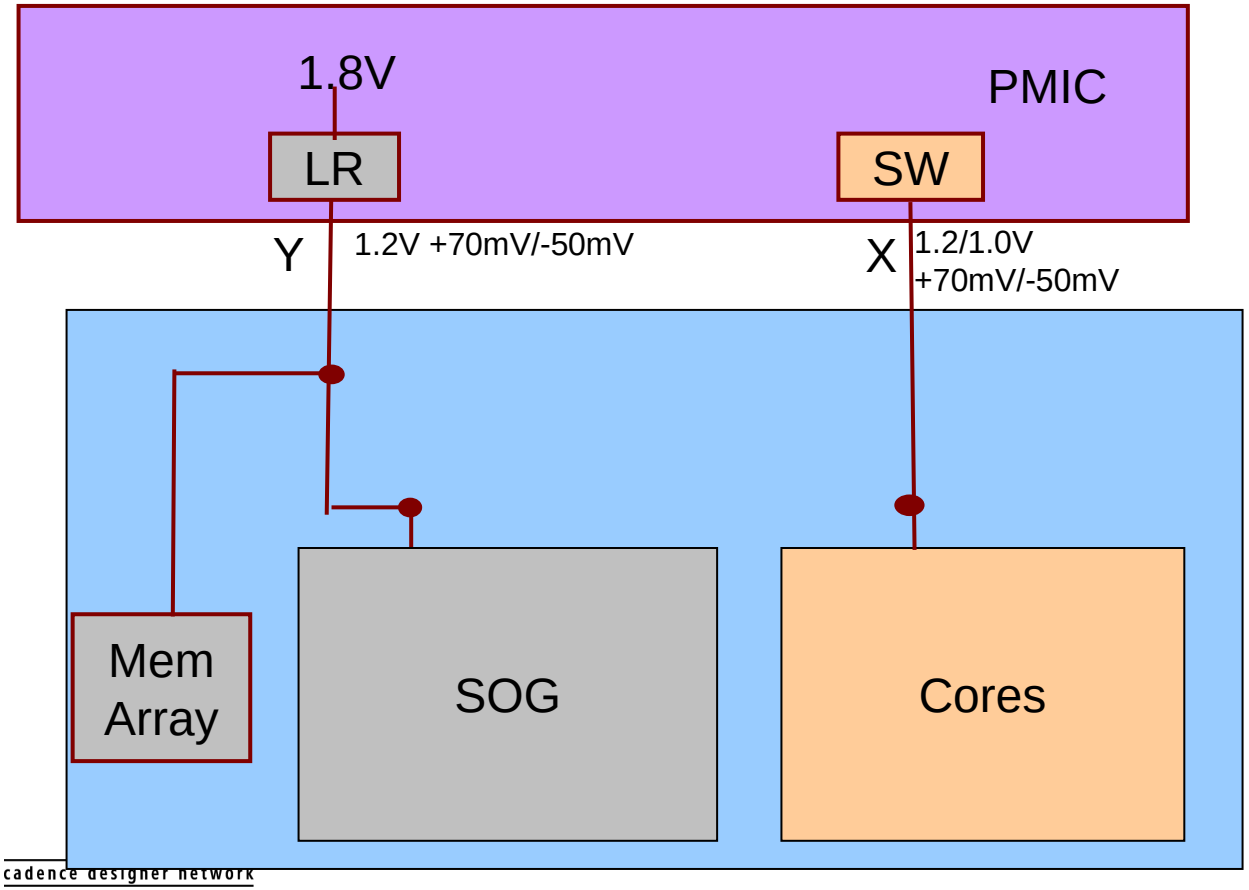
Objective of AMS-Ultra Flow

- **Multi-voltage domain on SoC**
- **Power Gating**
  - **SRPG (State Retention Power Gating)**
  - **Partial SRPG**
- **Dynamic Voltage and Frequency Scaling**

Objective of AMS-Ultra Flow

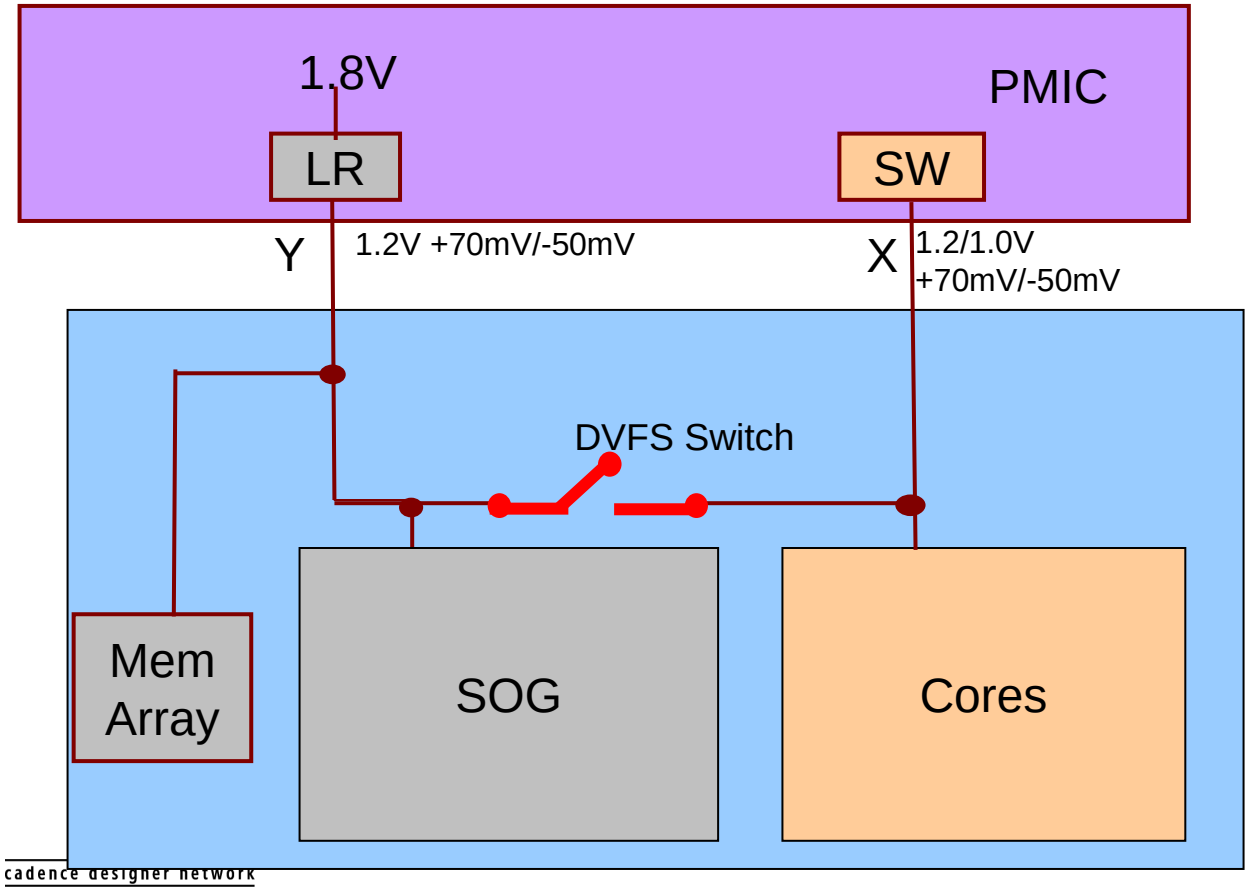
- Power-On Sequence Verification because of multiple Voltage Regulator
- Power-On-Reset Verification
- Proper Clock Sequence from Clock Generator Module and proper first instruction fetch by CORE
- Timing and Functionality closure between analog and digital signal interfaces
- Memory Verification, ROM

Multi-Voltage Domain On SoC



Issue
Timing Closure across
Voltage Island
due to voltage regulator uncertainty

Multi-Voltage Domain On SoC



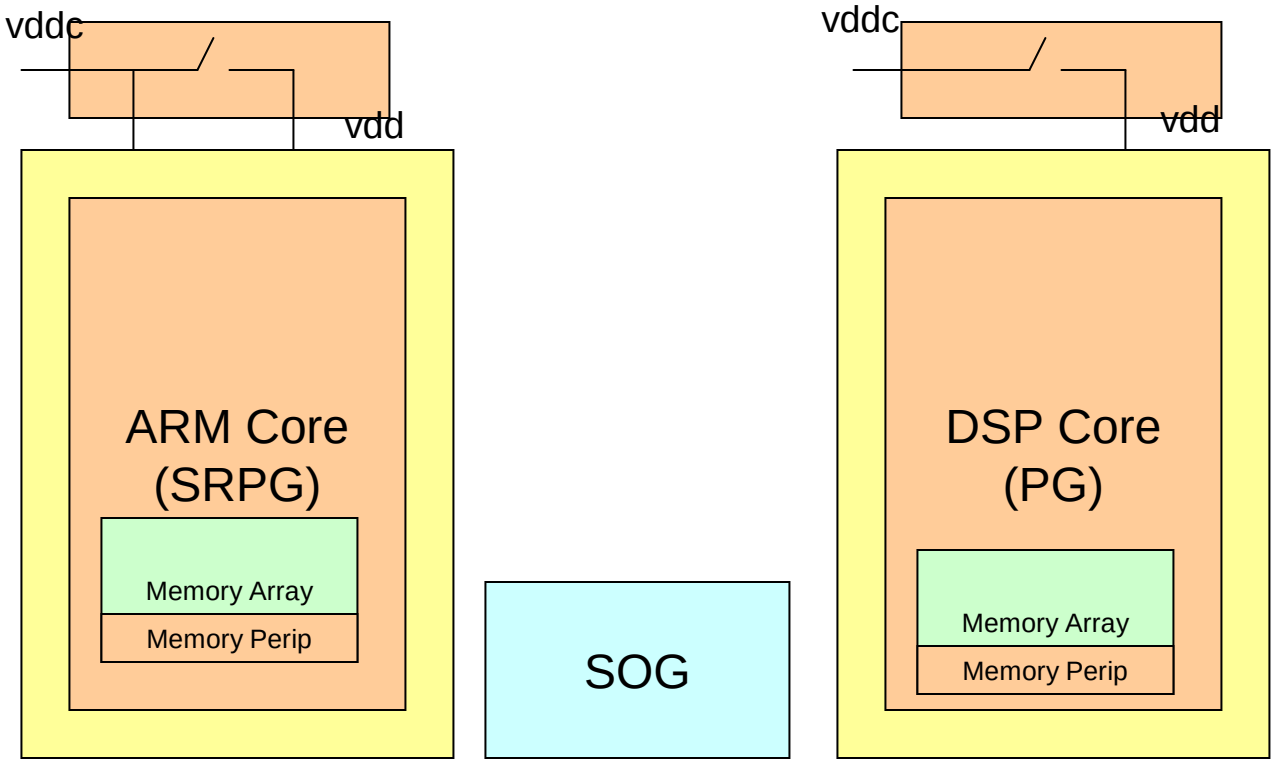
- Estimation of number of DVFS switches
- IR drop analysis across DVFS switch
- Substrate connectivity of the DVFS switches.

Multi-Voltage domain on SOC .. contd

How to Estimate Number of Switches:

- Current drawn wavefrom for SOG and COREs calculated from the PowerTheater feedback to DVFS switch spice as current sync for the estimation of the DVFS switches.
- Distributed value of Resistance, for the SOG and CORE Power Grid was used for the estimation of the IR drop across DVFS switches.

Power Gating



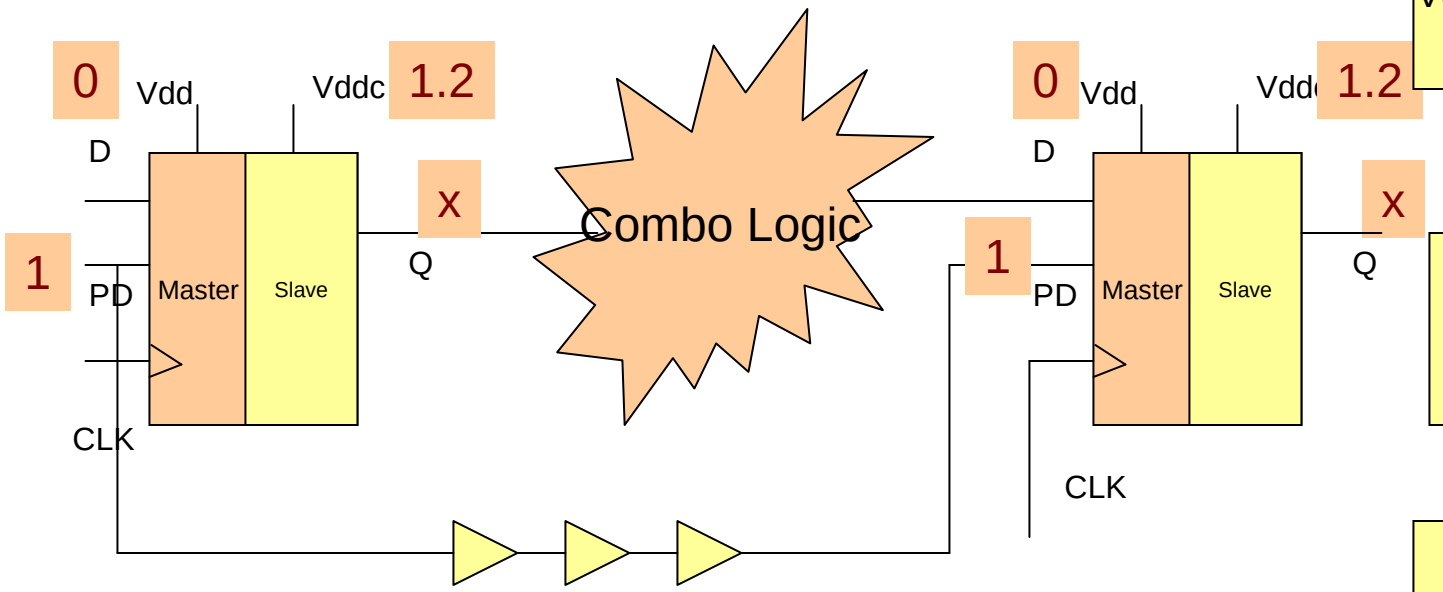
- Verifying Power Gating
- Verifying SRPG
- Verifying Memory Periphery Power Gating
- Number of Power gating switches & associated control logic
- IR Drop across switch

Logic on Gated Supply vdd

Logic on Continuous Supply vddc

Isolation Cell & Level shifter on Continuous Supply

SRPG



Issue1:
Verilog Verification does not have power information

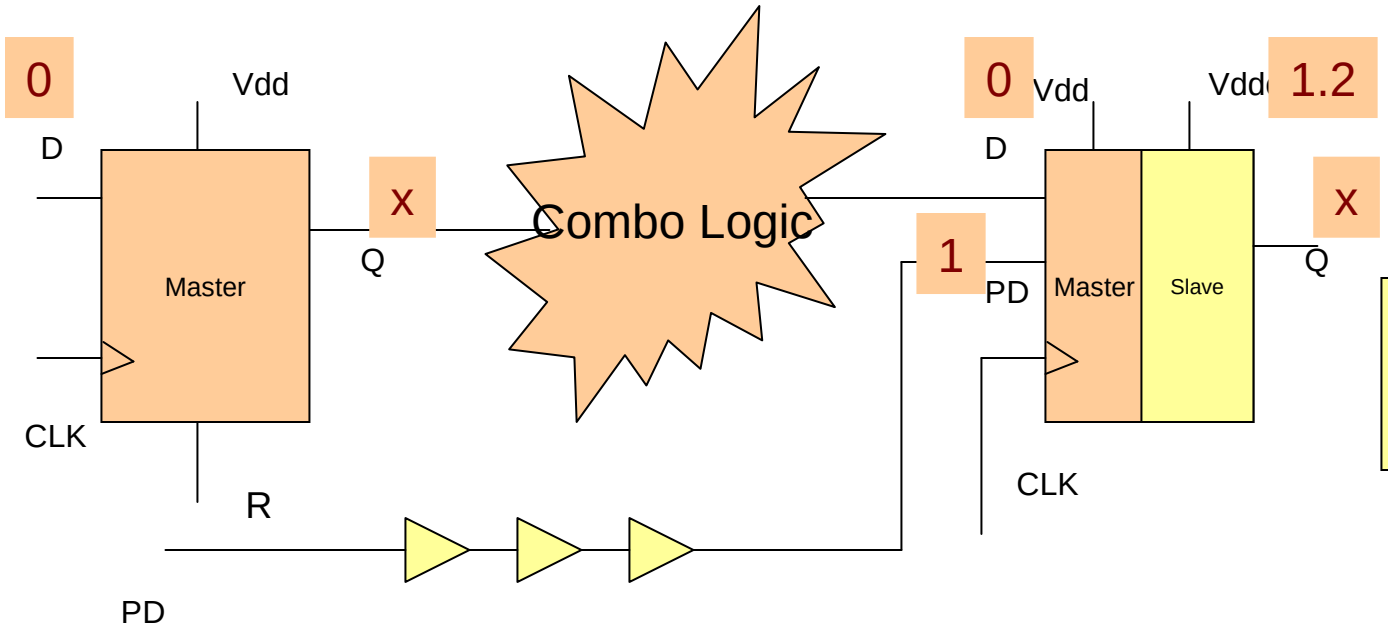
Issue2:
Power down, Power up Sequence verification

Issue3:
Proper SRPG functioning

Logic on Gated Supply vdd

Logic on Continuous Supply vddc

Partial SRPG



Issue1:
Which Flops are to be SRPG?

Issue2:
Is NON SRPG flop getting reset After Power up?

Logic on Gated Supply vdd

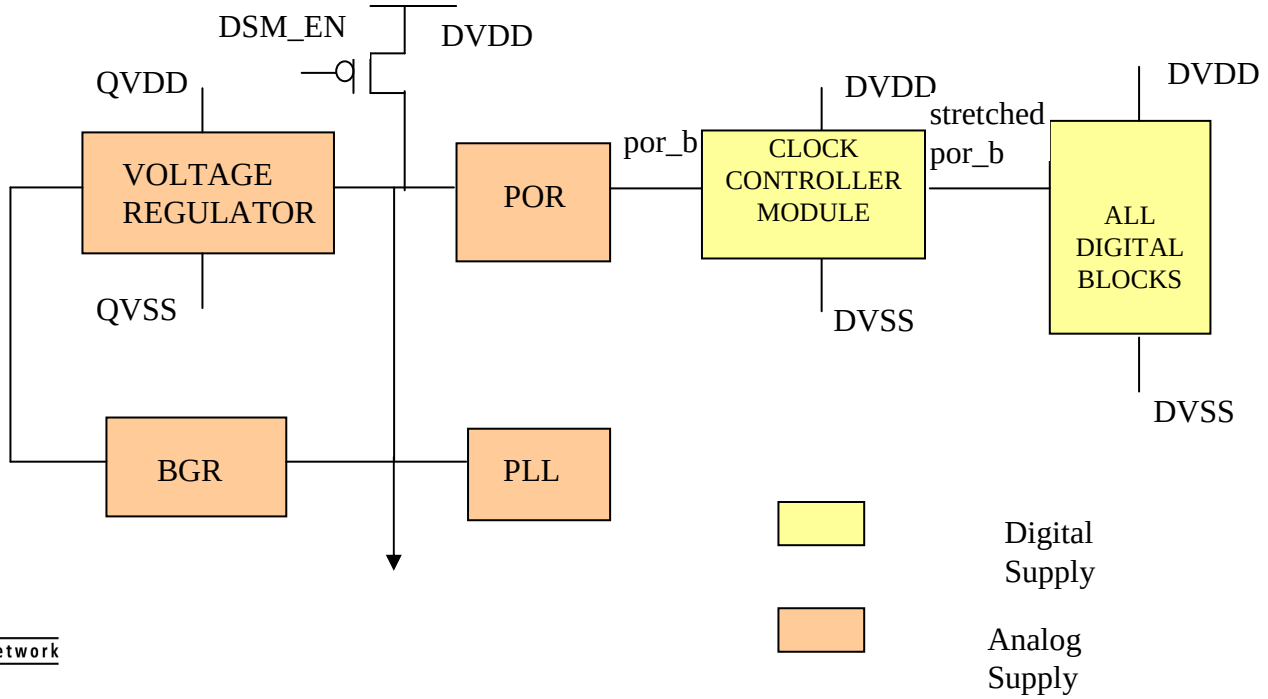
Logic on Continuous Supply vddc

Power Gating Verification

- Spice model for all the SPRG flops and always on cells have been taken in the AMS-Ultra flow.
- Verilog behavioral model was used for remaining logic.
- SOC level testbench was used.
- Stimulus was applied to verify power down and power up the block.

Dynamic voltage/frequency scaling

- **Challenge**
  - Verify Deep Sleep Mode for Proper Frequency of clock and also check respective clocks are stopped



Power up Sequence of chip

- **Challenge**
  - Multiple Power Domains
    - Digital Voltage Level: 0.9 - 1.2v
    - Analog Voltage Level: 1.875 - 2.75v
  - Proper Power up Sequence of Chip

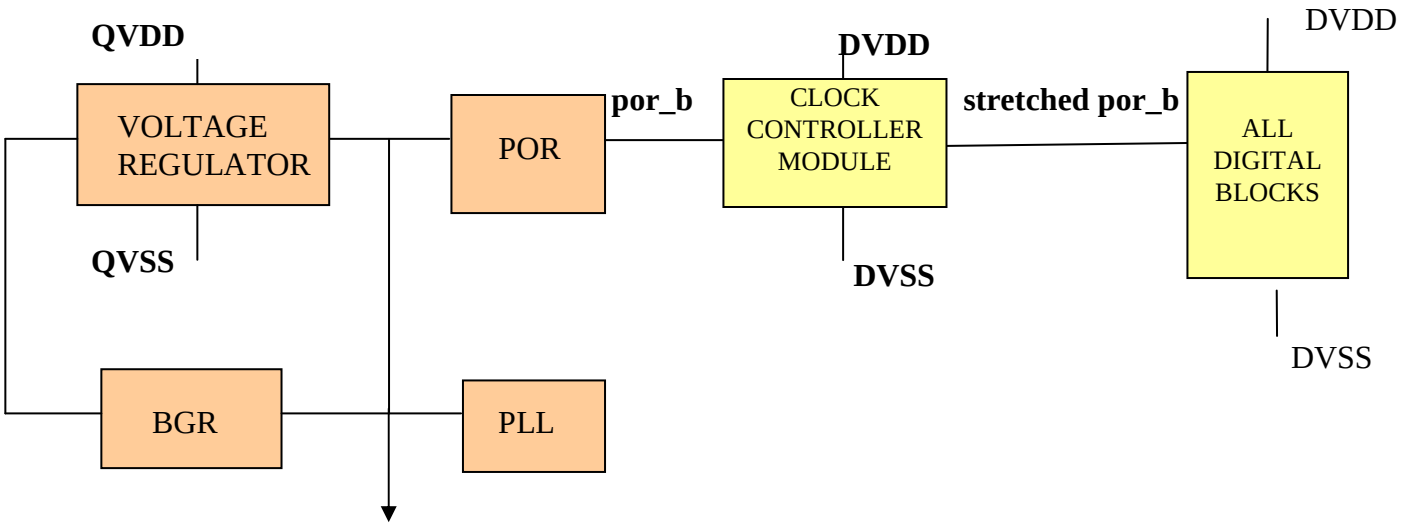
- **Blocks**
  - Analog : Voltage Regulator, Band Gap, Power-On-Reset, Level Shifters
  - Digital : Rest of the chip

Power On Reset sequence

- **Challenge**
  - Proper Power on Reset Generation due to involvement of Digital and Analog Blocks
  - Verify functionality of POR module after Power On Reset generation
  - Reset Stretch logic

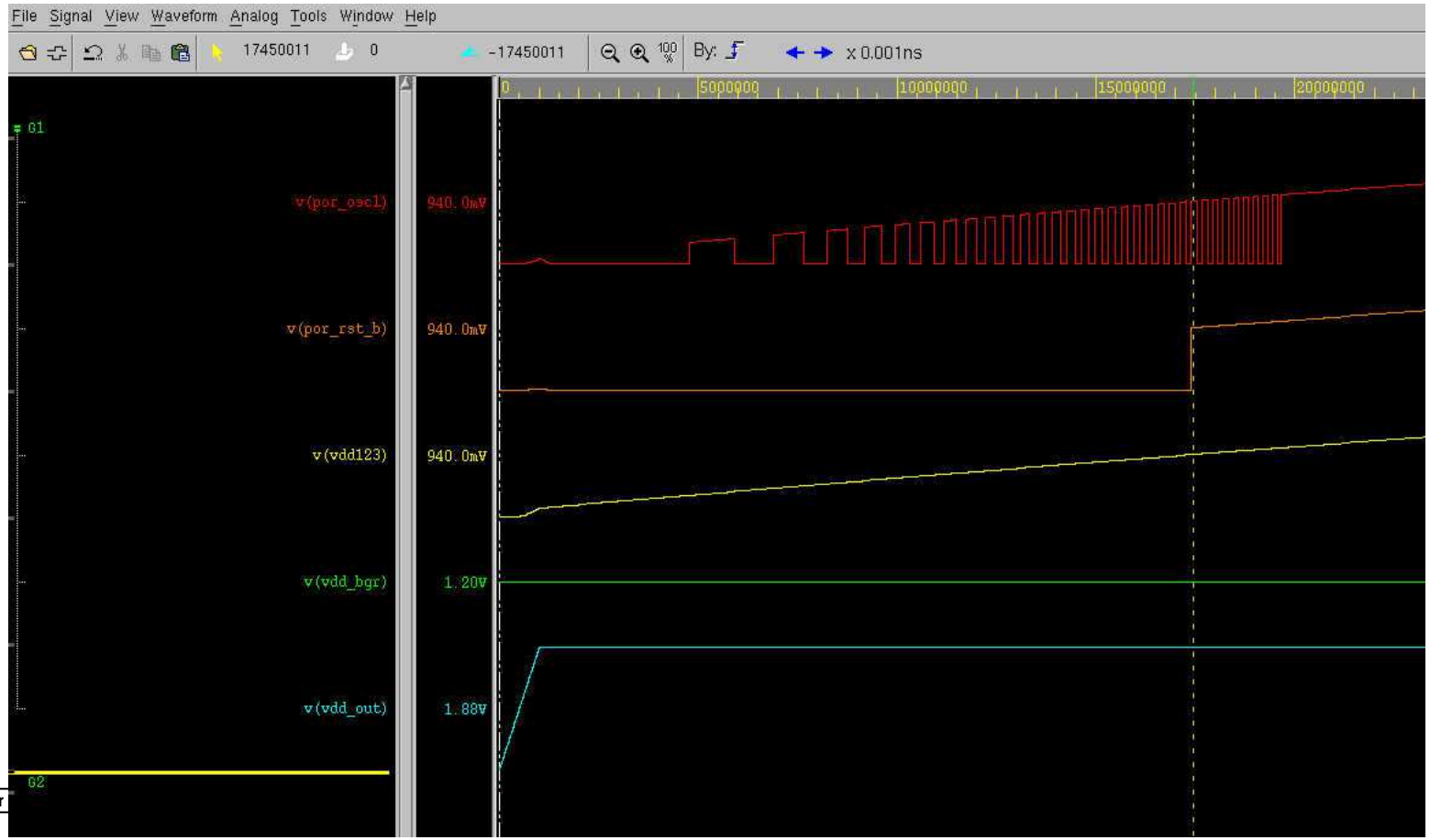
- **Blocks**
  - Analog : Voltage Regulator, Band Gap, Power-On-Reset, Level Shifters
  - Digital: Rest of the chip

Power On Reset sequence… Contd



Results

Power On Reset sequence



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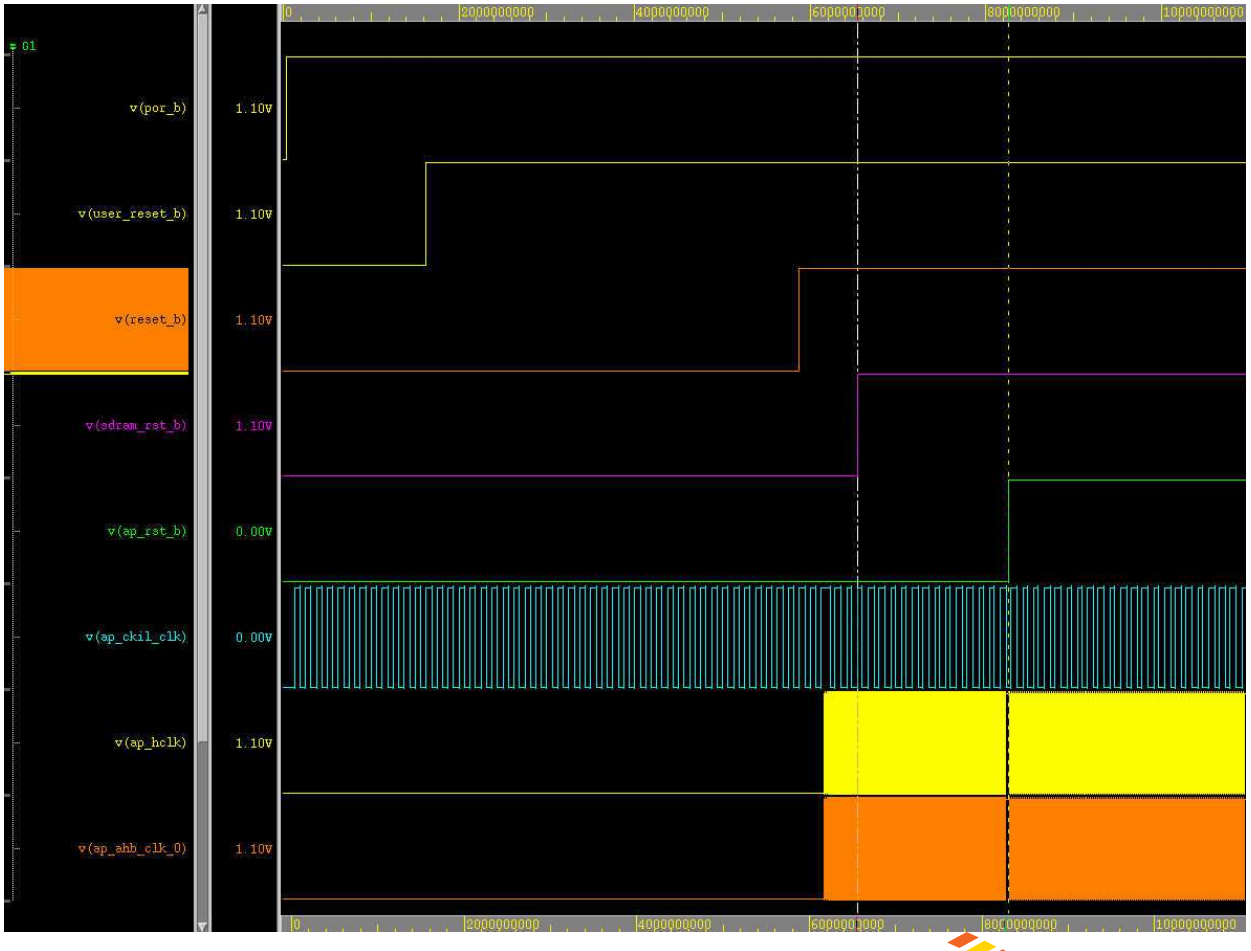
Clock Sequence from Clock Generator Module and proper first instruction fetch by CORES

- **Challenge**
  - Non Resetable flops causing X in Nc-verilog Simulation
  - Clocks getting X
- **Blocks**
  - Digital Spice Blocks : Clock Controller Blocks
  - Digital Extracted Gate Level Netlist : Full SOC Chip

Results

Proper Clock Sequence from Clock Generator Module

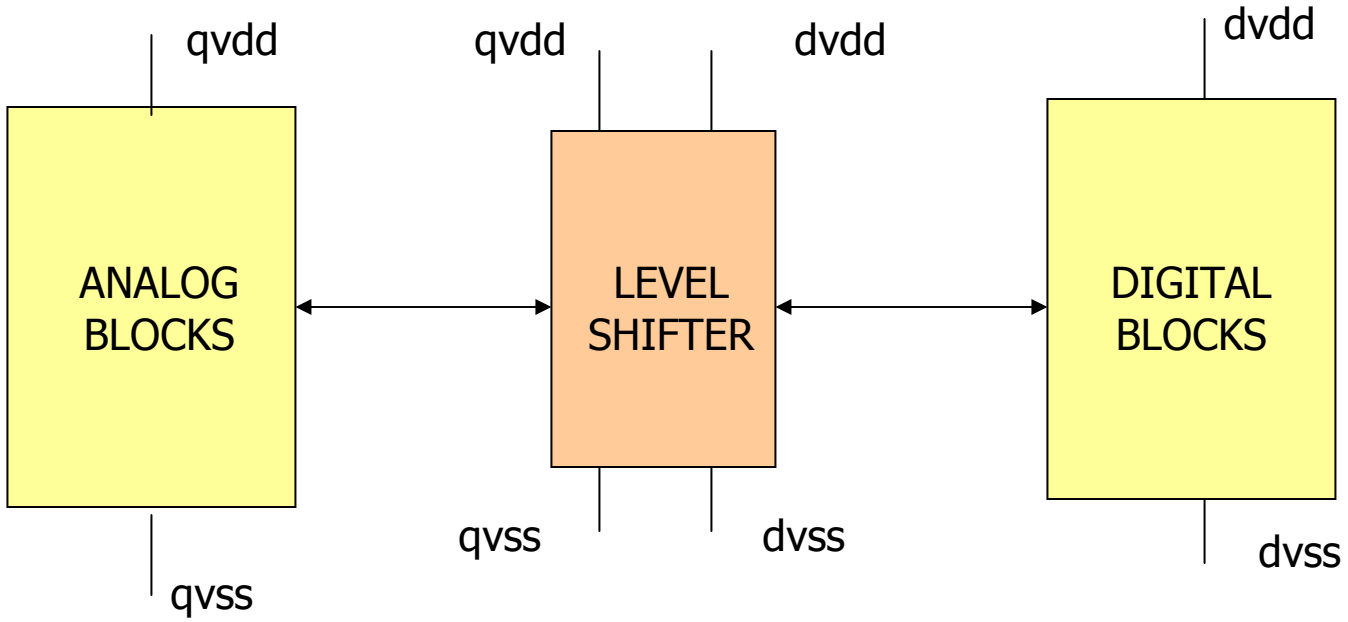


Timing and Functionality Closure between analog and digital signal interfaces

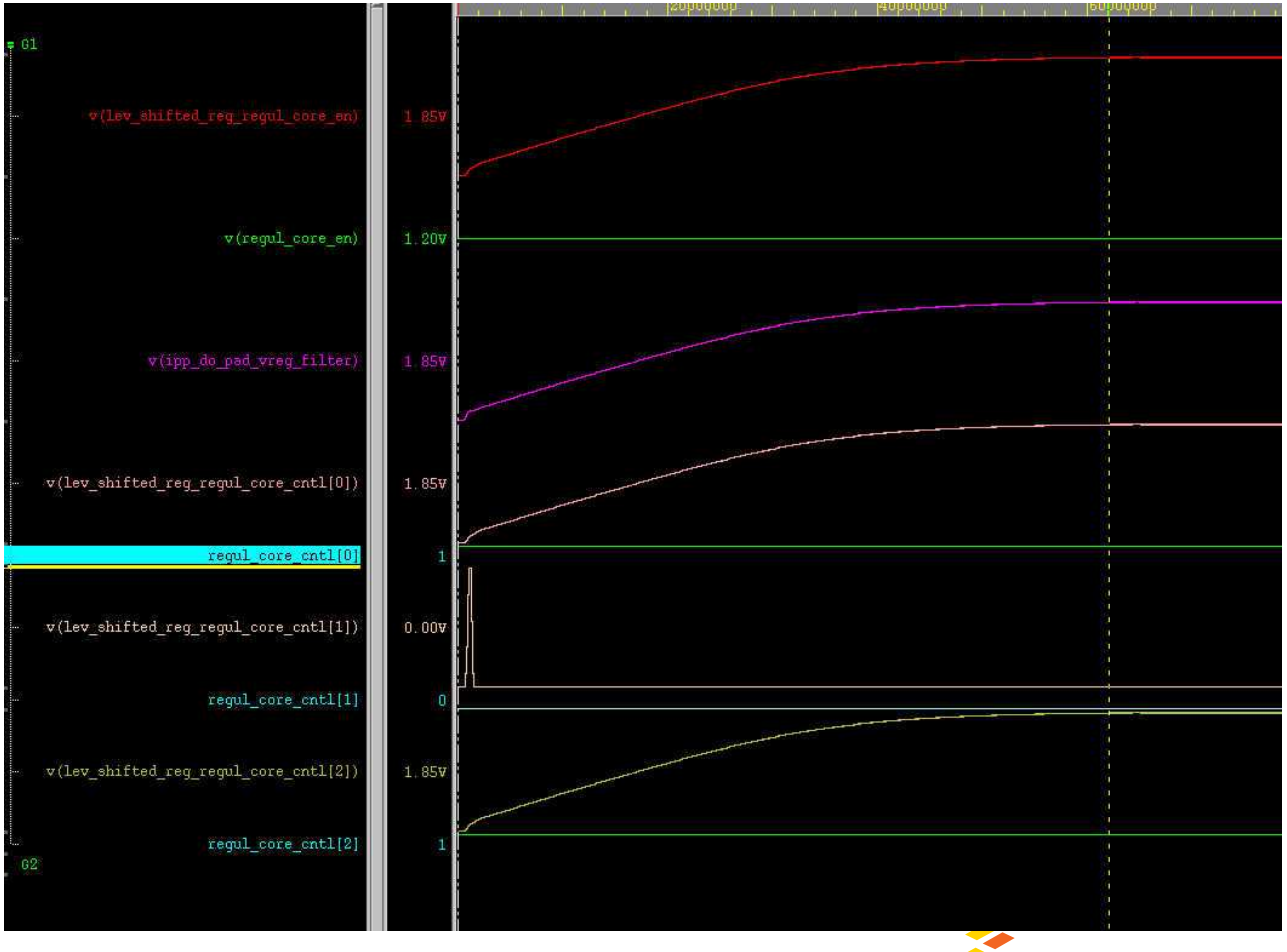
- **Challenge**
  - Verify Proper Voltage levels and timing for interface signals from Digital to Analog
  - Verify Proper Voltage levels and timing for interface signals from Analog to Digital

- **Blocks**
  - Analog Blocks : POR, BGR, Regul Core, PLL, DFD, CAMP, CMON, Level Shifters
  - Digital Blocks : Full SOC Chip

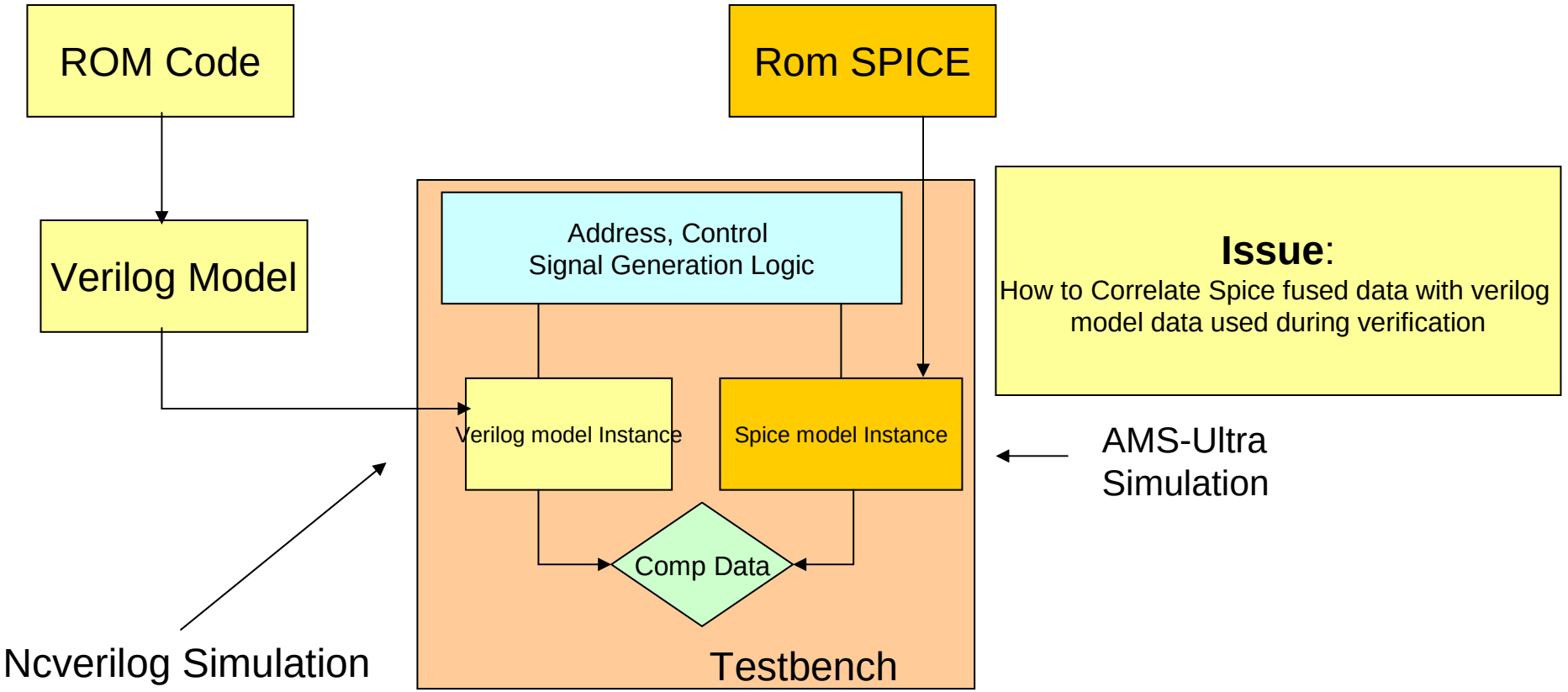
Level shifting from digital to analog



Timing and Functionality closure between analog and digital signal interfaces



Memory Verification, ROM



Methods adopted to speed-up simulation

- Use usim_vr option was used to simulate power switches to reduce partitioning nodes
- Use .usim_da|df and speed=6|7 for appropriate speed and accuracy depending upon the testcase
- Limit number of saved signals e.g. probe v(*) depth=2
- Use '-disres none' to disable discipline resolution
- Declaring in_port and out_port for spice ports in prop.cfg file to limit bidir CMs

Design flaws detected with AMS-Ultra

- Floating nodes inside memories were detected.
- IR drop through the DVFS switch was not meeting 5mV specs.
- On some of the interfacing signals, level shifter was not there which gave improper results
- Voltage regulator output not ramping up because of issues in start-up circuit of band gap reference
- Power On Reset signal not ramping up because of voltage regulator output not ramping

Bugs Reported in AMS-Ultra

Description of Issue	PCR / SR number
Wrong port name generated when >1 bus delimiter	PCR-922720
System virtual memory limit exceeded.	PCR-922736
Verilog+SPICE: Fix strict AMSIPC err for -disres none	PCR925239
Elaboration fails due to gwm_xcleanup internal error	PCR925211
Digital nets connected to IE should remain expanded	PCR925536
AMSVF 64Bit Support.	SR40427716 PCR927825

Bugs Reported in AMS-Ultra

Description of Issue	PCR / SR number
Setup ncverilog flow instead of 3 steps approach.	SR: 40345720
Power calculation on Spice block for VDD net.	SR: 40352404
AMSUltra_vf doesn't allow reg to spice connection	SR: 40352416 PCR: 915798
ncelab internal error: cu_get_ots_entry ()	SR: 40352416 PCR: 915820
Different timescale precision results in different result	PCR-919556
Implicit parameter pass issue in AMSVF	PCR-921106
Support wildcard for in_port out_port in sourcefile_opts	PCR925079

Enhancements required in AMS-Ultra

- Dynamically Switching Between Spice and verilog behavior model or c model
- CFG file requires in, out port information, Tool should take verilog and extract the in, out, inout information
- Intermediate Database creation, so as to start simulation from the saved database.
- Simplified testcase creation for sending database to Cadence for debugging
- Support for $monitor to access spice signals
- Improve messaging while tool crash with an 'internal error'
- OOMR into spice

Conclusion

- **AMS-Ultra provide good solution for mixed signal verification and SRPG verification, but for big design SRPG verification is not possible because of number of interconnect modules.**

- **Simulation run time is fast for timing but inaccurate for power estimation.**

Acknowledgement

Thanks to Irshad, Ram Kumar, Prabal, Vincent for helping us on the AMS-Ultra Flow

Thank You
Q&A .....