IBM System z

IBM z-Series Microprocessor and Cache Subsystem Chips Use CSR to Drive Multi-Gigahertz Design Point

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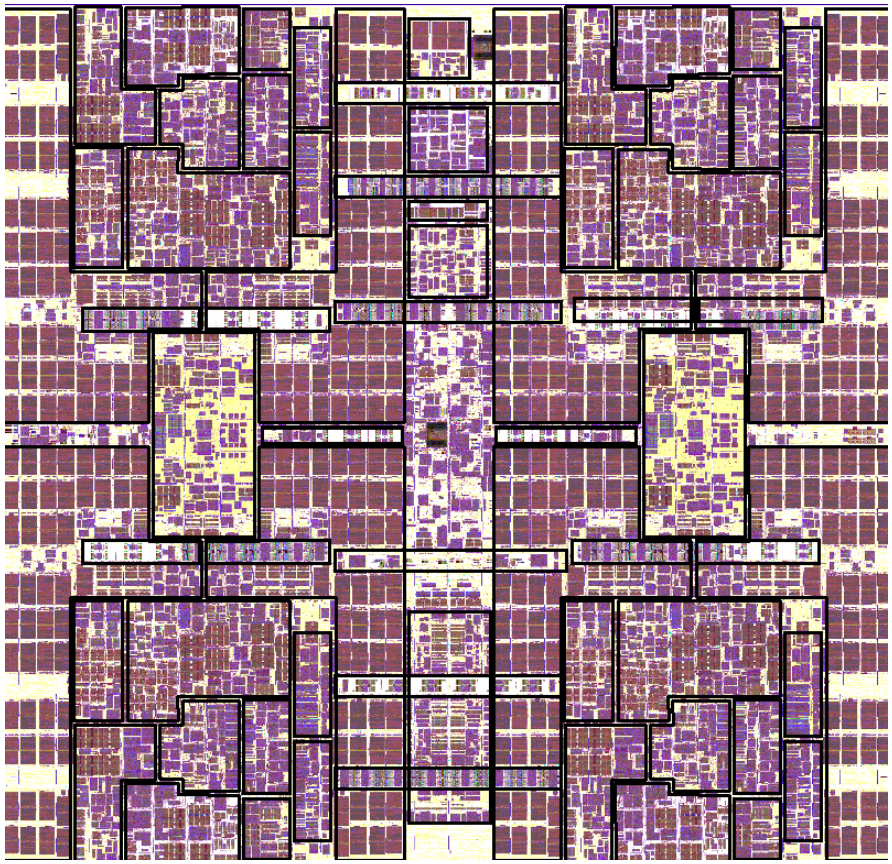
IBM Systems

IBM z6 Processor Chip

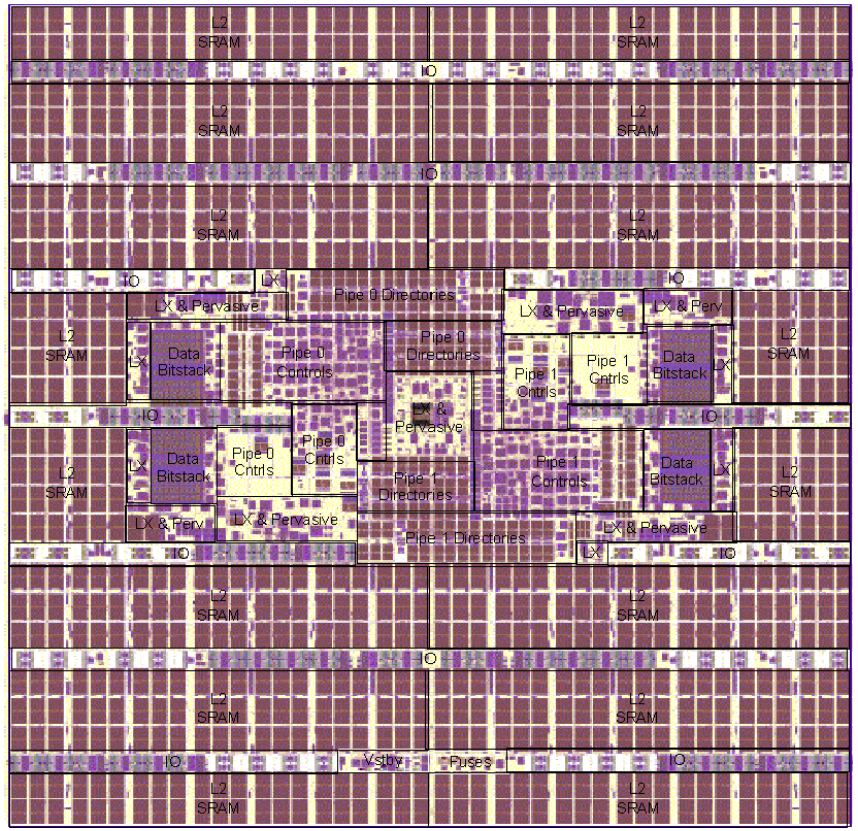
- **New high-frequency z/Architecture microprocessor core**
  - –4+ GHz operation in system
- **4 cores pre die**
- **3MB of 2nd level cache per core**
- **4 levels of concurrent hierarchy**
- **2 Coprocessor engines for Cryptography and Data Compression**
- **System interfaces**
  - –EI3 Technology at up to 3GHz bus speeds
  - –2 x 48 GB/s SMP Hub
  - –4 x 13 GB/s Memory
  - –2 x 17 GB/s IO



- **991M Transistors**
- **138 Mb SRAM**
- **6 km wire**
- **21.7mm x 20.0mm die (434 sq mm)**
- **1188 signal / 8765 total chip I/O's**

IBM z6 SMP Hub Chip

- **Connects multiple z6 Processor Chips**
  - –48 GB/sec bandwidth per processor
- **Shared 3rd Level Cache**
  - –24 MB SRAM Cache per SMP Hub Chip
  - –Hub chips can be paired for 48MB shared cache
- **Also 4 levels of concurrent hierarchy**



- **1.6B Transistors**
- **242 Mb SRAM**
- **3 km wire**
- **20.8mm x 21.4mm die (445 sq mm)**
- **2419 signal / 7984 total chip I/O's**

Why Cadence Space-Based Router?

- **Next generation routing program**
- Capabilities we couldn't get anywhere else
- Improved runtime and designer turnaround time
- Very tight coupling into router development team
- Still untapped potential…

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- **Capabilities we couldn't get anywhere else**
  - **Sign-off quality checking engine**
  - **More constraints and at a much finer granularity to control the router**
  - **Cadence Chip Optimizer**
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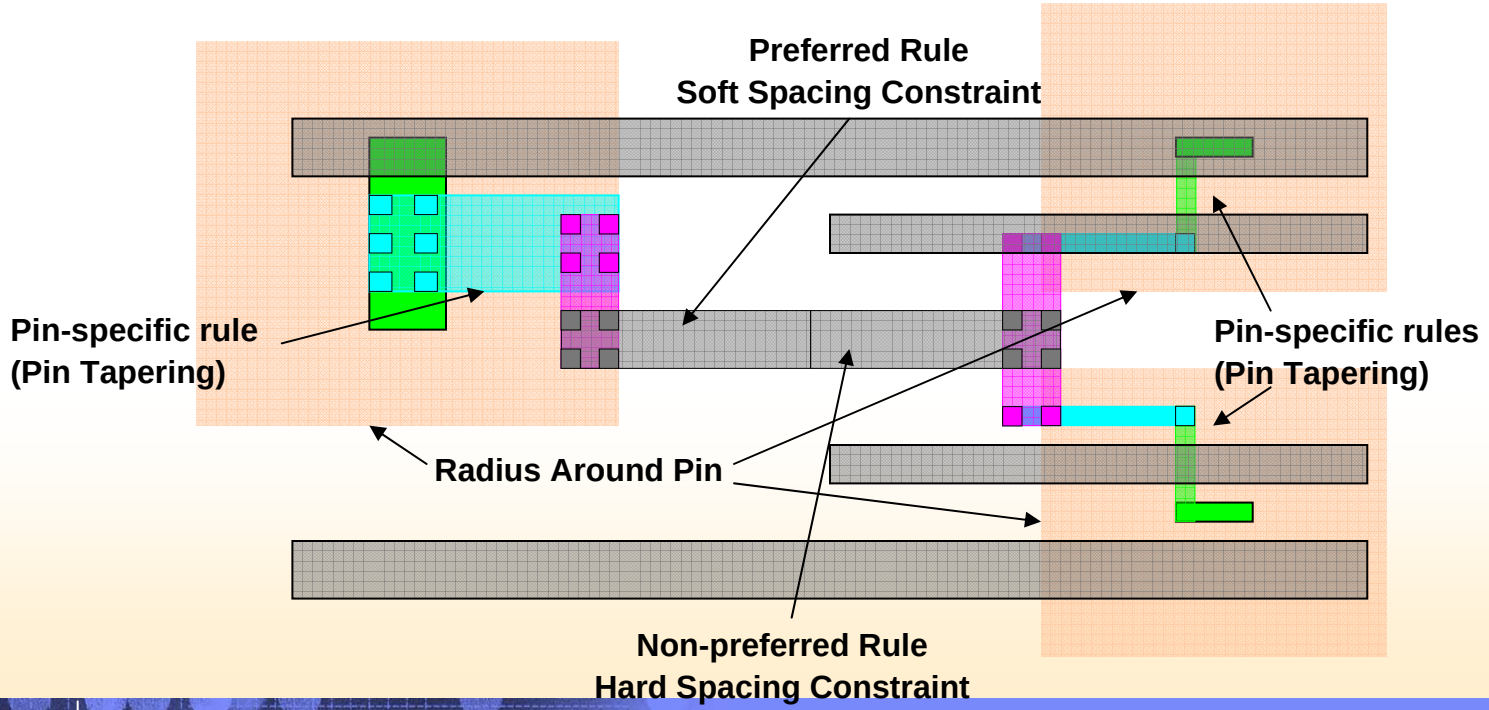
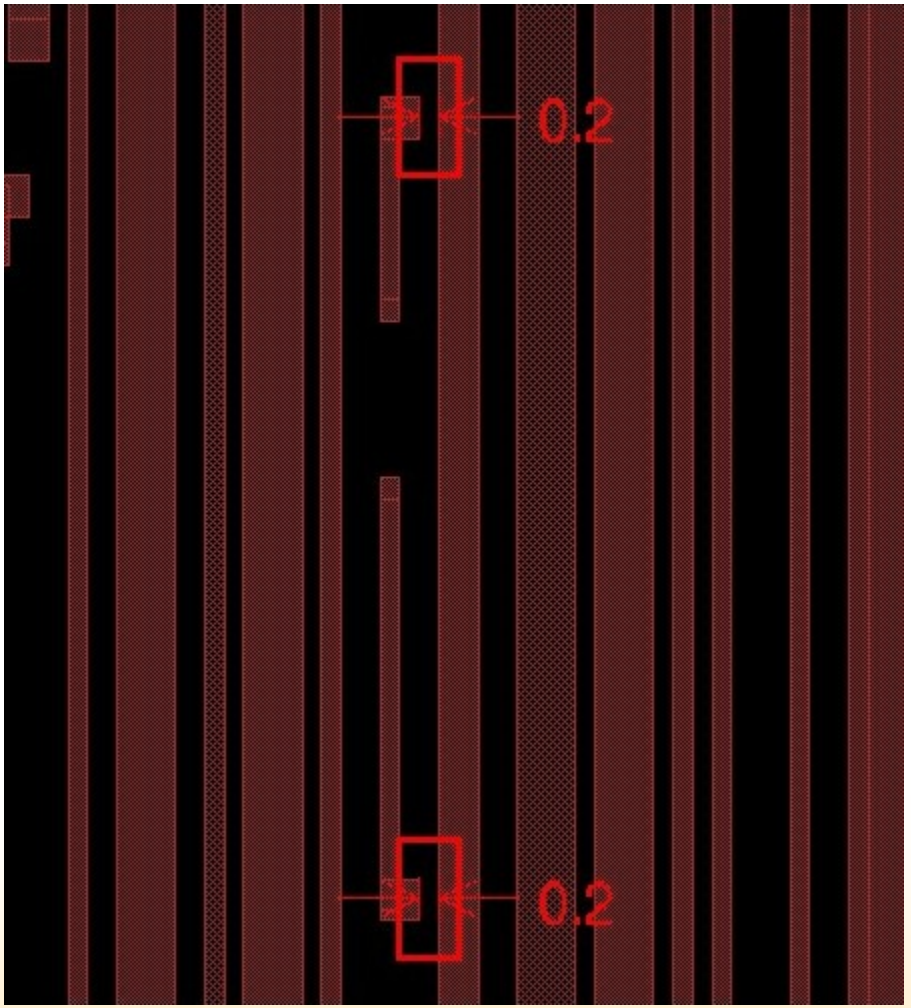
Example of High-Performance Routing

- **Objectives / Goals**
  - –Engineer critical nets (i.e., for performance, power) using constraints
  - –Eliminate / minimize the need for “pre-routing”
  - –Minimize wire delay, due to “scenic”, off “use-layer” routing

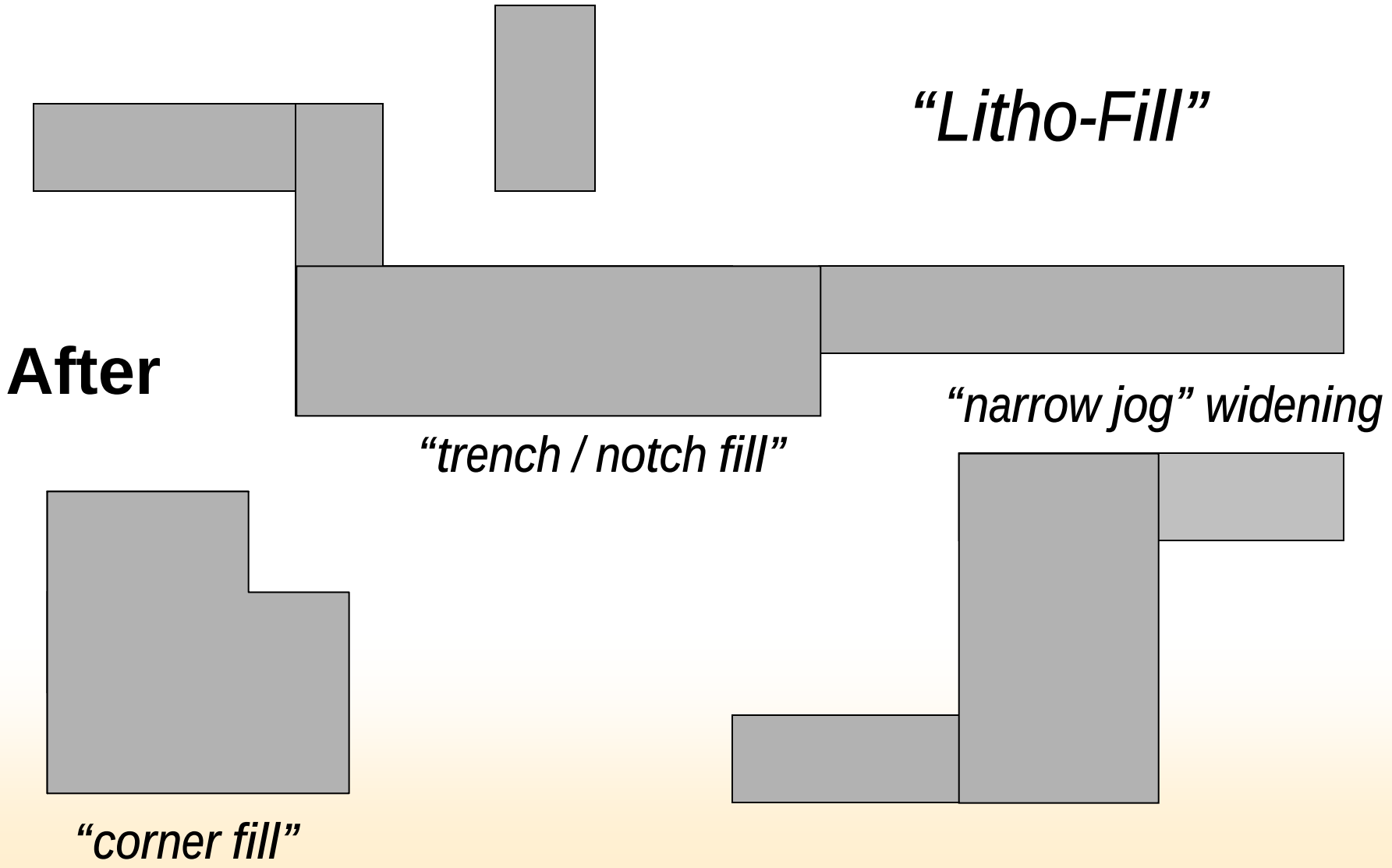


Preferred Spacing Constraint

- **Ability for router to “cheat” on greater than minimum spacing rules on a costed basis.**
- **Revolutionary difference in QOR, runtime and number of preroutes necessary.**
  - –4.1x runtime improvement
  - –10x less violations
  - –1.6x better use-layer usage



Cadence Chip Optimizer

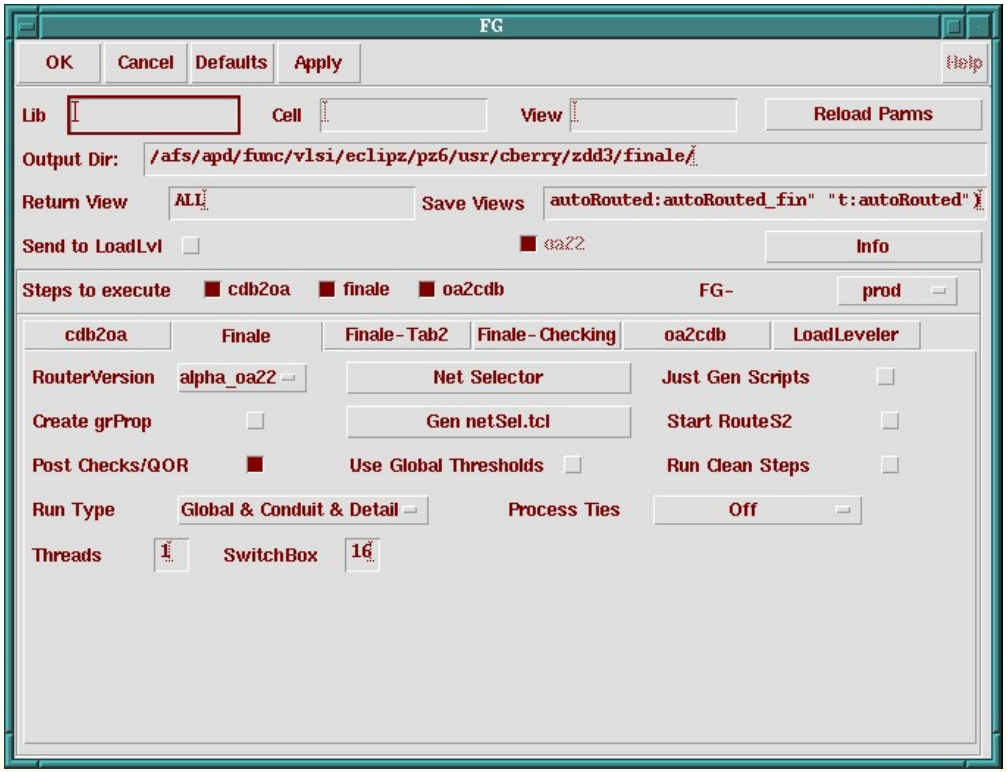


Why Cadence Space-Based Router?

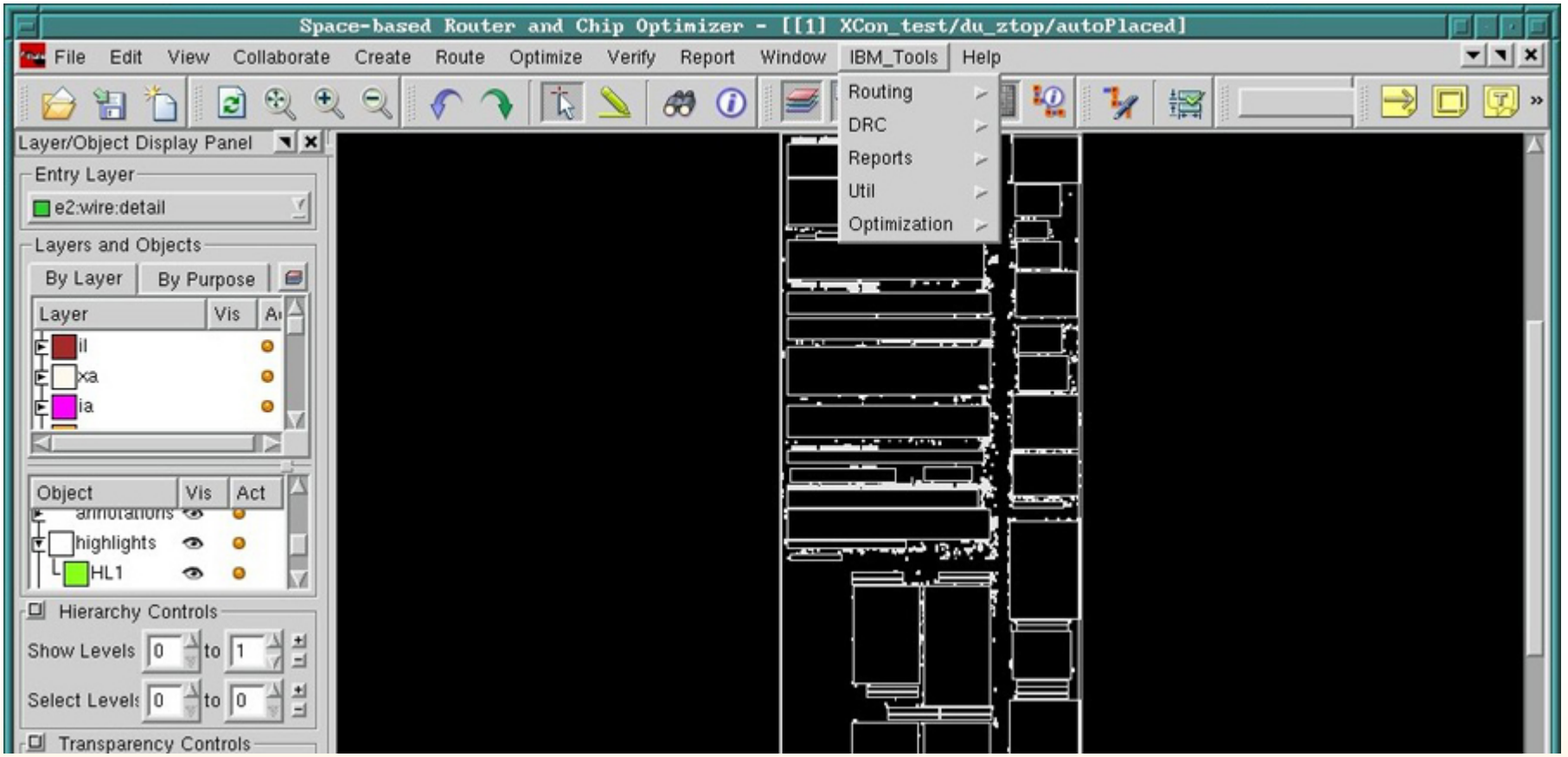
- Next generation routing program
- Capabilities we couldn't get anywhere else
- **Improved runtime and designer productivity**
  - **Runtime better than previous generation routing technology on all of our designs**
  - **Multi-threading improved that even further**
  - **Our own skill and tcl to help designers take advantage of the new capabilities**
- Very tight coupling into router development team
- Still untapped potential…

Skill and tcl wrappers

- **Absolutely necessary to make the adoption of a new tool go as smoothly as possible**
- **Lots of new functionality and we wanted the average designer to be able to take advantage of the important aspects**



Tcl wrappers continued…



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- **Still untapped potential…**
  - **Extend from integration to circuits domain**
  - **Power routing, Clock routing, and Litho-aware routing**
  - **Nearly limitless optimization capability to improve manufacturability**

In Conclusion

- **State of the Art technology.**
- **Very pleased with results on IBM z6 project.**
- **Lots of room to grow.**

Acknowledgements

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Thank You!

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