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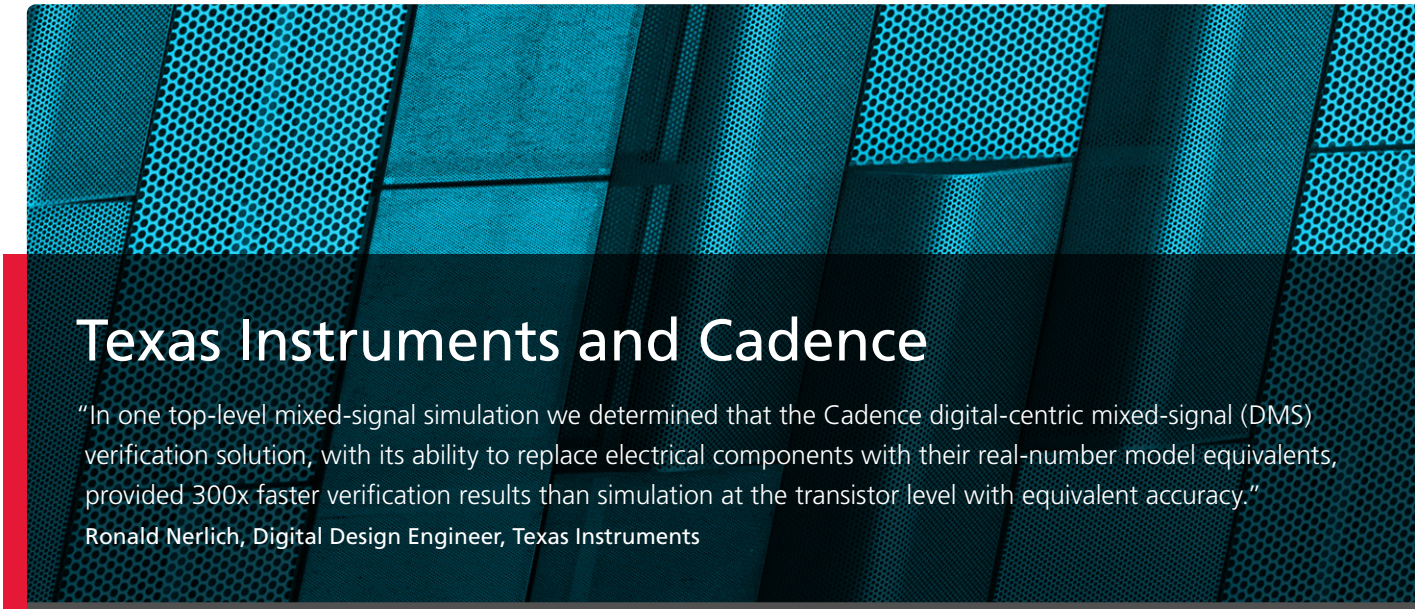

Texas Instruments and Cadence

"In one top-level mixed-signal simulation we determined that the Cadence digital-centric mixed-signal (DMS) verification solution, with its ability to replace electrical components with their real-number model equivalents, provided 300x faster verification results than simulation at the transistor level with equivalent accuracy."

Ronald Nerlich, Digital Design Engineer, Texas Instruments

The Customer

Texas Instruments (TI) semiconductor innovations help 90,000 customers unlock the possibilities of the world as it could be—smarter, safer, greener, healthier, and more fun. The company's commitment to building a better future is ingrained in everything it does—from the responsible manufacturing of its semiconductors, to caring for its employees, to giving back to its communities.

The Challenge

The TI MSP430 is a well-known microcontroller used in many applications. Its newest generation operates in ultra low-power (<0.5uA RTC) mode but maintains well-known features like ease-of-use and integrated analog components like analog-to-digital (A-to-D) and digital-to-analog (D-to-A) converters. This creates a system on chip (SoC) that can be sold in high-volume markets.

These specifications create critical design constraints during the mixed-signal design process. Analog and digital components interact closely; each component might have different power states; and verification coverage must be high to ensure quality.

"Because of our high-performance targets and complex modeling requirements, we couldn't separate the design into analog and digital buckets," says Tobias Leisgang, MSP430 Digital IP Supervisor at TI. "We needed to adopt a digital-centric, metric-driven verification methodology into our mixed-signal verification flow, and we needed a high level of reliability. Top-level SoC verification was critical—functional failures could lead to costly design iterations and a missed market window."

TI's digital design team had adopted the Cadence® metric-driven verification methodology years ago using Incisive® Enterprise Specman Elite® Testbench (for randomized testing) and Incisive Enterprise Manager (to measure coverage).

Business Challenges

- Short time-to-market window for complex mixed-signal design verification

Design Challenges

- High-performance, ultra low-power features in close interaction with core analog functional blocks at the SoC level
- High-volume product
- Functional failures would lead to costly design iterations

Cadence Solutions

- Digital-centric mixed-signal verification flow
- Incisive Enterprise Simulator Digital/Mixed-Signal (DMS) Option
- Incisive Enterprise Specman Elite Testbench
- Incisive Enterprise Manager
- Virtuoso AMS Designer with flexible analog simulation
- Virtuoso Accelerated Parallel Simulator
- Customer Support

Results

- 300x faster verification vs. mixed-signal simulation at the transistor level
- Improved time to market and product quality with mixed-signal regression runs
- Fewer re-spins with high-performance, real-number modeling and top-level, metric-driven mixed-signal SoC verification
- Earlier detection and correction of errors
- 10x cycle-time improvement in mixed-signal verification

However, classic mixed-signal simulation had performance limitations and modeling the analog components in pure-digital Verilog couldn't provide the accuracy.

The Solution

Cadence proposed that TI use the Digital/Mixed-Signal (DMS) Option and extend the successful metric-driven verification (MDV) methodology into the analog and mixed-signal domains. An extra DMS verification layer was added to the analog transistor-level/mixed-signal and pure-digital components. The analog components were up-abstracted to real-value models (wreal models in Verilog-AMS). A truly real-valued net/wire, called "wreal," represents a real-valued physical connection between structural entities. The value range is continuous and real, thus an ideal representation for analog voltages or current. And because a real/wreal value is time-discrete, it allows the digital engine to completely solve the wreal model description, which significantly increases simulation performance (up to several 1,000x over transistor-level simulation). This provides the speed-up required for a randomized testing methodology.

TI covered the ultra low-power requirements by using the Common Power Format (CPF) in the digital domain. This made it possible to effectively describe different power states and transitions. The effect of the power sequence on the analog portion and the A-to-D/D-to-A interactions was significant and required consideration in the context of an automated verification setup. Again, using MDV with wreal models provided a solution. The random-stimulus generation and coverage collection generated various power-state transitions, while the wreal models provided the accuracy to mimic the analog behavior and the simulation performance required for an effective setup.

"Thanks to our new DMS flow, mixed-signal verification has moved out of the critical path for the first time."

For the DMS methodology to be effective, it was important to replace all analog components with wreal models to eliminate the use of the analog solver during mixed-signal simulation. This was a significant modeling effort for the team that took several weeks. The use of the wreal modeling style in Verilog-AMS made it easy for the analog designers and digital verification engineers to model the blocks—traditional Verilog language was commonly known and the wreal enhancements were easy to adopt.

"We required real-number modeling of analog building blocks supported by Incisive Enterprise Simulator DMS Option and Cadence Virtuoso® AMS Designer, and the ability to verify interactions as opposed to just connectivity between analog blocks," says Roland Nerlich, Digital Design Engineer at TI. "We were able to perform pseudo-random regression runs for analog coverage, achieve runtime performance of the digital simulations, and easily transition from AMS-based simulation."

"Now we can simulate the complete analog path from the bondpad to the A-to-D converter," adds Thomas Fuchs, Mixed-Signal Design Engineer at TI. "This enables simulation scenarios that are much closer to real applications than we could achieve before."

Before the Cadence DMS solution, the engineers had to wait for all mandatory analog blocks to complete. They may have skipped a test and found the problem in the silicon, setting the project back by six months or more. Now the design team can start verification early, simulating an analog block with a real-number model. The impact on quality and cost is clear.

"In one top-level mixed signal simulation we determined that the Cadence DMS verification solution, with its ability to replace electrical components with their real-number model equivalents, provided 300x faster verification results than simulation at the transistor level with equivalent accuracy," Nerlich says.

The TI design team also relied on Cadence Support to help implement key functions. Close collaboration between TI and Cadence was a key factor in the project's success. "Whenever you use a new technology, there's a learning curve and some pipe cleaning is required," Nerlich says. "However, no problem remained unsolved for long. Cadence always came back with great support that we haven't seen from other vendors."

Summary and Future Plans

The Cadence DMS flow has led to measurable improvements in the TI design team's efficiency, quality, and time to market. Specman Elite Testbench accelerated time to market and greatly improved product quality. Its constrained-random testing took only 1 month—compared to 6–12 months of direct testing.

"We will continue to develop real-number models and leverage the new flow for future projects. We plan to use Virtuoso AMS Designer and Incisive Enterprise Simulator to further improve the development and reuse of real-number models."

"Cadence helped us streamline our verification environment. We successfully combined analog with digital verification and received the best of both worlds—and we received support for it all from one trusted vendor."

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Cadence is transforming the global electronics industry through a vision called EDA360. With an application-driven approach to design, our software, hardware, IP, and services help customers realize silicon, SoCs, and complete systems efficiently and profitably. www.cadence.com