

Interactive Short Locator: Establishing Efficiency and Predictability in the LVS Short Debug Process for Advanced SoC Designs

Debugging SoC designs grows more challenging as process technologies shrink. The time required to run multiple iterations of an entire SoC layout extraction renders that approach an increasingly impractical way to debug shorts. Interactive Short Locator technology in the Cadence® Physical Verification System provides an efficient debug solution that employs a dedicated analysis engine and interactive workflow to locate shorts quickly, easily, and consistently. In turn, the Interactive Short Locator reduces the number of layout extraction iterations while improving debug efficiency and overall productivity.

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Introduction

As nanometer process technologies shrink, the challenges expand for physical verification of advanced SoC designs. Design rules increase in both number and complexity, driving related increases in the size of the signoff rule deck and in the time required for debugging. Industry consensus holds that at the final signoff stage, designers spend approximately 80 percent of their time on the debug process. The impossibility of predicting the time needed to fix violations frequently leads to schedule delays and lost product revenue.

Shorts between different nets are the most common problem during the final tapeout, and fixing those shorts is one of the toughest challenges for layout extraction users. Here the solution lies in advanced physical verification tools that help designers quickly and easily identify and locate shorts. Such tools must be able to handle an increase in the quantity as well as the complexity of checks. And the tools must be effective enough to reduce the number of debug iterations and the total turnaround time, helping to ensure that schedules are met.

This technical paper discusses the Interactive Short Locator the unique debug technology found in the Cadence Physical Verification System and compares it to standard debug solutions available in the market. Two use cases of the Interactive Short Locator are also presented.

Approaches to Finding Shorts

With careful labeling of the layout, shorts can be identified during the layout extraction stage. However, the mixed IP common in today's advanced SoC designs makes accurate labeling difficult, effectively guaranteeing more shorts to fix in the debug process.

Existing solutions

Standard short debug tools simply report the short path. Users must then parse the shapes in the path, step by step. After designers identify the possible location of the short (label or shape), they need to manually change the design, stream out, and then rerun the entire layout extraction. Using this conventional flow to fix any given short can take several debug iterations and many hours.

As a class, standard short debug tools are inherently inefficient. They require a smaller number of shapes in the path and require signoff engineers to be familiar with the design or experienced in short debugging. Standard tools work well for ASIC designs but not for analog/mixed-signal or SoC designs, which include complex hierarchies and IP blocks.

Common design issues can create extreme consequences when using standard short debug tools. For instance, the power/ground short is a routine issue at the final chip-level signoff check; but if the short path includes thousands of shapes, the debug process often becomes an extended, time-intensive task for standard tool users. Likewise, when the design moves from the legacy node to the advanced node, standard tools can impose significant layout extraction runtimes. A single iteration run on a multi-CPU machine can take hours. And multiple iterations can take days.

Like other vendors, Cadence provides a standard short debug tool with the Physical Verification System, as shown in Figure 1.



Figure 1: GUI of standard tool for checking shorts

However, that standard tool may not provide the results needed to find the root cause of some shorts. In those cases, users can work with the Interactive Short Locator to continue investigating the issue.

Interactive Short Locator

The Interactive Short Locator is a separate engine that works with the Cadence Physical Verification System layout vs. schematic (LVS) engine to accelerate the task of finding shorts. After the first layout extraction run, the LVS engine passes the short information to the Interactive Short Locator. Designers then use the Interactive Short Locator to identify the possible root cause of the short with the intelligent user-friendly interface, virtually changing the design labels or marking certain shapes that could cause the short. The Interactive Short Locator takes designer input and quickly runs the diagnosis on the specific design change rather than the entire SoC design. The results are then passed back to the designers to help them further isolate the issue. Figure 2 compares the conventional short isolation flow and the Interactive Short Locator workflow.

Conventional Short Isolation



PVS Interactive Short Isolation



Figure 2: The Interactive Short Locator relies on a separate short-analysis engine to accelerate the debug process

The Interactive Short Locator provides the following essential features and benefits:

- An efficient, separate analysis engine
 - Generates results in less than five percent of the time needed to run a complete extraction
 - Prevents unnecessary extraction runs
- Seamless integration with the Cadence Virtuoso® custom design platform, Cadence Encounter® digital implementation platform, and Cadence QuickView Layout and Manufacturing Data Viewer
 - Allows users to launch and fix a short within both Virtuoso and Encounter environments
 - Runs the short isolation flow through the implementation platform database, eliminating the need for costly stream-out
- Ability to interactively enter labels for different elements of the layout, improving the efficiency of short path debug
- Ability to search the common path connecting different types of user-entered labels or labels already present in the layout
 - Automatically reduces the number of shapes in the short path
 - Helps customers reduce the debug burden and improves debugging efficiency
- Ability to interactively navigate between path elements, establishing a visual understanding of the short
- Ability to split a suspicious shape and check its causal role in a short, helping to confirm an existing short
- A distributed multi-threading architecture
 - Accelerates throughput without the need for specialized hardware

Use Cases

Many Cadence customers have used Physical Verification System with Interactive Short Locator technology to greatly improve their total turnaround time.

In one customer use case, designers use the Interactive Short Locator with the Physical Verification System LVS engine for a 40nm design. The extraction runtime is approximately 80 minutes with a 4-CPU run. Two scenarios have been tested with 1-CPU and 16-CPU runs, where designers launch the LVS check directly through the QuickView Layout and Manufacturing Data Viewer.

In this case, the shorted net is VDD-VSS, and the standard debug tool shows one single short path including all shapes on VDD and VSS nets. Designers run the Interactive Short Locator nine times, completely identifying a total of eight shorts in the VDD-VSS short net. Four metal layers, three via layers, and one label layer are used for the debug. Figure 3 shows one short between metal 2 and metal 3. The “Met3 Split Box” is the interactive box that designers can put in to split a suspicious shape and check its causal role in a short, helping to confirm an existing short.

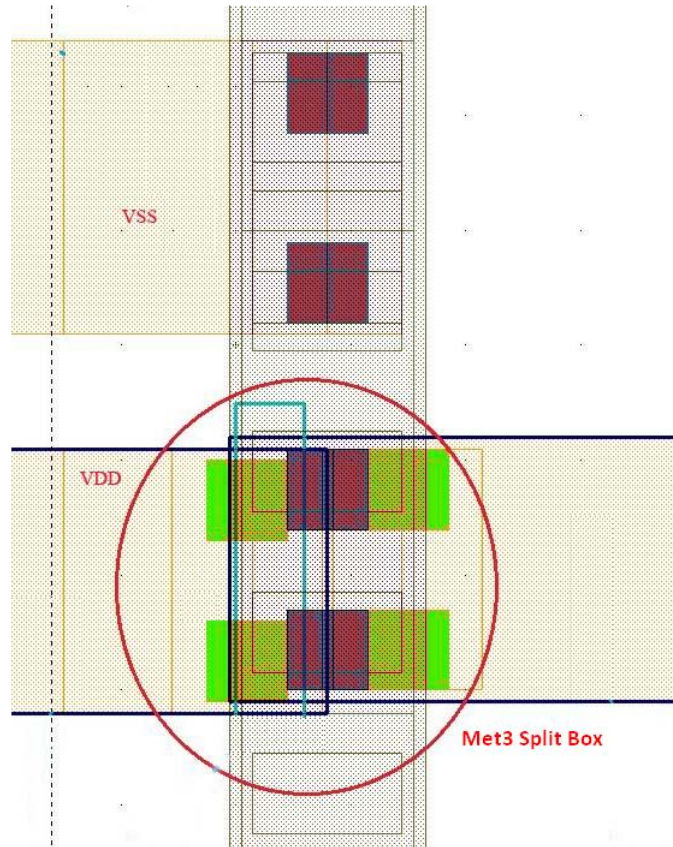


Figure 3: Short example between metal 2 and metal 3

To highlight the efficiency of the Interactive Short Locator, Figure 4 compares the time designers took to find the short in the same design, with and without the Interactive Short Locator. The Interactive Short Locator greatly reduces the short debug time and drastically reduces overall turnaround time from 13 hours to 3 hours 20 minutes on a 16-CPU run.

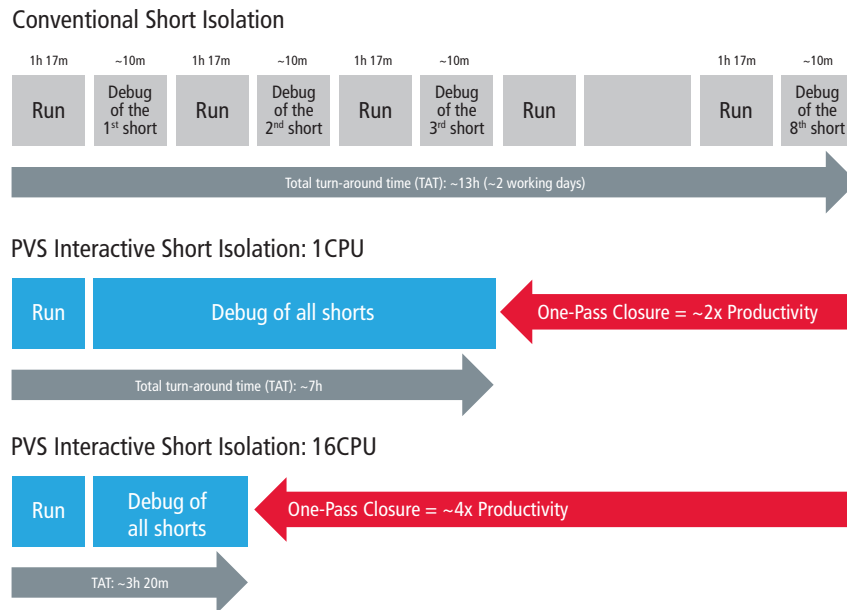


Figure 4: Comparison of short debug times with and without the Interactive Short Locator

Figure 5 demonstrates another use case, where the designer uses the Interactive Short Locator running in the Virtuoso Layout Editor to reduce final signoff turnaround time by a factor of two.

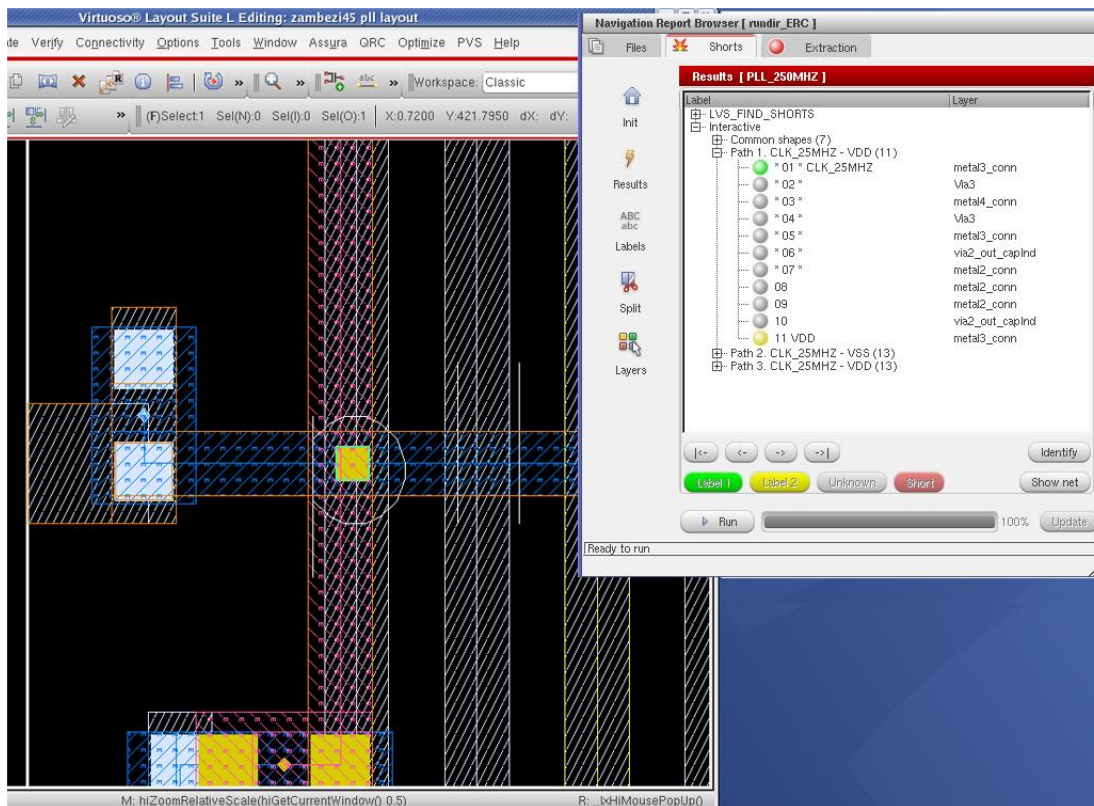


Figure 5: The Interactive Short Locator running within the Virtuoso Layout Editor

Summary

The Interactive Short Locator in the Cadence Physical Verification System provides an efficient and interactive way for SoC designers to find shorts quickly and more accurately. Leveraging Interactive Short Locator technology, design teams can streamline their short debug process, boost their overall verification productivity, and stay on schedule.