DATASHEET

VIRTUOSO LAYOUT MIGRATE

Cadence® Virtuoso® Layout Migrate is the physical layout migration tool of the Virtuoso custom design platform. It supports fast process and design rule migration of hard IP, custom digital designs, mixed-signal blocks, memories, and standard cell libraries.

THE VIRTUOSO CUSTOM DESIGN PLATFORM

When design objectives dictate manipulating precise analog quantities—voltages, currents, charges, and continuous ratios of parameter values such as resistance and capacitance—companies turn to custom design. Full-custom design maximizes performance while minimizing area and power. However, it requires significant handcrafting by a select set of engineers with very high skill levels. In addition, custom analog circuits are more sensitive to physical effects, which are exacerbated at new, nanometer process nodes.

The Virtuoso custom design platform accelerates the design of custom ICs across various process nodes. By selectively automating aspects of custom analog design and providing advanced technologies integrated on a common database, it allows engineers to focus on precision crafting their designs—without sacrificing creativity to repetitive manual tasks.

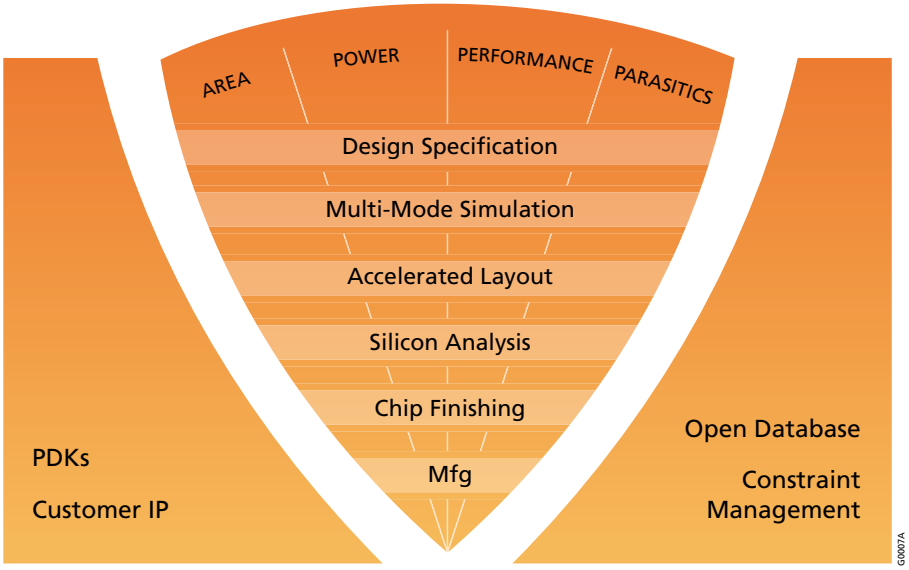

Figure 1: All components of the Virtuoso platform work together to support fast, silicon-accurate differentiated custom silicon

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VIRTUOSO LAYOUT MIGRATE

Virtuoso Layout Migrate enables fast migration of a given design to new or altered process geometry. Integrated within the Virtuoso platform, Virtuoso Layout Migrate provides hierarchical two-dimensional optimization algorithms to achieve significantly higher quality of results (QoR) than traditional methods using near-linear shrinks. Virtuoso Layout Migrate is also a cost-effective solution compared to a purely manual approach—saving both time and labor. Structure preservation and parameterized cell (Pcell) substitution capabilities enhance productivity, while the menu-driven flow configuration environment makes the setup procedure straightforward and efficient.

BENEFITS

- Rapid layout migration through support of all types of layout hierarchy—typically resulting in an order-of-magnitude productivity improvement over manual efforts
- Two-dimensional compaction that produces high QoR as compared with other solutions using one-dimensional algorithms
- Easy-to-use menu-driven setup and configuration, allowing new users to produce high-quality results within days of installation
- Support for complex design rules at 90 nanometers and beyond, targeted to improve yield and circuit performance
- Efficient engineering change order (ECO) implementation

FEATURES

FAST HIERARCHICAL AND TWO-DIMENSIONAL COMPACTION

Virtuoso Layout Migrate has been architected from the ground up to handle hierarchy directly—to enable rapid migration of hierarchical layout such as memories, custom datapath blocks, and mixed-signal designs. The user provides hierarchical GDS or Virtuoso data with a target process technology as input, and is returned an LVS/DRC-correct hierarchical GDS or Virtuoso layout. Abutment, alignment, and pitch matching are all handled implicitly with hierarchical optimization to improve ease of use and capacity on hierarchical and arrayed designs *(see Figure 2)*. Hierarchy-aware migration and technology mapping of Pcell layout is also fully supported *(see Figure 3)*.

All layout structure is preserved, including connectivity, properties, ports, parameters, Pcells, multi-part paths (MPPs), and symbolic contacts. This enables the layout generated by Virtuoso Layout Migrate to be linked with the schematic, rerouted by the Virtuoso router, manually edited, or modified using other layout functions. Optimal layout is achieved with native support for two-dimensional rules such as diagonal spacing, minimum area, 45˚ angles, common run, and end of line. Virtuoso Layout Migrate is a production-proven solution for advanced process geometries requiring special design rules, including preferred rules used for yield and performance improvements *(see Figure 4)*.

EASY-TO-USE MENU-DRIVEN SETUP AND FLOW CONFIGURATION

Virtuoso Layout Migrate includes an easy-to-use menu-driven setup and flow configuration system in the familiar

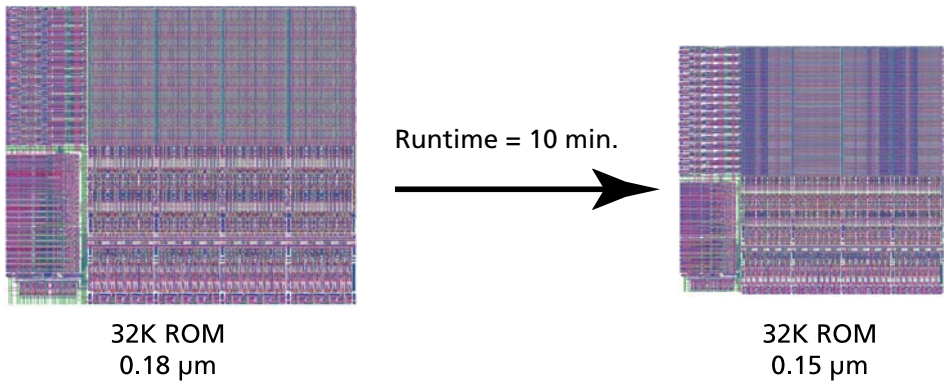

Figure 2: Example of fast layout migration showing implicit handling of hierarchy and abutment

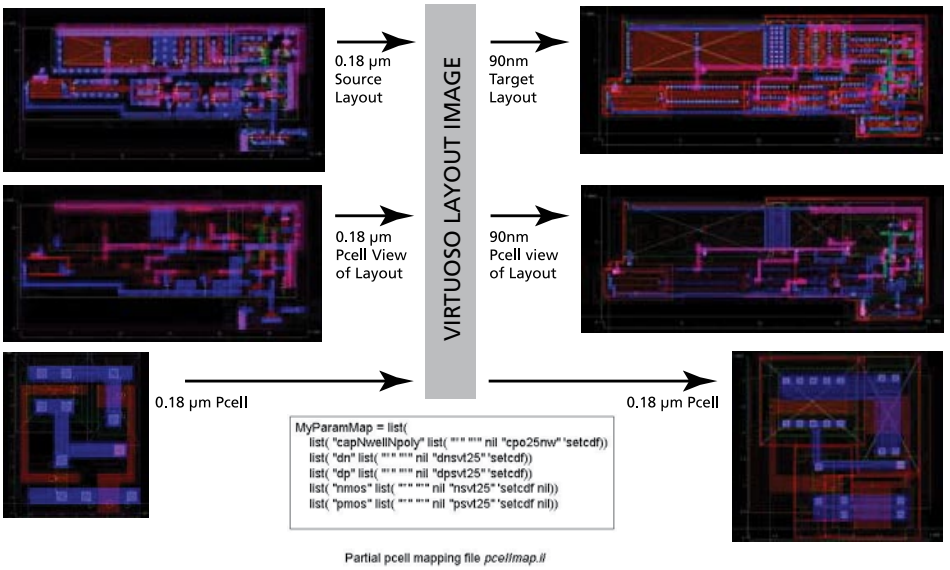

Figure 3: Fast and accurate layout migration with Pcell preservation, with an example of the Pcell map file

Virtuoso environment *(see Figure 5)*. With this menu system, the user can configure, run, and evaluate the results. The configurations menu allows the user to define an optimization flow consisting of preprocess, optimization, and postprocess commands. After a flow has been defined, the user needs only "one button" to optimize or migrate similar designs. A high degree of control within the familiar Virtuoso environment allows the user to freeze parts of the layout, relax a set of design rules, and set the amount of change introduced to achieve a design-rule-correct layout *(see Figure 6)*.

ECO SUPPORT WITH VIRTUOSO SCHEMATIC EDITOR AND NETLIST-BASED DEVICE SIZES

When using Virtuoso Layout Migrate in the ECO process, the user can update device sizes from within the schematics of Virtuoso Schematic Editor, and Virtuoso Layout Migrate will enforce the new device sizes while adhering to the design rules and maintaining circuit connectivity. Virtuoso Layout Migrate can also read in a SPICE netlist, which is then used during layout optimization. The transistor sizes within the layout are matched to the transistor sizes within the SPICE netlist. This device-matching technology works hierarchically and supports mismatched netlist/layout hierarchies.

SPECIFICATIONS

LAYOUT PROCESS AND DESIGN RULE MIGRATION

- Hierarchical two-dimensional optimization
- Structure preservation including paths, MPPs, symbolics, connectivity, and properties
- Pcell substitution to replace Pcells or update their parameters during migration
- Menu-driven setup and flow configuration system
- ECO support with Virtuoso Schematic Editor and netlist-based device sizes

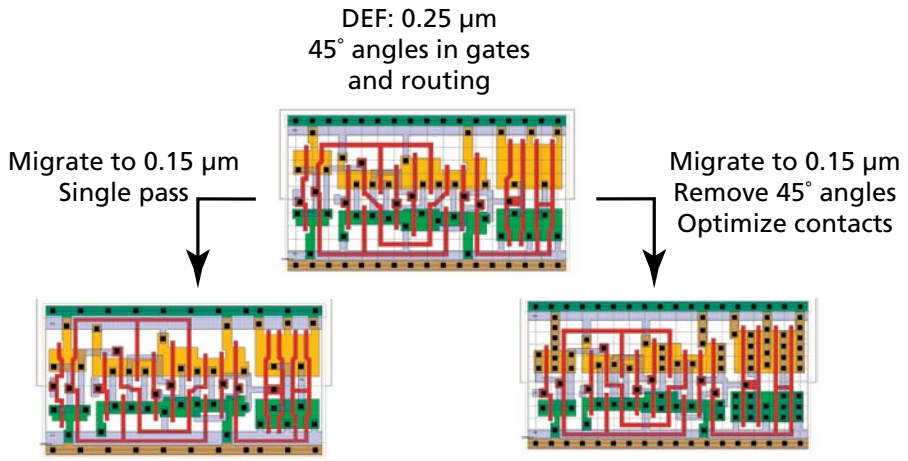

Figure 4: Example of fast layout migration showing the ability to handle complex design rules

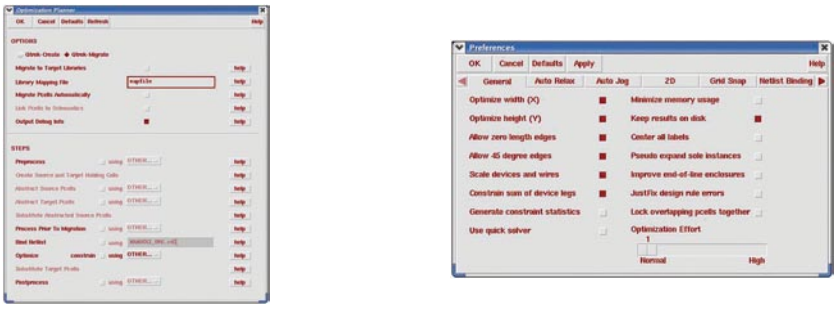

Figure 5: Easy-to-use menu-driven setup and flow configuration system—the fast track to productivity

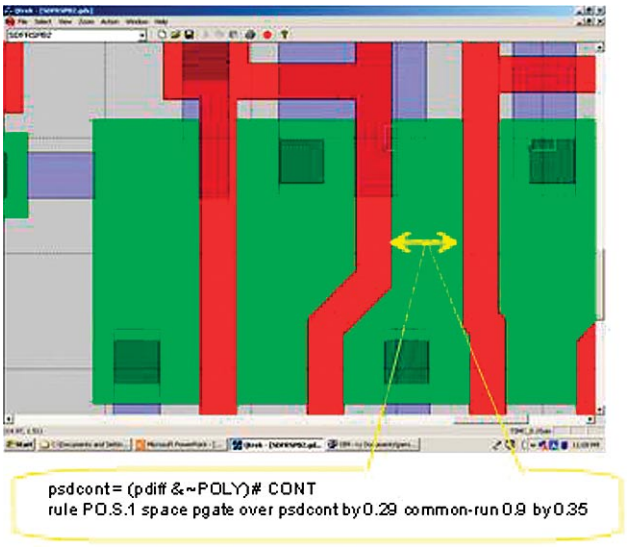

Figure 6: Technology files are easy to understand and write—this example shows how to implement a gate spacing rule

- Interactive user control in the Virtuoso environment
- Support for device-specific and net-specific design rules in advanced process geometry
- Preferred rules for improving yield and performance in leading-edge processes

DESIGN INPUTS

- Cadence CDBA database
- SKILL
- STREAM format
- Virtuoso Schematic Editor
- CDL and SPICE netlist format

DESIGN OUTPUTS

- Cadence CDBA database
- STREAM format

PLATFORM/OS

- Sun/Solaris
- HP-UX
- Linux

THIRD-PARTY SUPPORT

- SKILL-based tools and functions
- Process design kits (please refer to the PDK datasheets for more information)

OTHER ACCELERATED LAYOUT PRODUCTS

- Virtuoso Accelerated Layout: high-end custom block physical layout editor
- Virtuoso Layout Editor: industry-standard custom block physical layout editor
- Virtuoso Chip Editor: chip integration and finishing physical layout editor
- Virtuoso Chip Assembly Router: custom block and chip routing tool

CADENCE SERVICES AND SUPPORT

- Customer-focused solutions that increase ROI, reduce risk, and achieve your design goals faster
  - Collaborative approach and design infrastructure—virtual teaming
  - Proven methodology and flow tuned to your design environment
  - Design and EDA implementation expertise
- Product and flow training to fit your needs and preferred learning style
  - Over 80 instructor-led courses—certified instructors, real-world experience
  - More than 25 Internet Learning Series (iLS) online courses
- Cadence customer support that keeps your design team productive
  - Cadence applications engineers provide technical assistance
  - SourceLink® online support gives you access to software updates, technical documentation, and more—24 hours a day, seven days a week

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