Ultrasim Netlist Based Memory EMIR Flow

Cadence Design System

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ABSTRACT

In the deep submicron era, IR drop and electromigration (EM) analyses are becoming increasingly important. Transistor level dynamic reliability verification for memory is in high demand. Ultrasim netlist based memory EMIR flow was developed to meet this demand with a focus on memory and large mixed signal designs. Empowered by Ultrasim's superior post layout solutions with hierarchical stitching, the new flow offers virtually unlimited capacity for memory-like designs.

The flow involves two steps: the first step is post-layout simulation with parasitics stitched to the prelayout netlist. The geometry information on wires and vias comes in the format of a DSPF or SPEF file. Ultrasim computes IR drop and current density, and stores them in an intermediate database. The second step is basically post-processing, which converts the intermediate database to a CDBA/OA database for displaying in the DFII platform as violation maps. The flow can also output textual reports. To help navigate through the violation maps, an easy-to-use GUI was developed and was seamlessly integrated with the Virtuoso Layout Editor. The GUI features were designed to help users quickly identify the location of the problems and understand the causes and potential fixes.

Ultrasim's EMIR flow complements the existing Cadence reliability solutions. With the new flow targeting custom design space, Voltage Storm transistor level (VST) specializing in power grid analysis of digital designs and VAVO/VAEO focusing on small analog circuits, Cadence now offers reliability solutions that cover the whole spectrum of designs. Customer Beta engagements are under way.

1. INTRODUCTION

With CMOS process technology scaling down to 45nm and below, reliability analyses, such as IR drop and electromigration, are becoming increasingly important; they determine the performance and reliability of the chip. IR drop effect manifests itself mainly in the power grids and can potentially degrade the performance of the design. In its worst case, excessive IR drop may result in a functional failure in dynamic logic and a timing violation in static logic. In nanometer designs, the supply voltage has generally been reduced to 1V or below. With the ever shrinking interconnect size, the resistance per unit length of wires is increased, reducing the available V_{DD} at transistor contacts, which in turn degrades the switching speed of the CMOS gates and their DC noise margins. It has been shown that a 10% voltage drop in a 0.18um design increases the propagation delay of the gates by up to 8% [1]. Electromigration (EM) has more complicated mechanisms than IR drop. By definition, electromigration is the mass transport of a metal due to the momentum transfer between conducting electrons and diffusing metal atoms. It has long been recognized as a potential wear-out failure in VLSI circuits by causing shorts and voids (open) in the circuitry. Electromigration is thermally activated, its magnitude is proportional to average current density. Narrower metals usually encounter worse electromigration problems due to higher current density. In addition, Joule heating of conductors, caused by the root mean square (RMS) current, can aggravate electromigration, this is why both RMS current density and average current density must be limited in a design. There are many ways to tame the electromigration issues, for example, using different materials, changing the temperature and reducing current density. From a designer's point of view, limiting current density across the whole design is achievable by modifying the design. Limiting current densities is known as reliability budgeting. The limits are functions of interconnect size, temperature and process variations.

Reliability analysis can be done at both block and full chip level. It is reasonable to start looking at reliability problems early in the design cycle, as soon as the layout of a functional block is completed. The integrity of the power grid and signal nets in a block may be quickly analyzed and the appropriate changes should be made in the layout. Many common design mistakes can be found by performing block level analysis[2]. Some assumptions about the supply voltages, where a block connects either to the global power grid or other blocks, have to be made. However sometimes, due to the tight and complex interactions between different blocks of the design, it is hard to estimate the potential effects of reliability problems in a block-based context where current may be supplied to neighboring blocks. This is one of the reasons that full-chip analysis must be performed before sign-off to ensure that no IR and EM related problems will occur in the assembled design. At this stage, all parasitic elements can be extracted based on the layout and technology description. The ability to apply reliability analysis at the full chip level makes it possible to bring product reliability and reliability budgeting into designers' hands.

Traditionally for digital designs, an activity based static methodology is employed for full chip analysis. Clock cycles, average charges and/or capacitances with probabilities of switching activities are considered. Practical experience has shown that most reliability issues will show up during analysis based on static current data[3]. Static methods provide large capacity, fast turn around time and thorough coverage with the possibility to exercise all the nodes. However, the static estimation lacks accuracy for deep submicron SoC and memory designs, this is where transistor level (dynamic) full chip verification comes into play. Dynamic solutions provide transistor level accuracy and can handle instantaneous IR drop and EM due to simultaneously switching gates, but it comes with sacrifices, namely long simulation time. In reality, static and dynamic methodologies are both employed complementarily in a reliability flow, with static analysis normally conducted early in the design cycle and dynamic verifications later in the design cycle, after layout and extraction are completed.

Customers are asking for a transistor level dynamic reliability analysis tool that can handle real peak behavior on memory and large mixed signal designs. Reliability of both power grids and signal nets are of interest. Currently one competitor provides a solution in this area. The IR drop and EM information can be color-coded in so-called violation maps in GDSII format, which is then streamed into Virtuoso Layout Editor. The process is time consuming and quite user unfriendly. Overlaying the violation map on top of the original layout is very complicated. Since it is based on the GDSII format, its efficiency and capacity are in question. On the other hand, Ultrasim netlist based memory EMIR flow is built directly on the Virtuoso platform, taking advantage of the efficient CDBA and OA database. Simulation efficiency and user friendliness are major thrusts in Ultrasim's EMIR flow. Overlaying the violation map on top of the original layout can be accomplished by just one click of the mouse. Ultrasim's EMIR flow complements the existing Cadence reliability solutions. With the new flow targeting custom design space, Voltage Storm transistor level (VST) specializing in power grid analysis of digital designs and VAVO/VAEO focusing on small analog circuits, Cadence now offers reliability solutions that cover the whole spectrum of designs.

The key technologies in Ultrasim netlist based EMIR flow are presented in Section 2, followed by a few examples in Section 3, then a summary in Section 4.

2. KEY TECHNOLOGIES in Ultrasim Netlist Based EMIR Flow

Ultrasim is Cadence's hierarchical fast spice simulator. With fast-spice technologies, such as partitioning, isomorphism and simplified models, Ultrasim boasts virtually unlimited capacity for memory-like designs. Empowered by its hierarchical stitching techniques, Ultrasim offers superior post layout solutions, which serves as the foundation for the new flow. Ultrasim netlist based EMIR flow can analyze not only power grids, but also signal nets. The flow has two steps: the first step is to conduct post-layout simulation with parasitics back-annotated (a.k.a stitched) to the prelayout netlist. The geometry information on wires and vias/contacts along with parasitics comes in the format of a DSPF or SPEF file. After simulation finishes, a binary database is created. The second step is to convert the binary database to a CDBA and/or an OA database, the CDBA and OA database can be displayed in Virtuoso Layout Editor for interactive debugging. The key technologies in this flow, specifically, simulation and integration with Virtuoso environment, are discussed in this section.

Ultrasim netlist based EMIR flow is a dynamic tool for full chip verification. The tremendous amounts of data inherited in this problem are challenging, especially in EM analysis where RC reduction is generally not recommended. Data storage and management, simulation performance and analysis efficiency are all critical. Simulation is the first step of the flow. Ultrasim detects isomorphism of back-annotated parasitics and compactly store them in a highly compressed hierarchical library developed for capacity and performance. An efficient power network detection algorithm was developed to search for connected pieces of designated RC nets that are spread over the entire design for the purpose of EM and IR calculations. Furthermore a proprietary power network solver (UPS) was developed, it is an optimized solver designed to analyze linear power networks. In addition, for efficiency, Ultrasim computes IR drop and current density, including peak, average and rms values on-the-fly. When simulation is done, an intermediate binary database is generated.

The second step is basically post-processing. A utility tool is developed to convert the binary database generated during simulation to a CDBA or an OA database for displaying directly on the Virtuoso platform as violation maps. The CDBA/OA

database contains IR drop information for nodes and current density information for resistors, organized into groups. Each group is uniquely identified by a net name and the type of analysis on the net. The supported analysis types are peak IR drop, average current density, RMS current density and peak current density. By changing a so-called control file, it is easy for the user to control the types of analysis on specific nets. The format for EM rule files are compatible with other Cadence EM tools such as Virtuoso Analog Electromigration Option (VAEO). It supports temperature dependency and expression. This step is built directly on the Virtuoso platform, a very much appreciated feature over the competition. The flow outputs textual reports and color-coded violation maps. To help navigate through the violation maps, an easy-to-use GUI is developed and is seamlessly integrated with the Virtuoso Layout Editor[3]. This GUI provides designers with the following useful functionalities: (1) graphical display of the IR drop and EM violation standalone or on top of original layout; (2) cross-probing between the textual report and the violation maps; (3) customization of the visualization—changing color levels, control color map, sorting… etc. With the assistance of the GUI, circuit designers can quickly identify the location of the problems and understand the causes and potential fixes of the issues.

3 EXAMPLES

Three test cases are discussed in this section to demonstrate the advantages of the flow. A small VCO block is chosen to illustrate how the flow works and what the GUI looks like. A large ADC test case and a medium sized memory case are chosen to demonstrate the efficiency of data storage and management.

3.1 *VCO*

This is the smallest of the three test cases. The design has 300 MOSFETs and 2100 resistors. Capacitance is not extracted, Because of the small size, Ultrasim A mode is used. A DSPF file is generated by Assura RCX and is stitched to the pre-layout netlist for post-layout simulation. IR drop for power nets (VDD and VSS) and EM analysis for all nets are conducted, so no RC reduction is applied. The layout is in DFII CDBA format. Figure 1.a) is the color-coded map of the IR drop for VSS net.

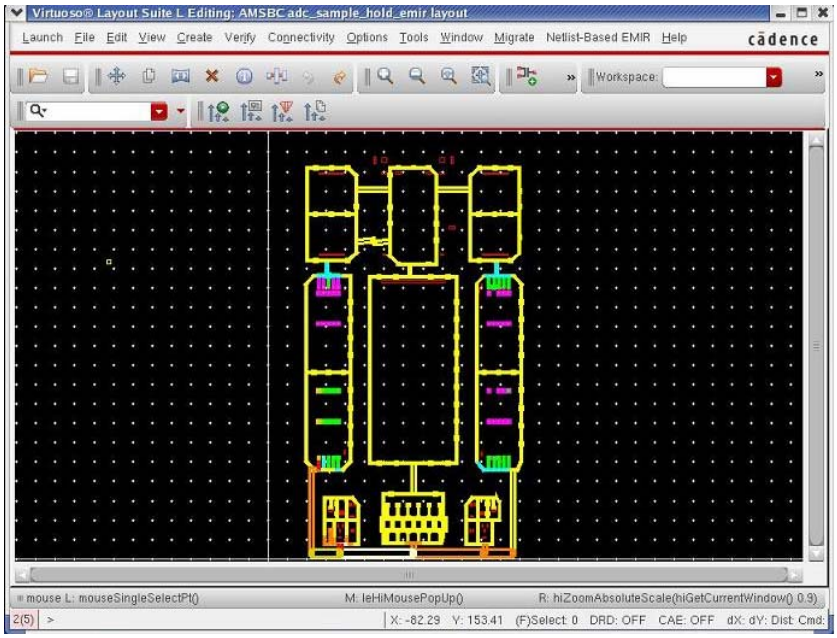

Figure 1.a) the color-coded map of IR analysis for the vss net

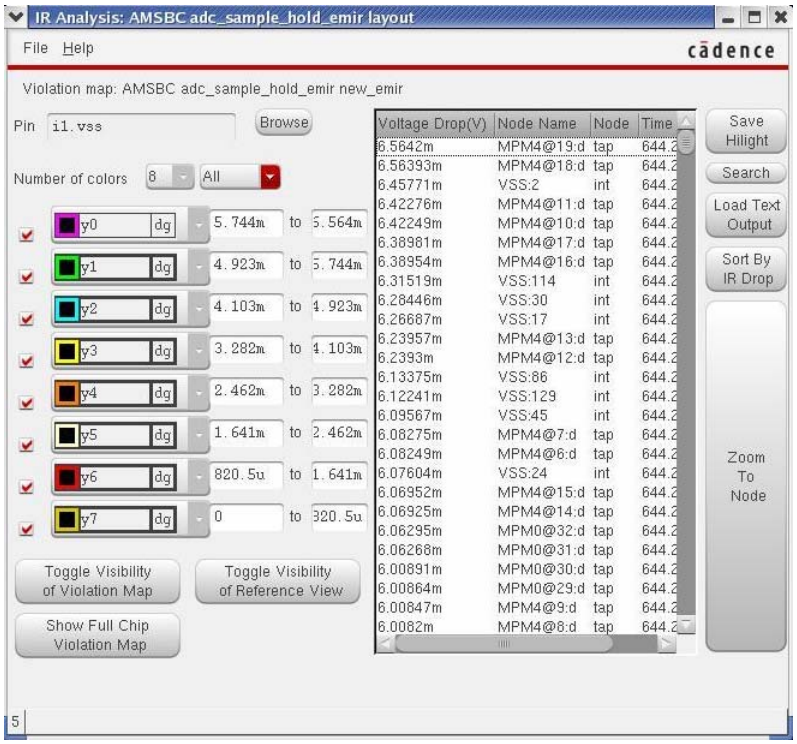

Figure 1.b) the user interface of IR analysis

Figure 1.b) is the user interface (UI) for IR drop analysis. The textual report is also shown in the GUI interface. The user can navigate through all the power nets. For each power net, the user can change the color of the bins. The user can choose to overlay the violation map on top of the original layout or display the violation map standalone. The cross-probing capability is provide by clicking the button “zoom to the net”.

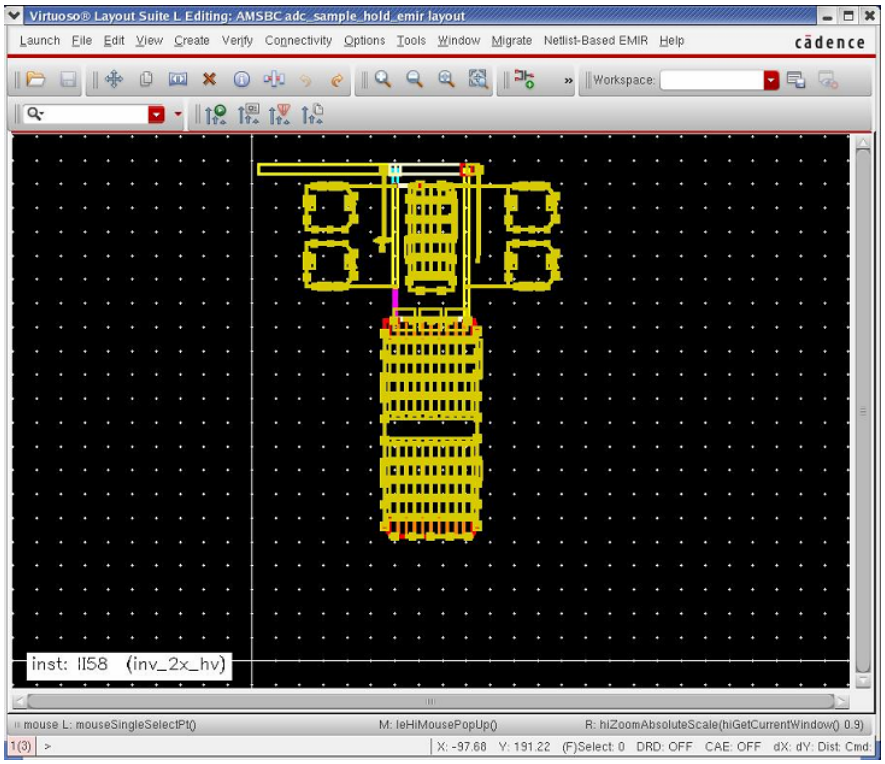

Figure 2.a) the color-coded EM violation map of the vdd net

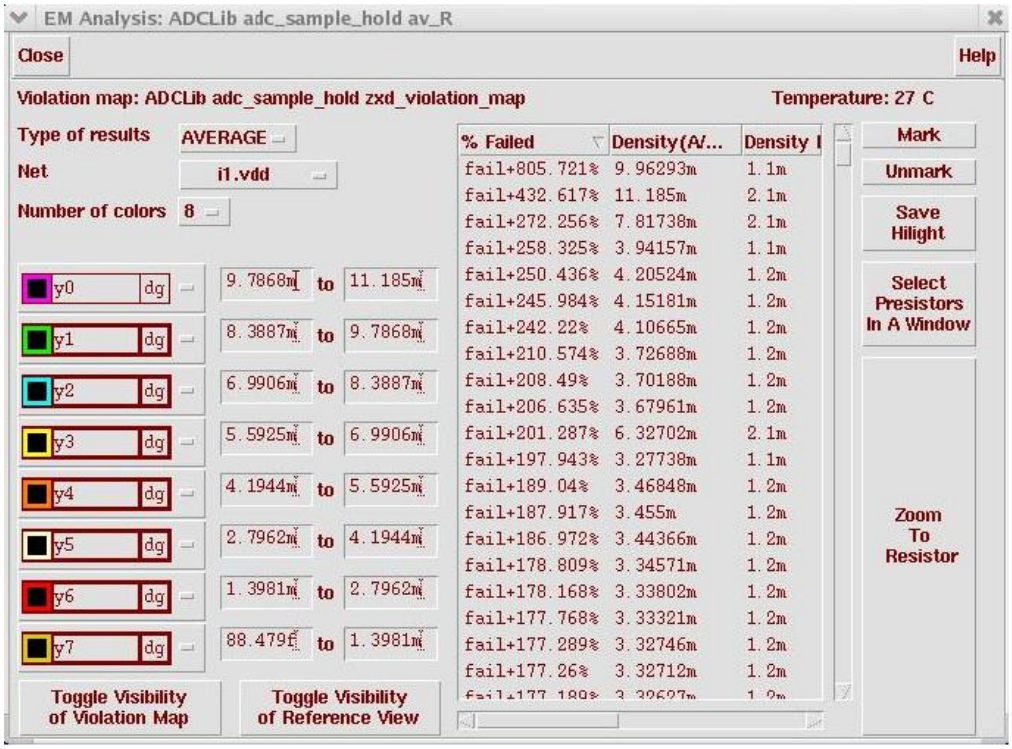

Figure 2.a) The User Interface of EM analysis

Figure 2.a) is the color-coded violation map of the EM analysis for VDD net. The EM GUI interface is shown in Figure 2.b). As with the UI for IR drop analysis, the user can navigate through nets, overlaying the violation map on top of the original layout. Cross-probing capability is provided by clicking “zoom to resistor” or “Select Presistors in a window”.

3.2 Large ADC

This test case is a large ADC test case. Only VDD net is extracted for power integrity analysis. The circuit consists of 600K MOSFETS, 3 Million parasitic resistors and capacitors on the power net. Since both IR drop and EM analysis of the power networks are of interest, no RC reduction can be applied. Extracted parasitics are in DSPF file format and they are stitched into the hierarchical pre-layout netlist. With the EMIR flow, total simulation time for 25 clock cycles takes 8 hours on an AMD Opteron 64bit Linux machine with 2.4GHz CPU. The created binary database is about 300MB, it took only 15min to convert it to CDBA on the same machine.

3.3 *Memory*

The third example is a memory design that consists of 200K mosfet, 1.8 Million resistors and 200K capacitors. The EM of the signal nets are of interest, no RC reduction is applied. The simulation took 2 hours on an AMD Opteron 64bit Linux Machine with 2.6GHz. The binary data base is 464MB, the conversion to CDBA took 23min on the same machine.

4 SUMMARY

Ultrasim netlist based EMIR flow was developed for IR drop and EM analysis on memory and large mixed signal designs. Based on Ultrasim’s superior post layout solutions with hierarchical stitching, the compaction of the simulation database was enhanced. Ultrasim computes IR drop and current density, including peak, average and rms values on-the-fly and stores them in a highly compressed hierarchical library developed for capacity and performance. The flow is built directly on the Virtuoso platform. Both a textual report and a graphic display are provided. An easy-to-use GUI in DFII is available. Initial customer engagements have proven the efficiency of the technology as well as the user-friendliness of the flow. The flow has been in production release since July 2007. A possible future expansion of the technology will be integration with physical design, such as simulation driven layout with constraints.

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