

VIRTUOSO SPECIFICATION-DRIVEN ENVIRONMENT

The Cadence® Virtuoso® Specification-Driven Environment is the advanced design and simulation environment for the Virtuoso custom design platform. By supporting extensive exploration of multiple designs against their objective specifications, Virtuoso Specification-Driven Environment sets the standard for fast, accurate design verification.

THE VIRTUOSO CUSTOM DESIGN PLATFORM

When design objectives dictate manipulating precise analog quantities—voltages, currents, charges, and continuous ratios of parameter values such as resistance and capacitance—companies turn to custom design. Full-custom design maximizes performance while minimizing area and power. However, it requires significant handcrafting by a select set of engineers with very high skill levels. In addition, custom analog circuits are more sensitive to physical effects, which are exacerbated at new, nanometer process nodes.

The Virtuoso custom design platform accelerates the design of custom ICs across various process nodes. By selectively automating aspects of custom analog design and providing advanced technologies integrated on a common database, it allows engineers to focus on precision crafting their designs—without sacrificing creativity to repetitive manual tasks.

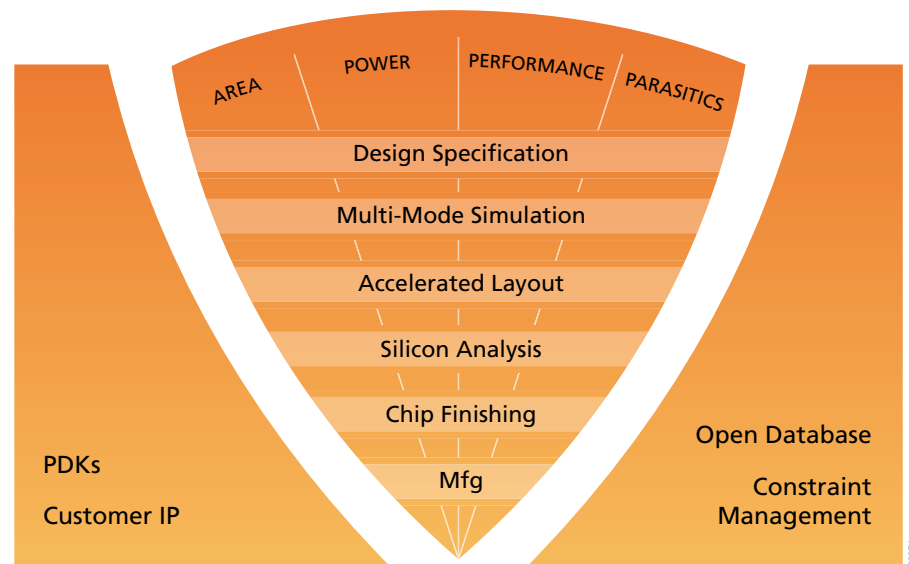


Figure 1: All components of the Virtuoso platform work together to support fast, silicon-accurate differentiated custom silicon

VITUOSO SPECIFICATION-DRIVEN ENVIRONMENT

Virtuoso Specification-driven Environment manages the exploration and verification of multiple designs in one easy-to-use tool. Throughout the design and verification process any circuit can be monitored against its objective specifications with fast pass/fail feedback. In addition, all the sweeps, corners, Monte Carlo statistics, and measurements are managed in one location for fast and accurate verification of a design.

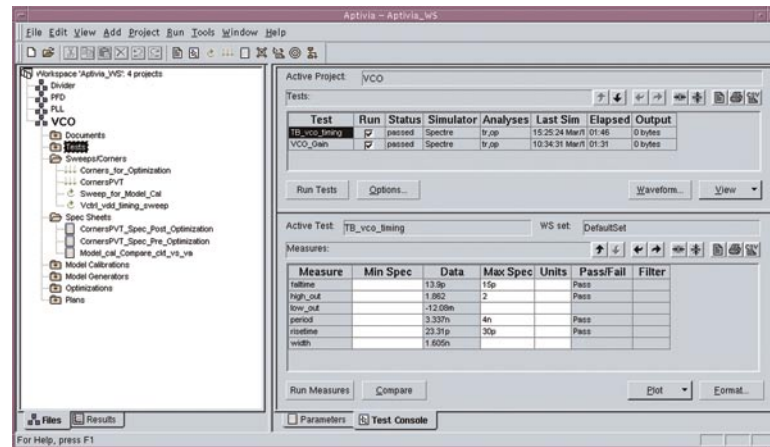
BENEFITS

- Maintains specification/design agreement with constant monitoring of objectives status
- Facilitates design reuse by capturing the design process as IP
- Improves verification speed with simulation distribution and multi-test management
- Improves quality through the standardization of design methodologies
- Manages multiple designs and all associated test requirements in one environment
- Provides visibility into the design status of multiple projects across multiple sites
- Enables easier design reviews with integral documentation, specifications, measurement results, and waveforms

FEATURES

SPECIFICATION-DRIVEN DESIGN

The Virtuoso Specification-driven Environment combines specification entry and design management into a single unified cockpit to accelerate design verification. A specification is made up of multiple tests, which are formed by combining test harnesses with specific measurements. The Virtuoso Specification-Driven Environment enables multiple tests to be developed and exercised over multiple conditions to validate design performance against the design specification. Once created, the tests and the complete specifications can be shared and managed across



SPECIFICATIONS

INTERACTIVE SIMULATION ENVIRONMENT

- Easy to learn and enter data
- Simulation set-ups can be reused
- Quick analysis of multiple simulation data
- Cross probing support for both schematics and layouts
- Multiple measurement syntaxes supported
- Clear tabular displays of test set-ups
- Testbench management built-in
- Support multisite workspaces
- Easy creation of design specification sheets (see Figure 4)
- Batch scripting

WAVEFORM DISPLAY

- Supports multiple Y-axes, strip plots, and Smith Charts
- Built-in waveform calculator
- Independent subwindow displays
- Horizontal and vertical measurement markers
- Independent pan and zoom capability
- User-defined labels and titles
- Color and line style controls
- Signal browser

Sweep	Test	Measure	Conditions	Min Spec	Min Value	Max Value	Max Spec	Pass/Fail
1	CornersPVT	VCO_Gain	max_freq	process_cornen=NN SS SS SS SF SF SF SF FS FS FS FS FF FF FF FF Vdd=1.8 1.6 1.6 2.2 1.6 1.6 2.2 1.6 1.6 2.2	325M	426.1M	640.4M	Pass
2	CornersPVT	VCO_Gain	min_freq	process_cornen=NN SS SS SS SF SF SF SF FS FS FS FS FF FF FF FF Vdd=1.8 1.6 1.6 2.2 1.6 1.6 2.2 1.6 1.6 2.2		46.86M	271.1M	220M Fail
3	CornersPVT	VCO_Gain	vco_gain	process_cornen=NN SS SS SS SF SF SF SF FS FS FS FS FF FF FF FF Vdd=1.8 1.6 1.6 2.2 1.6 1.6 2.2 1.6 1.6 2.2	275M	370.5M	733M	750M Pass

Figure 4: Specification sheet analysis

DISTRIBUTED PROCESSING

- Parallel analysis option
- Efficient use of existing computer farms
- Built-in basic load balancing or interface to other LSF load-balancing tools
- Job monitoring and controlling functions
- Graphical user interfaces for set-up and viewing status

DESIGN INPUTS

- OpenAccess data objects
- Cadence CDBA data objects
- SPICE

DESIGN OUTPUTS

- SPICE
- PSF Waveform format
- Perl language
- HTML

PLATFORM/OS

- Sun/Solaris
- HP-UX
- Linux

CADENCE SERVICES AND SUPPORT

- Customer-focused solutions that increase ROI, reduce risk, and achieve your design goals faster
 - Collaborative approach and design infrastructure—virtual teaming
 - Proven methodology and flow tuned to your design environment
 - Design and EDA implementation expertise
- Product and flow training to fit your needs and preferred learning style
 - Over 80 instructor-led courses—certified instructors, real world experience
 - More than 25 Internet Learning Series (ILS) online courses
- Cadence customer support that keeps your design team productive
 - Cadence applications engineers provide technical assistance
 - SourceLink® online support gives you access to software updates, technical documentation, and more—24 hours a day, seven days a week

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