

ASSURA DESIGN RULE CHECKER

Cadence® Assura® Design Rule Checker (DRC) is part of the design verification suite of tools within the Virtuoso® custom design platform. Assura DRC is a full-featured tool that supports both interactive and batch operation modes and utilizes hierarchical processing for fast, efficient identification and correction of design rule errors in even the most advanced designs.

THE VIRTUOSO CUSTOM DESIGN PLATFORM

When design objectives dictate manipulating precise analog quantities—voltages, currents, charges, and continuous ratios of parameter values such as resistance and capacitance—companies turn to custom design. Full-custom design maximizes performance while minimizing area and power. However, it requires significant handcrafting by a select set of engineers with very high skill levels. In addition, custom analog circuits are more sensitive to physical effects, which are exacerbated at new, nanometer process nodes.

The Virtuoso custom design platform accelerates the design of custom ICs across various process nodes. By selectively automating aspects of custom analog design and providing advanced technologies integrated on a common database, it allows engineers to focus on precision crafting their designs—without sacrificing creativity to repetitive manual tasks.

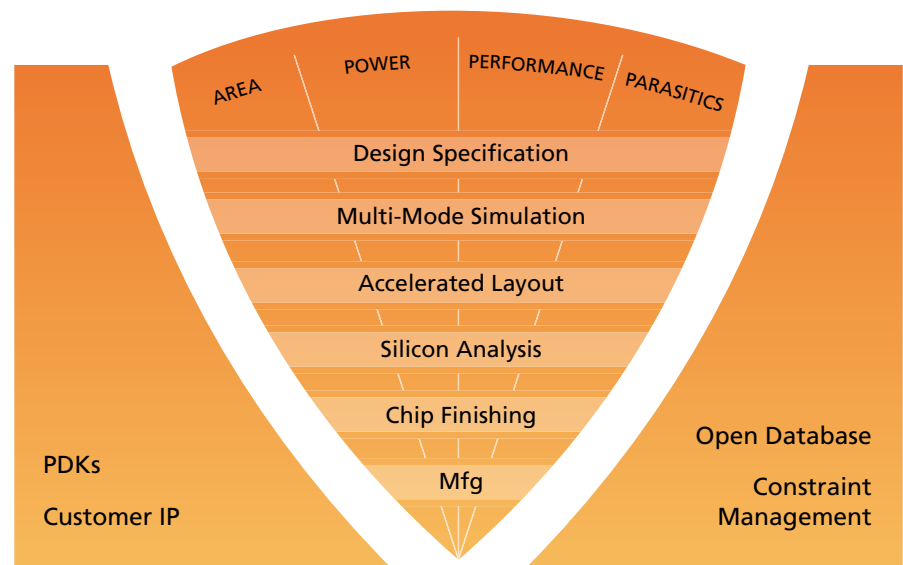


Figure 1: All components of the Virtuoso platform work together to support fast, silicon-accurate differentiated custom silicon

ASSURA DRC

Assura DRC is part of the Virtuoso custom design platform that enables design teams to check, identify, and correct design rule errors and achieve design sign-off before tapeout. Using hierarchical processing techniques, Assura DRC can efficiently handle designs with high complexity and many levels of layout hierarchy. Assura DRC, combined with Assura LVS and Assura RCX, provides the best choice for doing fast and accurate silicon analysis of your custom designs.

BENEFITS

- Simplifies design process with a common database for data transfer within the Virtuoso custom design platform
- Accelerates design-to-volume with production-proven interactive design rule checking
- Reduces re-spins by eliminating design rule errors before tapeout
- Ensures fast, silicon-accurate custom design with an integrated silicon verification and analysis flow within the Virtuoso custom design platform

FEATURES

UNIQUE PATTERN CHECKING

With design features getting smaller and smaller, both design rule volume and complexity are increasing exponentially. Certain rules, such as metal enclosure of contact at line-end, are not easy to write and are best checked using pattern recognition methods. The Assura DRC unique pattern checking capabilities enable simple rule development and maintenance for hard-to-write rules. Fast checks for simple environments can provide up to 20x performance improvement for such checks, which in turn can improve the overall runtime for the entire DRC task up to 2x.

A set of design rules can be described by drawings in a model, which can be specified in GDSII or DFI format or ASCII coordinates (see *Figure 2*). A model contains a primary polygon (contact, fuse opening, DRC error marker) and environment polygons (metals enclosing contact, fuse metals/vias, waivable layout configuration per error marker). Pattern check is triggered only if a primary polygon is found in the design. This pattern checking capability is unique to Assura DRC, making it extremely easy to specify complicated rules and improving DRC runtime performance.

DENSITY CHECK AND METAL FILL

Metal or area fill is needed in certain layouts to balance the density in the sparse and dense areas. Assura DRC offers users the option to do density checks and decide where fill patterns are needed in the layout. Typically, fill patterns are placed where density is low so that the layout has an even distribution of polygons for every layer across the chip. Density check can be done for the whole chip or in a little “stepped” window that moves across the layout.

After performing the density check, the next step is to add fill patterns to the layout. Assura DRC offers “context-sensitive” fill patterns, meaning users can place whatever patterns wherever they are needed in the layout. As shown in *Figure 3*, fill patterns can be customized and in whatever shape (custom fill cells, squares, rectangles, skewed, bridging bars) necessary for balancing the layout density. The area fill command is also capable of connecting all features together to the same equal-potential. Assura DRC can perform area fill in flat or hierarchical mode.

INTERACTIVE AND BATCH VERIFICATION

Assura DRC can perform design rule checking in both interactive and batch mode. The ability to perform physical verification interactively within the Virtuoso custom design platform is especially important for design teams to hand-craft their full custom ICs in order to maximize silicon performance and yield. The Assura DRC interactive use model is very similar to that of Diva® physical verification. Batch verification mode can be applied when hand-crafted custom blocks are assembled to form the finished chip. Only a single rule file is needed for both interactive and batch verification.

HIERARCHICAL PROCESSING

Assura DRC uses hierarchical processing techniques to perform design rule checking, resulting in higher performance and capacity. Designs such as memory that utilize various levels of layout hierarchy can be efficiently checked with the hierarchical processing techniques. Furthermore, design rule errors reported hierarchically helps users locate them quickly and solve the problem at the root cause as errors in the same hierarchy only have to be corrected once. Hierarchical processing is included in the base price of Assura DRC.

Figure 2: Pattern check is triggered by primary polygons in the design

UNIFIED ENVIRONMENT

Assura DRC is an integral part of the Virtuoso custom design platform. Every release of Assura DRC is flow tested with the other segments of the platform. The unified environment makes it easy for users to design custom ICs starting from physical layout design to physical verification to parasitic extractions to simulation and analysis before tapeout, leading to increased design productivity, chip performance, and silicon yield.

MASTER KEY

The master key is a feature of the Cadence customer-focused adoption program with Assura physical verification, aiding customers during the transition of Diva or Dracula® products to Assura verification. The master key enables you to convert existing Diva or Dracula licenses to Assura licenses such that Assura licenses can be used to run Diva and Dracula tools during the transition. Please check with your Cadence sales representative for more detail of the master key.

SPECIFICATIONS

POWERFUL RULE LANGUAGE/ SYNTAX

- Area-based rules allow multiple design rules on a single chip
- Hierarchical area fill capabilities with support for customer-defined filler cells
- SKILL-based rules language facilitates complex data manipulations and DRC rules
- Comprehensive antenna rule syntax supports conjunctive, conditional rules and multiple checks in one run
- Advanced features include data snapping, end-of-line checks, corner commands
- Support width-dependent separation check (90nm halation rule)
- Read Diva rules files directly; Dracula rule translator provided

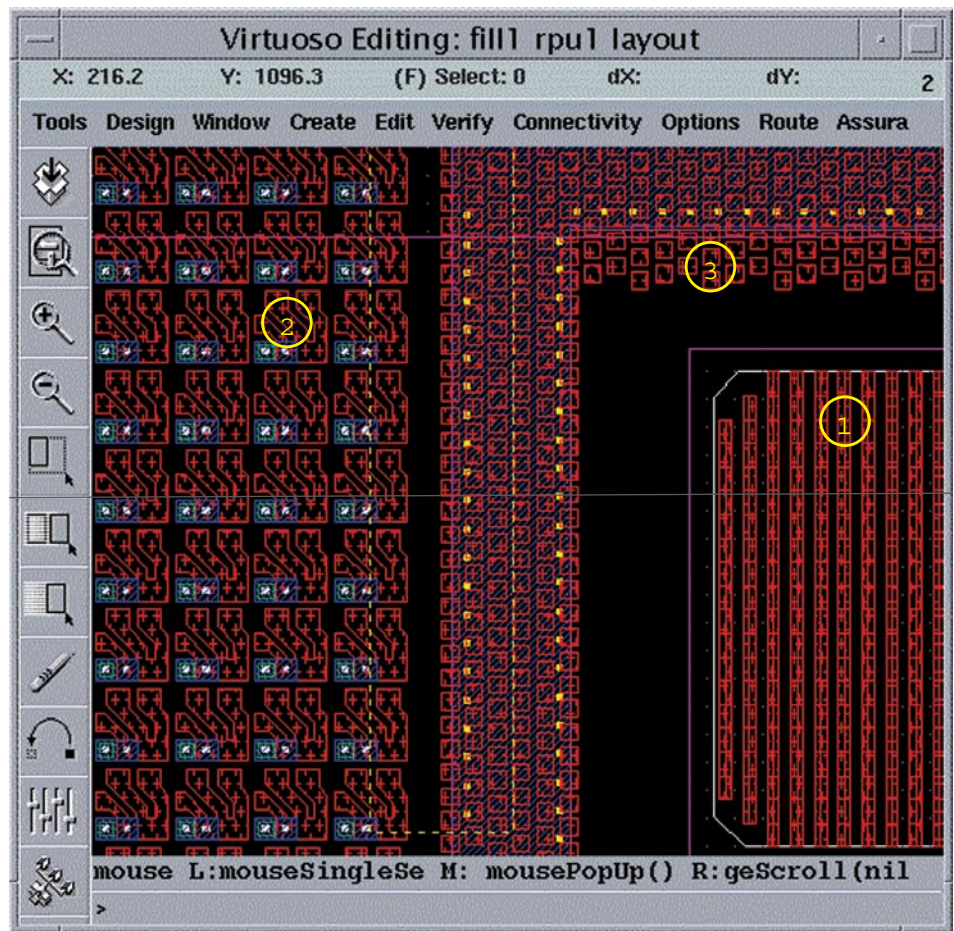


Figure 3: Sample context-dependent fill recipe: rectangular fill (1) under bond pad, grounded multi-layer custom fill (2) pattern in empty areas, skewed square fill (3) under power lines

PERFORMANCE AND CAPACITY

- Patented hierarchical algorithms (cell repetition analysis, auto-adaptive partitioning, and auto-array recognition) process large volumes of data
- Multiprocessor support for reduction in runtime (uses both rules-based and data-based parallelism to optimize runtimes automatically)
- Restart function for interrupted jobs saves precious CPU time

EASY-TO-USE GRAPHICAL USER INTERFACE (GUI)

- Tightly integrated with Virtuoso Layout Editor and Virtuoso Analog Design Environment
- Fast error correction using edit-in-place or descend modes within Virtuoso Layout Editor
- Show errors by rule type or by layout cell
- Perform XOR comparison between two databases
- Support sign-off or false error marker exception handling
- Window DRC operation allows fast localized checking, especially useful during chip assembly or for last minute edits to reduce redundant checking and runtimes

- Immediate error and warning messages during interactive sessions via command interpreter window (CIW)
- Access layout data in edit- or read-only modes
- Remote job submission/LSF support

DESIGN INPUTS

- Cadence CDBA database (DFII) or OpenAccess
- GDSII layout data (single or multiple GDSII files)
- Diva, Vampire, or Assura rules
- Dracula rules (via translator)

DESIGN OUTPUTS

- Cadence CDBA (DFII) or OpenAccess data
- GDSII
- Error markers
- Textual reports for debugging and archival purposes

INTERFACES

- Knights Technology

PLATFORM/OS

- Sun/Solaris
- HP-UX
- IBM AIX
- Linux (Red Hat)

CADENCE SERVICES AND SUPPORT

- Customer-focused solutions that increase ROI, reduce risk, and achieve your design goals faster
 - Collaborative approach and design infrastructure—virtual teaming
 - Proven methodology and flow tuned to your design environment
 - Design and EDA implementation expertise
- Product and flow training to fit your needs and preferred learning style
 - Over 80 instructor-led courses—certified instructors, real world experience
 - More than 25 Internet Learning Series (iLS) online courses
- Cadence customer support that keeps your design team productive
 - Cadence applications engineers provide technical assistance
 - SourceLink® online support gives you access to software updates, technical documentation, and more—24 hours a day, seven days a week

CADENCE PDK AND FOUNDRY SUPPORT

Assura DRC rule files are fully qualified for use with the Cadence process design kits (PDKs), which can be obtained for free from the merchant foundries. These kits are developed and tested by Cadence and supplied to the foundries to support your success in designing chips with particular foundry processes. Please check your merchant foundry web site for the availability of PDK and Assura DRC rule files.

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