Getting **plastered**

EDA tools have helped to bring to fruition a mixed signal chip targeted at a 'digital plaster' application.

*By **Vanessa Knivett**.*

Until relatively recently, wireless technology was regarded as a possible source of interference for critical hospital systems. However, now that approvals have been granted for diagnostic devices that integrate wireless technology – such as Given Imaging's M2A wireless endoscope – and restrictions have been eased on the use of mobile phones in some hospital areas, there is a strong case for healthcare service providers to make more use of the technology.

One such application is remote patient monitoring, which could be achieved using body worn sensors connected wirelessly to a handheld device. Information could then be fed to a central database, from which medical practitioners could track a patient's progress. Remote monitoring would allow patients more freedom, replacing the sometimes bulky devices that need to be used in situ.

Toumaz Technology is one company developing wireless wearable sensors for remote monitoring applications. Having developed Sensium, an ultra low power sensor interface and transceiver platform, the company is now integrating it into a digital plaster style application that could be used to provide real time healthcare monitoring.

When combined with a variety of chemical sensors, Sensium can be used for wireless monitoring of multiple vital signs, such as ECG, heart rate, body temperature, respiration and physical activity. Ironically, Toumaz believes the technology could not only be used to monitor patients with chronic conditions, such as heart disease, but also for monitoring elite athletes in training as they prepare for competition.

Applications such as these require high reliability and exceptionally low power. Low power consumption is required because there is very little battery power available on what is, essentially, a disposable patch. Low power also facilitates low current leakage, an important feature of the design. Chemical sensors for detecting blood glucose, for example, need to be biased at very low voltages because the current levels which the chip is trying to measure are in the nano and picoamp range. If the circuit generates its own leakage, then it creates the potential for a false reading.

Managing leakage

Realising a chip that draws just 2.5mA when communicating has required Toumaz to embark on custom hardware design – and managing leakage has been a significant challenge.

Dr Alison Burdett, Toumaz' director of technology, explains the implications of working with such a low power design. "We are working with transistors biased at non traditional power levels – they are actually below the threshold at which you would consider a transistor to be on. When you bias transistors at very low levels, they tend to have large offsets and mismatches and the resulting circuit performance is quite lousy. So we used the embedded digital processor to implement a lot of on chip automatic calibration. These routines tend to fire up on start up, do the calibration and then go back to sleep."

An implication of all this low power circuitry is the potential for interference between the digital and analogue domains. Says Dr Burdett: "Because the analogue signals are working at incredibly low voltages and currents and our digital circuits aren't being clocked at hundreds of megahertz, crosstalk is a real issue." The ability to simulate – sometimes down to the individual transistor level in high risk circuit blocks – was imperative, yet

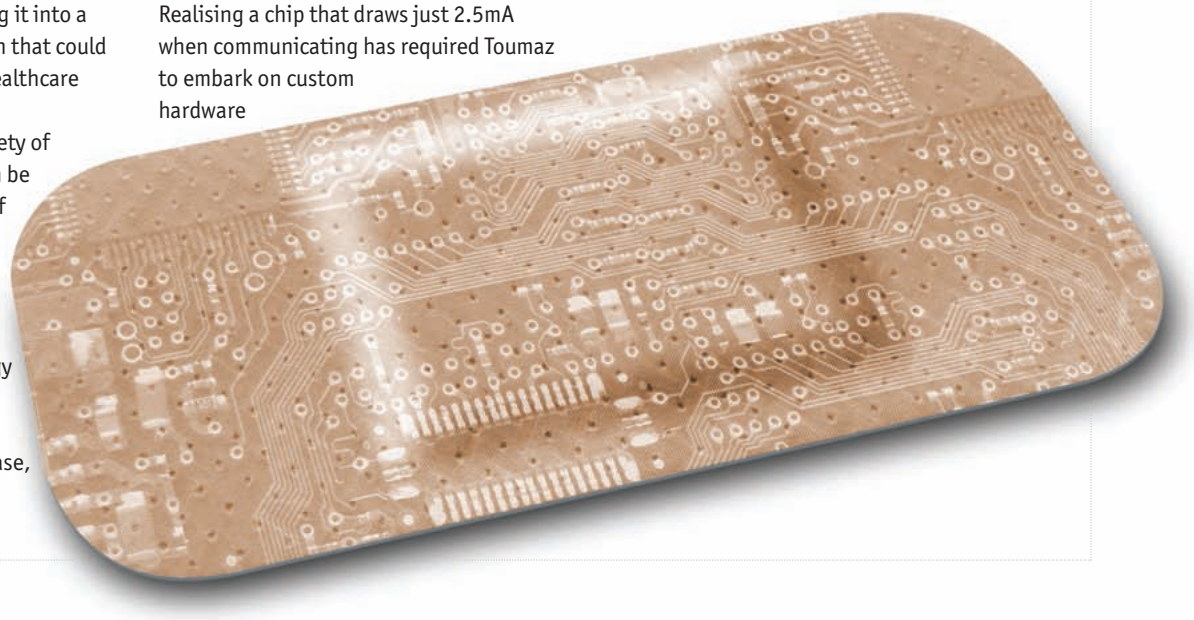
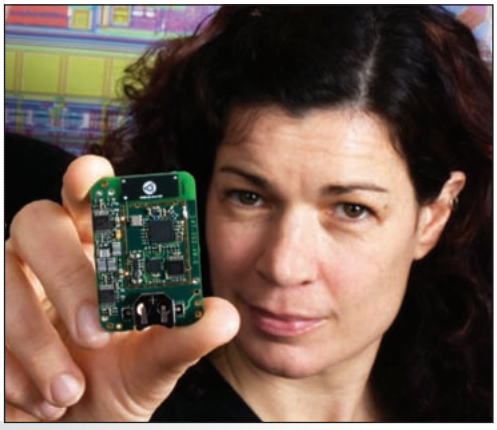


Illustration: Jürgen Ziewe

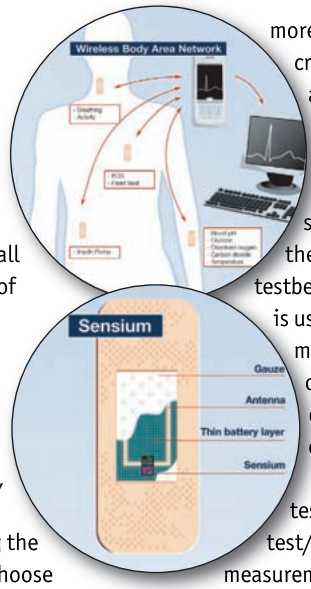
Toumaz couldn't rely on standard simulation methods. As Dr Burdett notes: "Our transistors are biased for weak inversion, so it's not a normal simulation regime – we needed to be able to verify the simulation models themselves."

A simulation challenge

Dr Burdett infers that Sensium had already pushed the limits of traditional simulation. "After verifying the analogue block in an analogue transistor level simulator, such as Spice or Spectre, and then verifying your digital circuitry in a digital simulator, be it Vhdl or Verilog, you go on to verify the top level connectivity, or behavioural level verification. So you can verify, for example, that pin 1 of the digital is connected to the appropriate analogue connector. However, what's really needed is functional verification, where you are verifying the analogue and digital functions together."



Toumaz used Cadence's Analog Design Environment (ADE) to set up structured simulations of the blocks across a range of environmental conditions. ADE is a single verification environment that incorporates test benches, simulation and measurement. The software tool is available in three versions – L, XL and GXL – catering for basic design creation and implementation through to meeting the needs of those creating manufacturing readied designs.



Notes Robert Schweiger, Cadence's field platform marketing director EMEA for custom ics: "ADE L supports all our simulators that are part of MMSIM. No matter which simulator is used, the designer always sees the same user interface when setting up the simulation. Within the ADE environment, you can switch between simulators without changing the testbench, allowing you to choose the right simulator for the right simulation task."

Dr Burdett concurs, saying that when you are wondering about how one block interacts with another, it is as simple as switching in and out of the views you want and running the simulation.

In terms of verification, the hierarchy editor feature makes the process of testing more efficient, and potentially more rigorous, because it creates testbenches automatically. Dr Burdett recounts that the hierarchy editor within ADE enables the design team to access a schematic representation of the chip from which a top level testbench can be generated. This is used as a sort of 'golden model', so you avoid relying on the whims of individual designers drawing up their own testbenches.

Schweiger points out that testbench set up, test/simulation plans and measurements can be modified and reused – facilitating design reuse best practice. Dr Burdett also notes that different people or teams are often responsible for different parts of a chip. For example, in Sensium's case, there is the sensor interface, the digital control block and a wireless receiver. "A common testbench is a necessity for a circuit of this complexity. When a chip is being built up, a testbench is needed for every new level and each new testbench introduces a potential source of error."

Whilst it was already standard practice within Toumaz for the analogue designer to verify the associated digital block and vice versa, Cadence's mixed signal engine AMSDesigner, which offers schematic or hdly based models, assisted that process.

Comments Dr Burdett: "I don't think it would have been possible to design this chip before real mixed signal tools were available." Whilst you might have expected that test chips would have been necessary, Toumaz went straight to silicon. Whilst Dr Burdett estimates the design team spent about six weeks running all the top level simulations, she feels the time was well spent. "If we had encountered a bug at metal fix, then another tape out would have been required. Manual debug might take four weeks, a set of correct masks could then take another four weeks to make – you could be looking at 12 weeks of extra design time alone." ■

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