DATASHEET

VIRTUOSO CHIP EDITOR

Cadence® Virtuoso® Chip Editor is the centerpiece of the Virtuoso custom design platform's full-chip integration component. It provides high-performance editing for full-chip finishing tasks and can handle even your largest designs. Virtuoso Chip Editor is fully interoperable with the Cadence Encounter® digital IC design platform and it leverages the industry-standard Virtuoso Layout Editor environment and infrastructure for layout productivity when you need it most—at tapeout.

THE VIRTUOSO CUSTOM DESIGN PLATFORM

When design objectives dictate manipulating precise analog quantities—voltages, currents, charges, and continuous ratios of parameter values such as resistance and capacitance—companies turn to custom design. Full-custom design maximizes performance while minimizing area and power. However, it requires significant handcrafting by a select set of engineers with very high skill levels. In addition, custom analog circuits are more sensitive to physical effects, which are exacerbated at new, nanometer process nodes.

The Virtuoso custom design platform accelerates the design of custom ICs across various process nodes. By selectively automating aspects of custom analog design and providing advanced technologies integrated on a common database, it allows engineers to focus on precision crafting their designs—without sacrificing creativity to repetitive manual tasks.

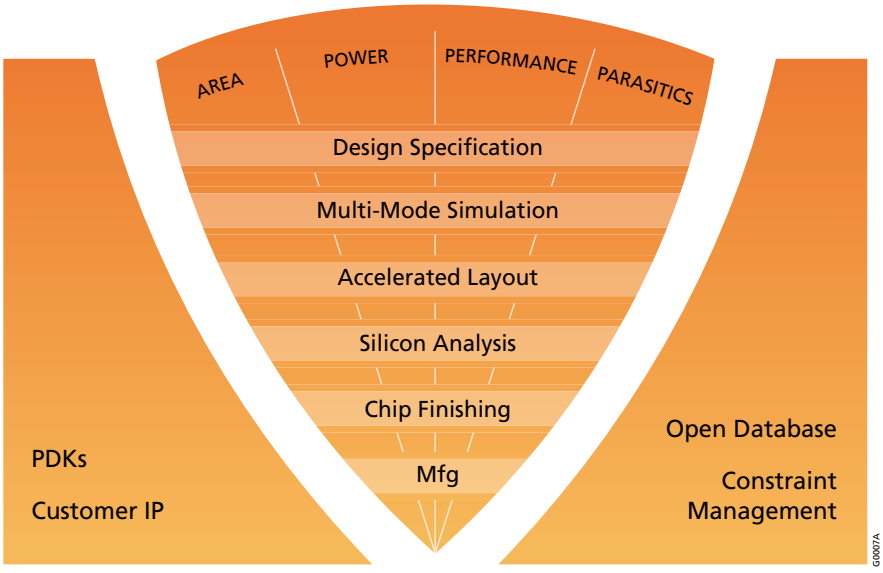

Figure 1: All components of the Virtuoso platform work together to support fast, silicon-accurate differentiated custom silicon

cadence™

VIRTUOSO CHIP EDITOR

Virtuoso Chip Editor combines the high performance and high capacity of OpenAccess with the industry-standard Virtuoso Layout Editor to provide next-generation chip finishing for today's and tomorrow's largest, most complex chip designs. Virtuoso Chip Editor provides chip-planning capabilities, SKILL access, connectivity awareness, and design-rule–driven editing functions that create a chip-finishing solution for complex digital and mixed-signal designs. It is fully interoperable with the Cadence SoC Encounter™ system and provides a seamless roundtrip editing flow for large digital designs *(see Figure 2)*.

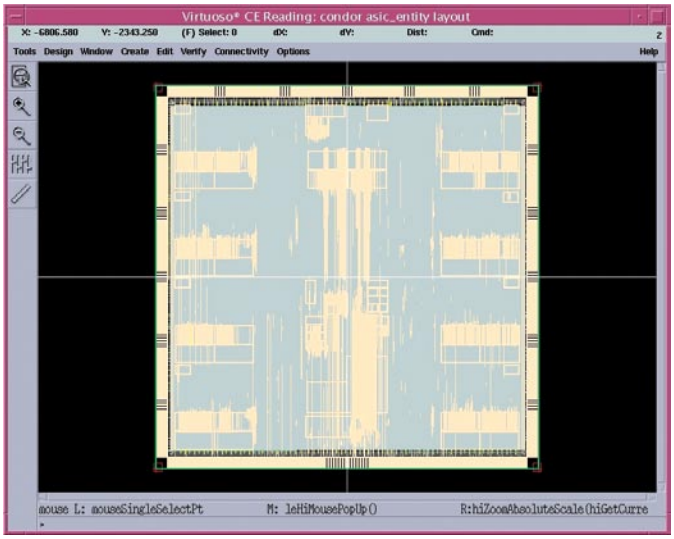

Figure 2: Virtuoso Chip Editor handles the largest designs of today and tomorrow

BENEFITS

- Reduces time to market with increased layout productivity
- Provides high performance and high capacity to handle even the largest designs
- Minimizes training requirements by retaining the look and feel of Virtuoso Layout Editor
- Expedites ECO flow for complex digital and mixed-signal designs through roundtrip editing with the SoC Encounter system
- Reduces the design cycle by providing chip-planning capabilities and minimizing data translation steps

FEATURES

PROFORMANCE GAINS

Virtuoso Chip Editor facilitates your chip tapeout process by reducing the time needed to produce GDSII. XSTREAM reads and writes from the native OpenAccess database at speeds up to 20x faster than other commercially available translators. Interactive tasks that usually take minutes now take less than a second to complete, thanks to new algorithms tuned to full-chip needs. And with OpenAccess, data from many industry-leading physical design tools help eliminate tedious translation steps to save precious time and minimize missteps. The tapeout stage that ordinarily lasts for weeks now takes only days.

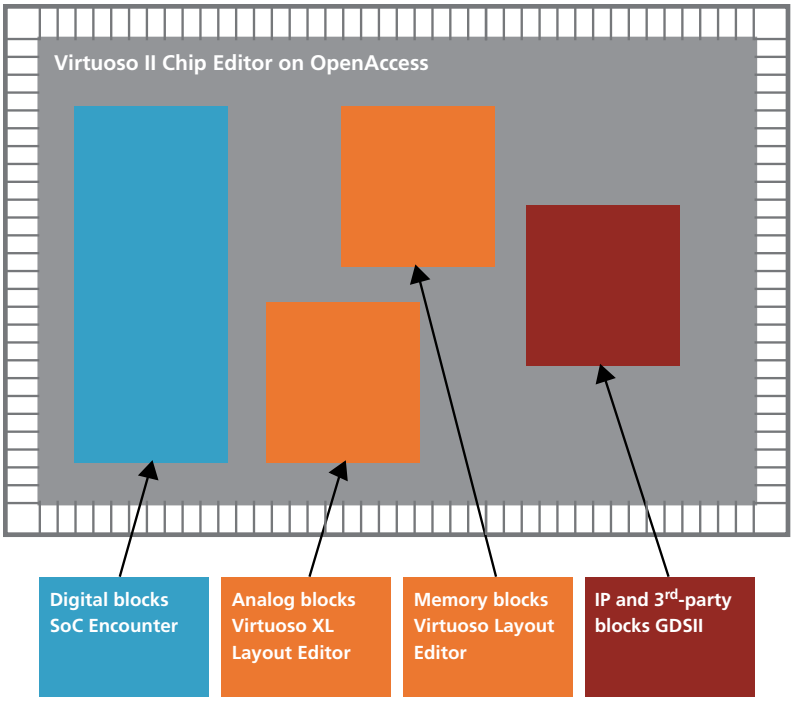

Figure 3: Virtuoso Chip Editor automates chip-finishing tasks

CAPACITY GAINS

Today's designs are pushing the limits of database capacity. But with industry-standard OpenAccess supporting multi-gigabyte files and large virtual memory requirements, Virtuoso Chip Editor efficiently handles your design needs of today and of the future, with space of 3x or more to spare than in other databases.

DESIGN AUTOMATION

Virtuoso Chip Editor responds to the demands for higher productivity of large, complex designs by offering automation technology specifically tuned to chip-finishing tasks for efficient design completion. The editing environment is connectivity-aware and design-rule–driven to help you avoid common mistakes such as inadvertently introducing power and ground shorts. Tuned to OpenAccess for high performance,

Virtuoso Chip Editor also expedites full-chip editing tasks. Critical tapeout tasks that used to take hours now take minutes, shrinking the final tapeout stage from weeks to days.

DFII INFRASTRUCTURE

Virtuoso Chip Editor keeps the look and feel of the industry-standard Virtuoso family of layout tools, saving you time and money spent on training and ramping up. More than 99% of your existing SKILL code can be re-used directly, leveraging your legacy designs and methodologies. Virtuoso Chip Editor is compatible with other DFII tools ported to OpenAccess, which smooths out your design flow and gets your chip out fast.

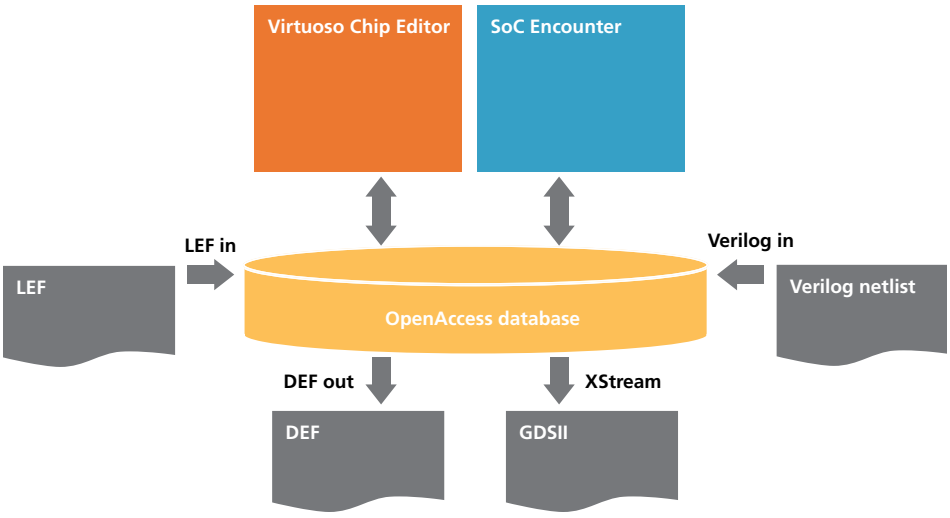

Figure 4: ECO flow between Virtuoso Chip Editor and the SoC Encounter system

SPECIFICATIONS

CHIP FINISHING

- Complete physical design hierarchy support
- Connectivity awareness
- Design-rule–driven editing environment with user-controlled settings (mode of operation, visual feedback)
- OpenAccess database
- SKILL support for OpenAccess objects
- Full suite of Virtuoso Layout Editor commands
- XSTREAM GDSII data translator

DESIGN INPUTS

- OpenAccess data objects
- GDSII
- Virtuoso DFII layout data
- LEF/DEF

DESIGN OUTPUTS

- OpenAccess data objects
- GDSII
- LEF/DEF

PLATFORM/OS

- Sun/Solaris
- HP-UX
- IBM AIX
- Linux

CADENCE SERVICES AND SUPPORT

- Customer-focused solutions that increase ROI, reduce risk, and achieve your design goals faster
  - Collaborative approach and design infrastructure—virtual teaming
  - Proven methodology and flow tuned to your design environment
  - Design and EDA implementation expertise
- Product and flow training to fit your needs and preferred learning style
  - Over 80 instructor-led courses—certified instructors, real-world experience
  - More than 25 Internet Learning Series (iLS) online courses
- Cadence customer support that keeps your design team productive
  - Cadence applications engineers provide technical assistance
  - SourceLink® online support gives you access to software updates, technical documentation, and more—24 hours a day, seven days a week

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