cadence®

Virtuoso Custom Design Platform GXL

The Cadence® Virtuoso® custom design platform is the industry's leading design system for complete front-to-back analog, RF, mixed-signal, and custom digital design. The GXL tier comprises the platform's most advanced configuration of design and analysis technologies, including expanded physical design capabilities and an enhanced simulation environment.

Virtuoso Custom Design Platform GXL

The Virtuoso Analog Design Environment GXL is designed to help users create manufacturing-robust designs. It gives designers access to a new parasitic estimation and comparison flow and optimization algorithms that help to center a design better for yield improvement and advanced matching and sensitivity analyses. This makes it possible to completely explore the design for problem areas. In addition, it incorporates the same advanced custom IC environment used within the Cadence Allegro® platform for creating system-in-package (SiP) designs.

As the high-end custom block authoring physical layout tool for the Virtuoso platform, Virtuoso Layout Suite GXL supports custom digital, mixed-signal and analog designs at the device, cell, and block levels. These accelerated features provide advanced automation to accelerate custom block authoring. It includes capabilities for device generation and editing, block floorplanning, automatic placement, and interactive routing.

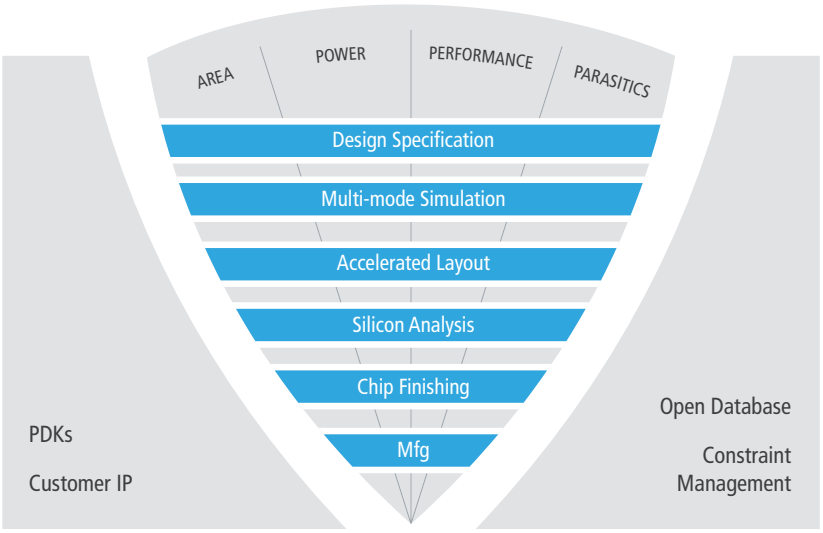

Figure 1: All components of the Virtuoso platform work together to support fast, silicon-accurate differentiated custom silicon

Driven by a comprehensive analog constraint capture and management system, Virtuoso Layout Suite GXL makes design reuse, engineering change, retargeting, and process migration possible. It uses unique placement and routing engines to automatically or interactively generate and optimize device geometry, place devices (adhering to constraints) within a cell footprint, and subsequently complete the layout interconnect routing.

Benefits

- Accelerated block authoring through connectivity-driven features and flow, schematic or netlist. Also promotes correct-by-construction LVS correct layout to reduce verification iterations
- Increased productivity and design quality with constraint- and design-rule-driven features to automatically ensure design and process correctness in real time
- Simplification and optimization of device generation using a new menu-driven QuickCell feature or the standard SKILL programmable parameterized cells
- Efficient planning, placement and routing of large block designs with custom floorplanning, automatic placement, and advanced interactive routing features
- Enhanced analog design team productivity gains–up to 10x over manual methods
- Unique support for meeting new performance specifications, and for handling design reuse, technology migration, and ECOs
- Advanced optimization algorithms improve design centering and yield
- Built-in parasitic estimation and comparison flow help to quickly identify severe parasitics inside the design

Features

Parasitic resimulation flow

Users can place parasitic estimates onto their schematics. These are then translated into wire constraints, which can prompt a layout person that certain nets are critical and their length and width should be minimized to minimize parasitics introduced into the system. Post-extraction, the parasitic estimates can be quickly compared to the extracted parasitics to find trouble spots within the design.

Design for yield flow

Designers can use a series of both global and local optimization methods to center their design values to help maximize yield. This optimizes the parametric yield of circuits by extrapolating the statistical distribution up to six sigma margins.

Advanced layout automation for simplified and optimized block authoring

Virtuoso Layout Suite GXL simplifies and optimizes block authoring with advanced layout automation features that leverage the design-rule–driven functions and flow of the Virtuoso platform. Menu-driven parameterized cells (QCells) or SKILL programmable parameterized cells (Pcells) simplify and optimize device generation and editing. Floorplanning and automatic placement simplifies and optimizes the design planning and location of devices. Advanced shape-based constraint and design-rule-driven routing simplifies and optimizes the tedious interconnect task.

Automatic placement, routing and editing

The GXL placement engine places devices for density, performance, and precision while maintaining symmetries and matching. Device generators produce geometry for complex devices with varying aspect ratios (variants), and then the placer explores these device variants for better packing. Similarly, the placer can optimize the cell footprint to accommodate the cell contents. Floating pins are placed to achieve optimal signal flow and proper spacing is reserved for wide wires. While optimizing latchup, the placer merges wells and creates guard rings—all automatically and with initial constraints respected throughout the placement process.

The GXL routing engine optimizes wiring while adhering to the constraints specified in the Constraint Editor. The router handles arbitrary width and spacing constraints as well as known cross-talk problems. It further supports routing of self-symmetric nets to achieve balanced routing for structures such as T-nets. Also included is support for partially symmetric nets—users can choose to route the critical segments of their nets in a symmetric and highly matched form, while letting the router choose the shortest path for the non-critical net segments.

The interactive editing mode allows designers to move and align devices and change their orientation and shape. Changes to devices automatically regenerate any associated wells or guard rings. Real-time DRC ensures layout quality. Designers can reroute nets and fix the location of critical wires. When the routing of one net is modified, any symmetric nets mirror the new path. As always, the layout synthesis engine respects constraints throughout the routing process.

Precision device generation and layout synthesis

Virtoso platform GXL provides several options for generating the individual devices that are to be used by the placer. It supports Pcells (including ROD), the user's proprietary cells, and even legacy GDSII layouts imported as subcells. For more complex devices, the use of one of the precision generators (Modgens) is recommended. Complex quad-FETs, interdigitated and matched FET arrays and highly matched precise passives are supported. Modgens provide the ability to map several devices to one complex group and then edit the whole arrangement easily. Virtuoso platform GXL also provides a comprehensive layout synthesis engine that generates and optimizes device geometry, cell foot print, device placement and wire routing as guided by the analog constraints for the design (see Figures 2 and 3)

Specifications

Layout creation and editing

- Interactive Pick-From-Schematic or automated Gen-From-Source device selection

- Menu-driven QCell (QuickCell) or SKILL programmable automated device generation
- ExpressPcell mechanism to speed up evaluation of parameterized cells and make them more interoperable with third-party tools
- Automated device editing, including abutment, pin permutation, folding, chaining, and cloning
- Menu-driven or programmable multi-part path (MPP) feature for guard rings, slotting, etc.
- Design-rule driven-editing with real-time notification or enforcement of process rules
- Dynamic measurement
- Constraint-driven specification, management, and real-time notification or enforcement
- Block floorplanning with support rectilinear blocks, pin optimization, and template support
- Automatic constraint- and design-rule-driven placement of pins, devices, cells, and blocks
- Advanced shape-based constraint and design-rule-driven interactive routing
- Bi-directional interfacing to Virtuoso Schematic Editor, Cadence Chip Assembly router and the Cadence Space-based Router
- ECO support
- Virtuoso Layout Migration integrated into Virtuoso Layout Suite GXL
- Legacy non-connectivity design importing and connectivity mapping
- Cadence Diva® and Cadence Assura® physical verification support
- Comprehensive device and cell support
  - All analog cells including opamps, charge pumps, bandgaps, comparators, VCOs, regulators and others in technology portable manner. Provides support for ADCs, PLLs, DLLs and others
  - Supports Pcells including ROD, proprietary cells, and legacy GDSII layouts

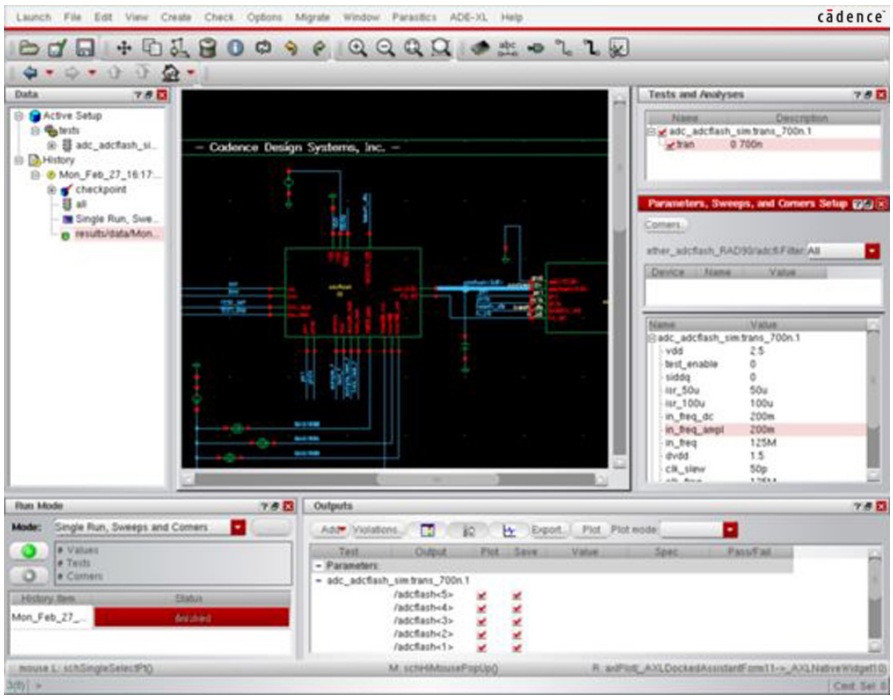

Figure 2: Virtuoso Analog Design Environment GXL

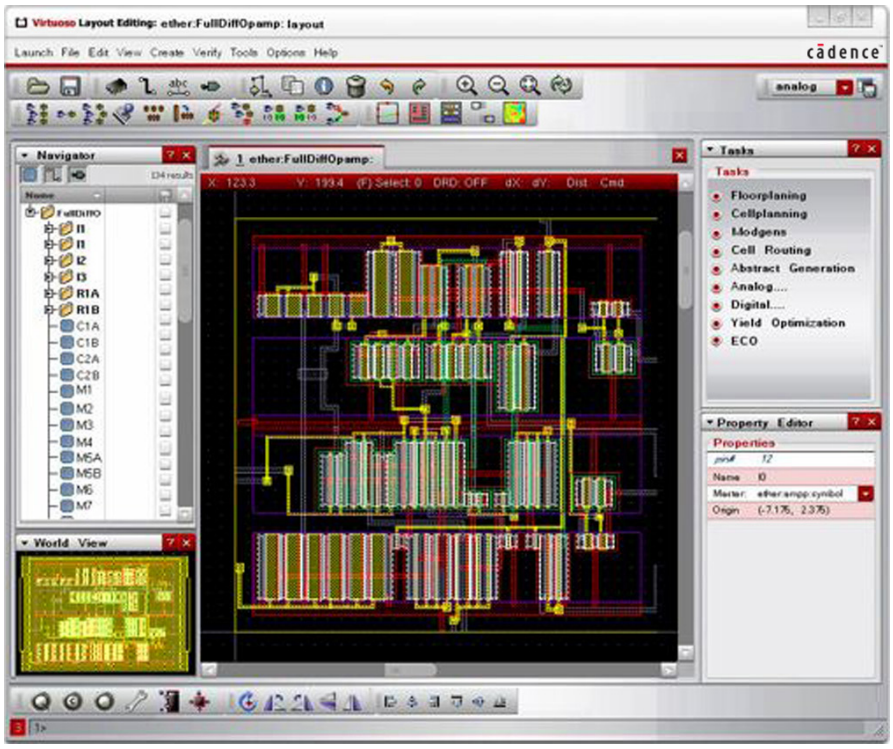

Figure 3: Virtuoso Layout Suite GXL

  - Complex quad-FETs, interdigitated, matched FET arrays and matched passives
  - Supports guard rings, dummy devices wells, and mulit-part paths

- Comprehensive integration
  - Cadence DFII library structure captures constraints, devices, parameters, and connectivity
  - Full compatibility with Virtuoso XL Layout Editor connectivity model
  - Includes technology set-up wizard for fast set-up of a new processes
  - Tightly coupled ECO flow

- Automatic and interactive capabilities
  - Automatic device and device array generation
  - Automatic device placement, including symmetry and matching
  - Automatic routing with symmetry and cross-talk avoidance
  - Move, align and modify devices
  - Interactive routing with symmetric update
  - Real-time design rule and constraint checking

Schematic and simulation environment

- Virtuoso Schematic Editor or netlist-driven hierarchical layout

- New analog schematic generator to convert netlists into schematics

- Simulation environment extensions
  - Inherits all features and functionality from Virtuoso Analog Design Environment XL
  - Tools for comparing and fixing design parasitics
  - Local and Global Optimization to improve design yield and design centering
  - Connections to Allegro platform to enable SiP design
  - Design characterization and modeling features to create Verilog A models
  - Sensitivity and Matching analyses

Virtuoso Custom Design Platform GXL Features

	Virtuoso Analog Design Environment	Virtuoso Layout Suite GXL
New Common Cockpit	X	X
New Icon Style	X	X
Multi-Tab Support	X	X
Bookmarks and History	X	X
Updated Pulldown Menus	X	X
Window Config Support	X	X
World View Assistant	X	X
Search Assistant	X	X
Property Editor Assistant		X
Navigator Assistant		X
Contraint Browser		X
Design Explorer		X
Single Testbench	X	
Simple Parametric Analysis	X	
Device Checking	X	
Global Variable Support	X	
Updated Wavescan	X	
New Calculator	X	
Simulation Support: Virtuoso Multi-mode Simulation, HSPICE	X	
Circuit Optimization	X	
Behavioral Model Generation	X	
Parasitic Resimulation	X	
Yield Analysis	X	
Mismatch/Sensitivity Analysis	X	
SiP Support	X	
Basic Polygon Editing		X
QCells		X
DRD Editing		X
A & D Device Placer		X
ModGens		X
Cell Planning		X
Chip Assembly Router		X
Floorplanning		X
Cell Block Placer		X
Layout Optimization		X
Space-Based Router		X

Design inputs

- SKILL
- STREAM format
- OpenAccess database
- Virtuoso Schematic Editor L or XL
- CDL and SPICE netlist format
- Virtuoso Chip Assembly Router database format

Design outputs

- OpenAccess database
- SKILL
- STREAM format

Platform/OS

- Sun/Solaris
- HP-UX
- IBM AIX
- LINUX

Third-party support

- SKILL-based tools and functions
- OpenAccess tools and functions
- Process design kits (Please reference the Cadence Virtuoso PDK datasheet for more information)

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

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