Cadence OrCAD Signal Explorer

Pre- and post-route topology exploration and signal integrity analysis

Cadence® OrCAD® Signal Explorer helps engineers address signal integrity issues throughout the design process from the conceptual schematic through placement and final routing. It enables pre- and post-route topology exploration, signal analysis, and validation, allowing designers to increase circuit reliability and drive known-good interconnect requirements throughout the PCB design flow.

Increasing design density, complexity, and faster edge rates create a multitude of signal integrity issues, which can lead to time-consuming and frustrating simulate-fix-simulate iterations and increased production costs. Cadence OrCAD Signal Explorer helps engineers address these issues throughout the design process—from the very beginning of the cycle through placement and final routing.

The same signal integrity issues increase the need for an integrated design flow that enables designers to easily perform post-layout extraction and verification of complex PCB interconnect. An integrated design and analysis environment eliminates the need to translate design databases to run simulations and analysis. Seamless integration with Cadence OrCAD PCB Editor eliminates database conversion and possible translation issues. Engineers can now perform signal integrity analysis or topology exploration at any stage of the design cycle—when the board is partially or fully placed, partially or fully routed, and even when no netlist or PCB database exists.

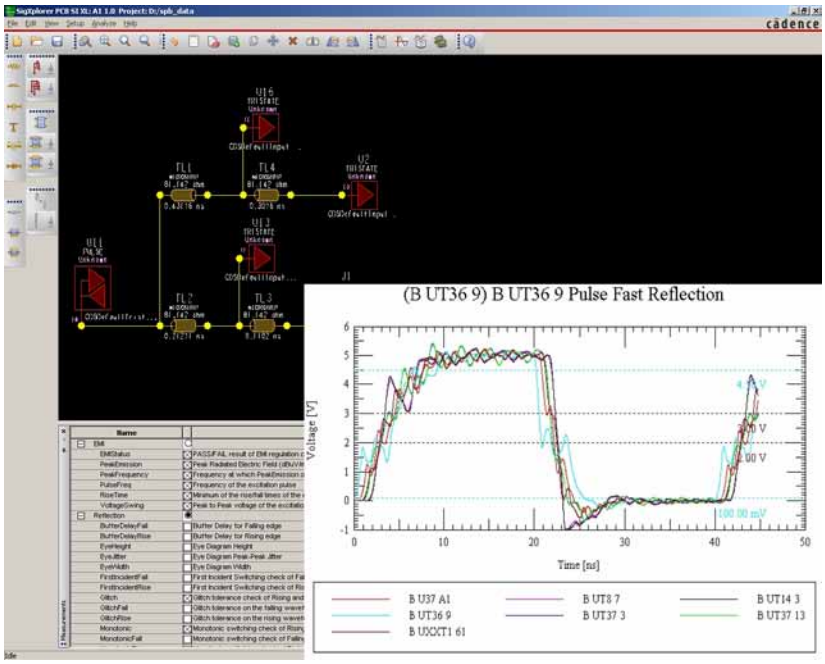

Figure 1: OrCAD Signal Explorer analyzes and validates topologies and interconnect to help minimize potential SI-related issues for fewer re-spins and shorter lab debug time

OrCAD Signal Explorer consists of the Tlsim simulation engine, the SigXplorer topology editor, the SigWave waveform display, translators from other modeling formats, and a library model editing/management subsystem. The IBIS modeling standard is supported natively in addition to Cadence DML (device modeling language) support. A transistor-level model import wizard prepares models to run with the native SPICE simulators.

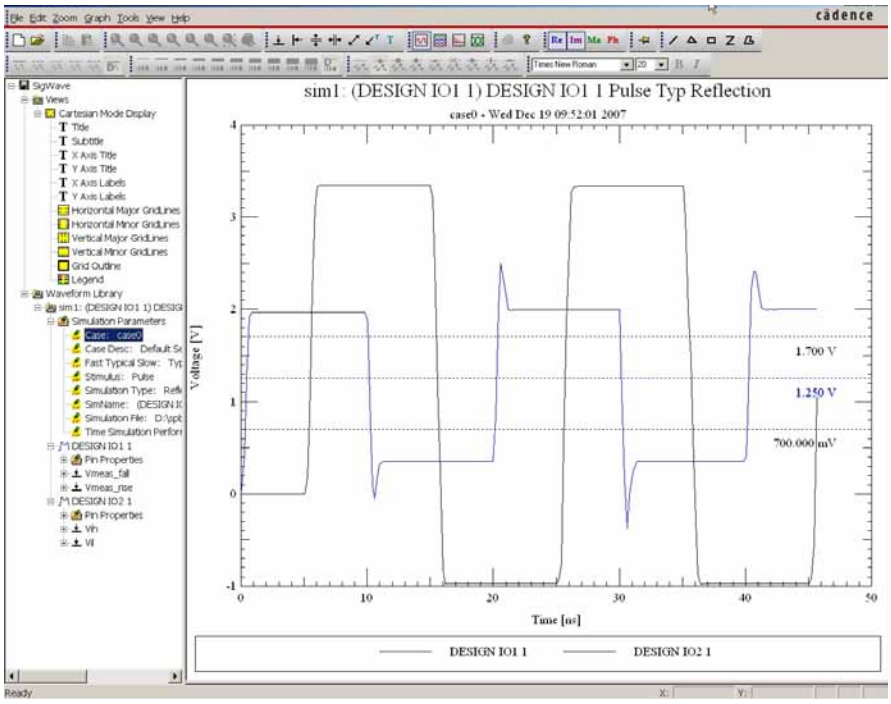

Figure 2: View and analyze simulation results in SigWave

Benefits

- Enables pre- and post-layout signal integrity analysis at any stage of the design cycle, ensuring constraint adherence
- Allows exploration, analysis, and design of interconnect topologies to increase circuit reliability, improve circuit performance, and reduce prototype re-spins
- Eliminates the need to translate design databases to run simulations by importing extracted topologies directly from OrCAD PCB Editor
- Provides an easy-to-use model editing environment that creates, manipulates, and validates a variety of models, quickly improving model/simulation performance

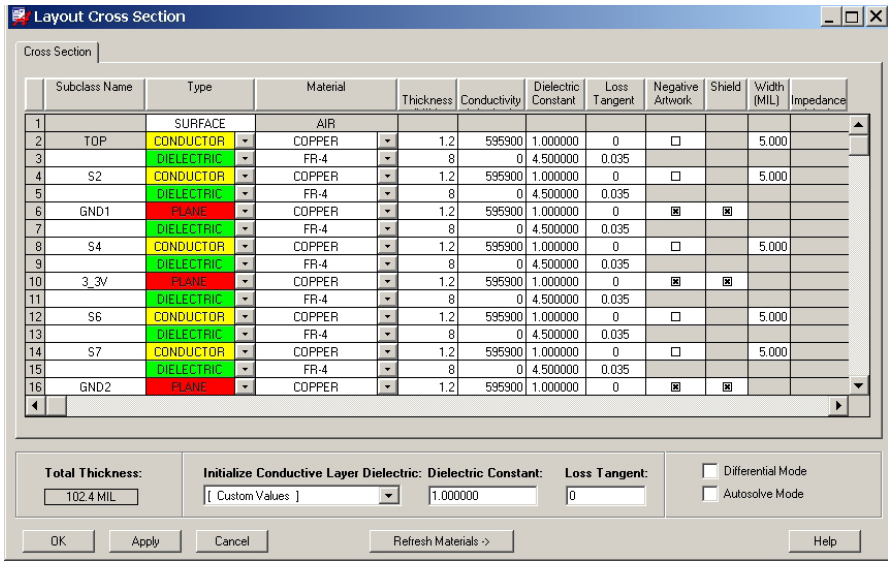

Figure 3: Users can change topologies or stack-up information and perform quick, iterative tradeoffs

Features

Analysis

OrCAD Signal Explorer provides pre- and post-route topology exploration and transmission line analysis. It allows conceptual, pre-design / schematic topology exploration and simulation as well as routed or unrouted board topology extraction and analysis directly from an OrCAD PCB Editor database (.brd).

Pre-layout analysis

Through topology exploration and simulation, critical nets can be planned proactively to minimize signal integrity problems earlier in the design cycle. Using the SigXplorer canvas, topologies are easily defined along with board stack-up requirements and signal termination strategies.

Post-layout analysis

With the ability to extract topologies directly from the PCB design database, simulation on critical nets allows detailed analysis to validate the layout work matches the pre-route requirements. Signals are extracted back into the same canvas that was used to analyze the net, during pre-route, and the routed signal's analysis can be compared to the expected results. If the results do not match, the routed board can be modified and the net re-analyzed.

SigXplorer module

OrCAD Signal Explorer provides an electrical view of the physical interconnect and a simulation cockpit for analysis of critical high-speed signals. Users can explore a net before schematics are created by using the SigXplorer module in a standalone mode. SigXplorer provides various stripline and microstrip models—lossy or lossless—to get started with the exploration. Since OrCAD Signal Explorer integrates seamlessly with OrCAD PCB Editor, users can extract a net in the pre-route or post-route stage right into SigXplorer. Users can then quickly analyze the signal using SPICE-based simulation.

SigWave

The SigWave waveform display can present simulation results in multiple formats. The oscilloscope mode allows the display of individual waveforms on and off, and provides markers for on-screen measurement. The logic analyzer mode presents waveforms alongside one another, so logic behavior and bus transactions are easier to observe. The spectrum analyzer mode displays signal behavior in the frequency domain using one of several FFT techniques. The eye-diagram mode is useful for viewing patterns in long simulation sequences. SigWave also allows import of waveform data directly from various standard test equipment formats as well as from the output formats of popular signal integrity analysis tools.

Model integrity

The Model Integrity module provides an editing environment within OrCAD Signal Explorer that allows the creation, manipulation, and validation of models quickly and easily. This module includes a model browser and syntax checker for models written in IBIS as well as for advanced models written in DML.

OrCAD Signal Explorer accepts device models from a variety of digital modeling formats—including support for the IBIS modeling standard—which means models created by most semiconductor manufacturers can be used. In addition, OrCAD Signal Explorer provides DML, a next-generation modeling language for more complex devices. This flexible macromodeling extension language augments IBIS and allows state-of-the-art I/O functionality to be modeled quickly and accurately.

Simulation environment

The Tlsim simulation engine combines the advantages of traditional SPICE-based structural modeling with the speed of behavioral analysis. It includes an IBIS-style behavioral driver element that models I/O behavior based on the V-I and V-T data provided by behavioral modeling techniques.

By combining both structural and behavioral modeling techniques, Tlsim enables accurate and efficient modeling of complex device behavior. It includes a lossy, frequency-dependent transmission-line model that accurately predicts the distributed behavior of PCB traces up to several gigahertz. An integrated electrical field solver determines the electrical characteristics of routed etch and creates electrical models of PCB vias.

Future-Proof Scalability

Unlike other signal integrity solutions, OrCAD Signal Explorer has the ability to grow with changing exploration and analysis needs and technology challenges. Based on Allegro® SI technology, the OrCAD SI solution provides the security of scalability to meet future challenges easily. Features and technologies are shared across the OrCAD and Allegro product lines. This allows products to be easily upgraded and expanded without the need to translate databases or libraries, learn new applications, or change use models.

Sales, Technical Support, and Training

The OrCAD product line is owned by Cadence Design Systems, Inc., and supported by a worldwide network of Cadence Channel Partners (VARs).

For sales, technical support, or training, contact your local Cadence Channel Partner (VAR). For a complete list of authorized Cadence Channel Partners (VARs), visit www.cadence.com/Alliances/channel_partner

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