APPLICATION NOTE

Obtain S-Parameter Data from the Probe Window

December 2009

OVERVIEW

RF and microwave circuit designers frequently express the input and output characteristics of circuits in terms of scattering parameters (s-parameters). By adding two subcircuits, s-parameter data can be printed to the output file or displayed in the Probe window. The method presented here is qualified for two-port networks, but the concept can be extended for n-port networks.

THEORY

S-parameters measure the ratio of the incident and reflected signal. The incident signals are defined as *a1* and *a2*. The reflected signals are defined as *b1* and *b2*. The incident and reflected signals are related to voltages and currents at ports 1 and 2 by

$$a1 = \frac{V1 + Z_0 I1}{2\sqrt{Z}} \qquad (1)$$

$$b1 = \frac{V1 - Z_0 I1}{2\sqrt{Z}} \qquad (2)$$

$$a2 = \frac{V2 + Z_0 I2}{2\sqrt{Z}} \qquad (3)$$

$$b2 = \frac{V2 - Z_0 I2}{2\sqrt{Z}} \qquad (4)$$

The scattered waves are related to the incident waves by the following set of linear equations:

$$b1 = S_{11} a1 + S_{12} a2 \qquad (5)$$

$$b2 = S_{21} a1 + S_{22} a2 \qquad (6)$$

or, in matrix form as

$$\begin{bmatrix} b1 \\ b2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a1 \\ a2 \end{bmatrix} \qquad (7)$$

The *Sij* coefficients are dimensionless ratios; for most applications, the characteristic impedance of the system, *Z0*, is 50 ohms. *S11* is the input reflection ratio and is defined as the ratio of the input port reflected wave to the input incident wave. If the incident wave at the output, *a2*, is set to zero, then the equations reduce to *b1 = S11a1* and *b2 = S21a1*. Using the defining equations, this reduces to

$$S_{11} = \frac{b1}{a1} = \frac{V1 - Z_0 I1}{V1 + Z_0 I1} = \frac{Z - Z_0}{Z + Z_0} = 2\left(\frac{Z}{Z + Z_0}\right) - 1 \qquad (8)$$

where *V1/I1* is the input impedance *Z*. Similarly, *S21* is the forward transmission ratio and is defined as the ratio *b2/a1*. If the input and output load impedances of the circuit are the same, then *S21* is the voltage measured at the output multiplied by 2. If the incident wave at the input is set to zero, then the equations reduce to *b1 = S12a2* and *b2 = S22a2*.

DEFINING THE SUBSCHEMATICS

To make all of the necessary measurements, two subschematics are required. These subschematics are shown in Figure 1 and Figure 4 and can be created by drawing the schematic in Cadence® OrCAD® Capture and creating a hierarchical part for each. For the purpose of this article, these custom parts are named XMITS and REFLECTS, respectively. See Creating and Editing Parts in the OrCAD Capture User's Guide for reference to creating hierarchical parts.

The XMITS circuit shown in Figure 1 is used to measure the forward, *S21*, and reverse, *S12*, transmission coefficients. Since the output load matches the input load, the transmission coefficients are the output voltage multiplied by 2. The E device, E1, has a gain of 2. The port labeled CKT is used to connect to the external circuit. The port, STR, is a hidden pin (see Figure 2); if it is left unconnected in a schematic, OrCAD Capture will generate a unique net. Alternatively, a specific net can be named for the connection by editing the `PSpiceDefaultNet` attribute value (see Figure 3) for the XMITS part instance; this way, the STR pin will have a known label (s21 in this case) when analyzing simulation results within the Probe window.

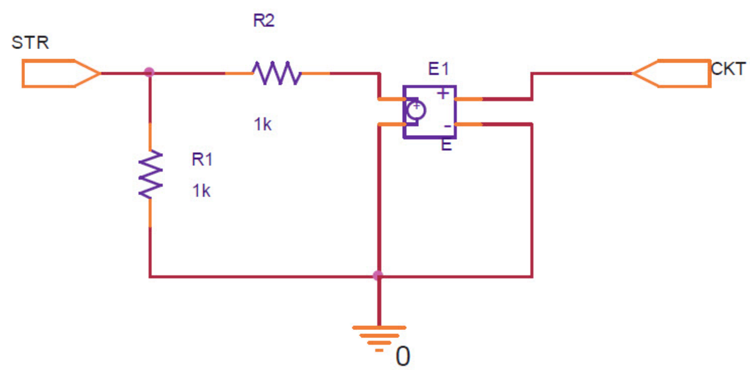

Figure 1: Transmission coefficients measurement subschematic

Figure 2: OrCAD Capture Part for the XMITS subschematic

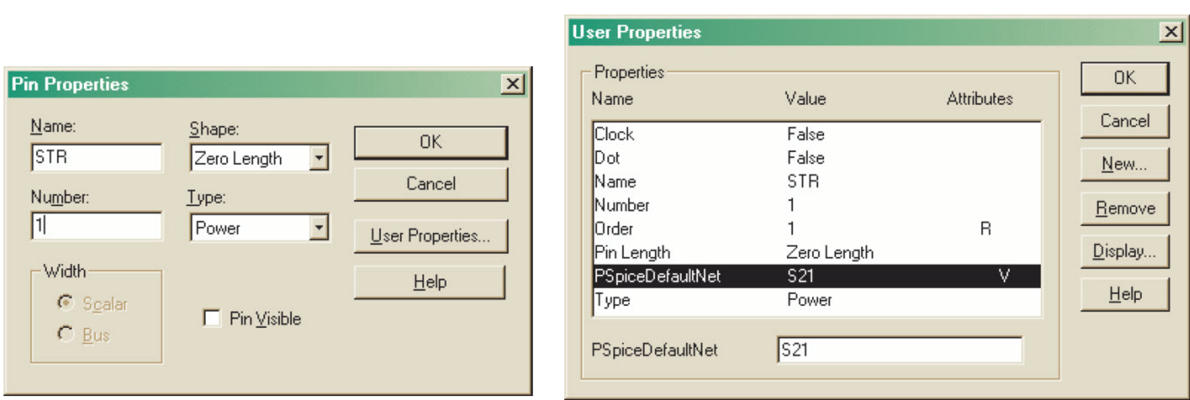

Figure 3: Pin Properties for the XMITS part showing hidden S_TR pin

The REFLECTS circuit shown in Figure 4 is used to measure the input, *S11*, and output, *S22*, reflection coefficients. The reflection coefficients are the input voltage multiplied by 2 minus AC unity. The E device, E1, has a gain of 2. As in the transmission coefficients measurement circuit, the interface pin labeled CKT is used to connect to the external circuit. The pin, SRE, is a hidden pin like STR described above, (see Figure 5). The REFLECTS symbol also has a *DCbias* property. On active circuits, the DC level can be set on voltage source, V1, by changing the *DCbias* property for the REFLECTS part instance in OrCAD Capture. By default, this property is set to zero.

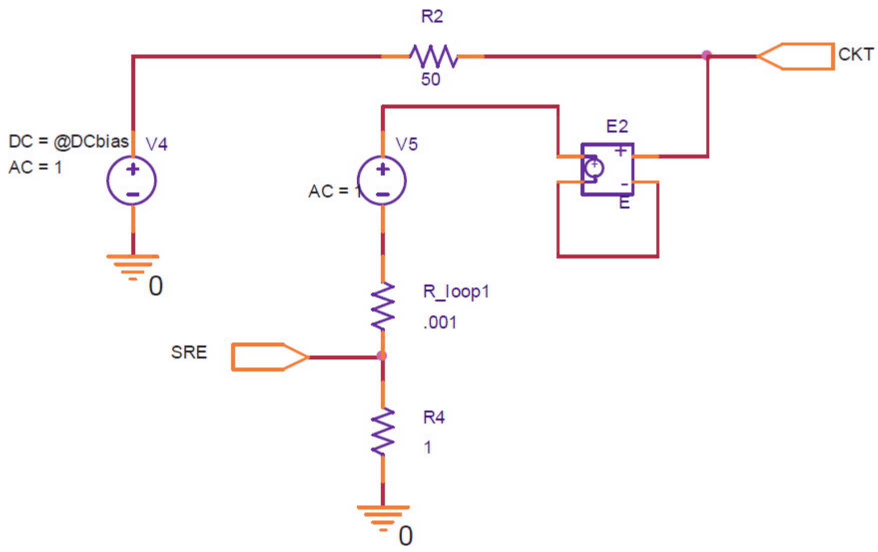

Figure 4: Reflection coefficients measurement subschematic

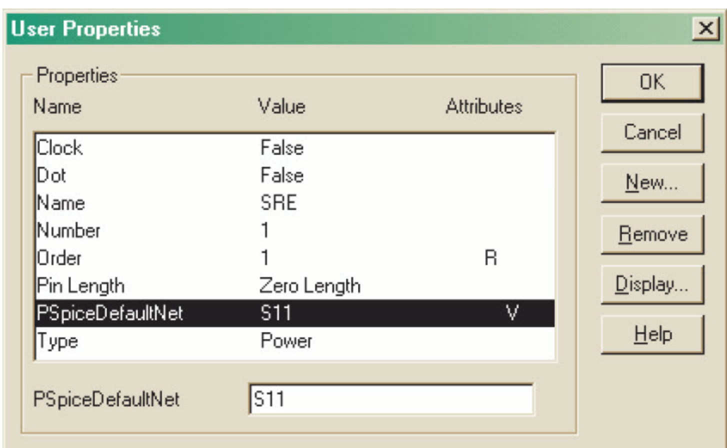

Figure 5: Pin Properties for the Reflects symbol showing hidden S_RE pin

USING THE SUBSCHEMATICS

The subschematics can be used for both passive and active circuits. You can also use the XMIT and REFLECTS symbol which are available in the library 'sparam.olb' attached with the example for this application note. The circuit shown in Figure 6 is a forth-order Butterworth bandpass filter with a center frequency of 250 MHz. The first circuit measures S11 and S21. The second circuit measures S12 and S22. For simulation, the AC analysis settings are 500 linear points from 200 MHz to 350 MHz. The results of the analysis are shown in Figure 7.

Download example file for passive circuit: `passive.zip`

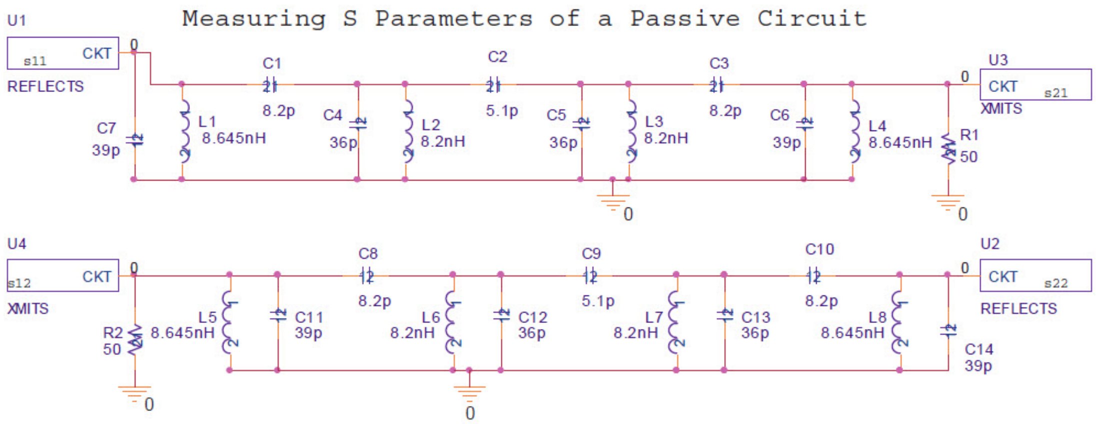

Figure 6: Bandpass filter example

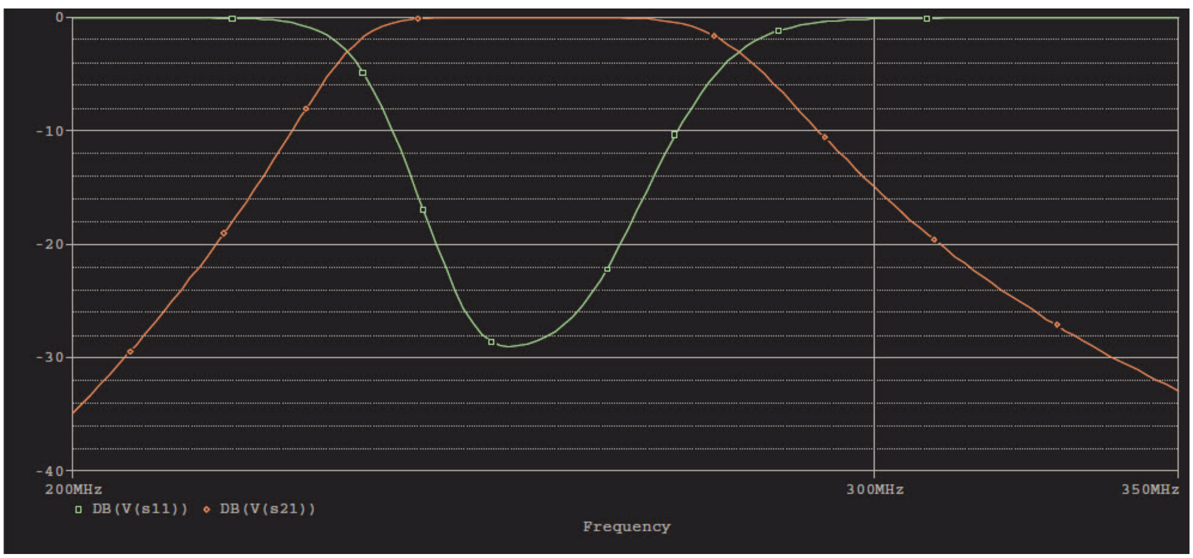

Figure 7: S11 and S21 for Filter Example

It is also possible to measure the *s*-parameters of an active circuit. To illustrate this, we have chosen to measure the *s*-parameters of the RF transistor, MRF5711/MC. Figure 8 shows the circuits for this example. The transistor is biased for a VCE of 6.0 volts and an IC of 5.0 mA. The current is set by the current source at the emitter of the transistor. The DC bias is set by V1 in the circuit that measures *S11* and *S21*, and by the *DCbias* attribute in the reflection measurement subcircuit that measures *S12* and *S22*.

For simulation, the AC analysis settings are 100 points per decade from 200 MHz to 2 GHz. The results shown in Figure 9, Figure 10, and Figure 11 are expressed as magnitude and phase. This is typically the way most manufacturers' data sheets show the *s*-parameters.

Download example file for active circuit: `active_circuit.zip`

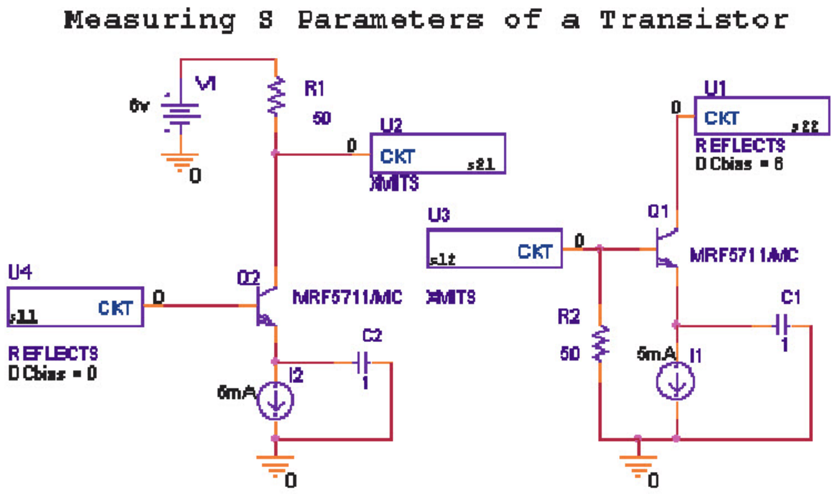

Figure 8: Transistor example

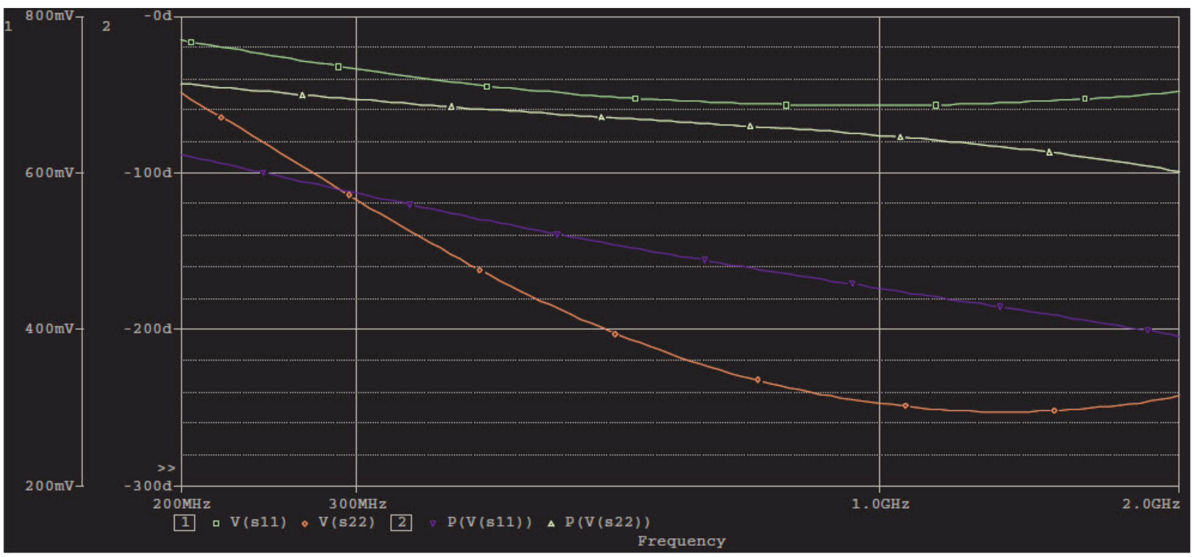

Figure 9: S11 and S22 magnitude and phase

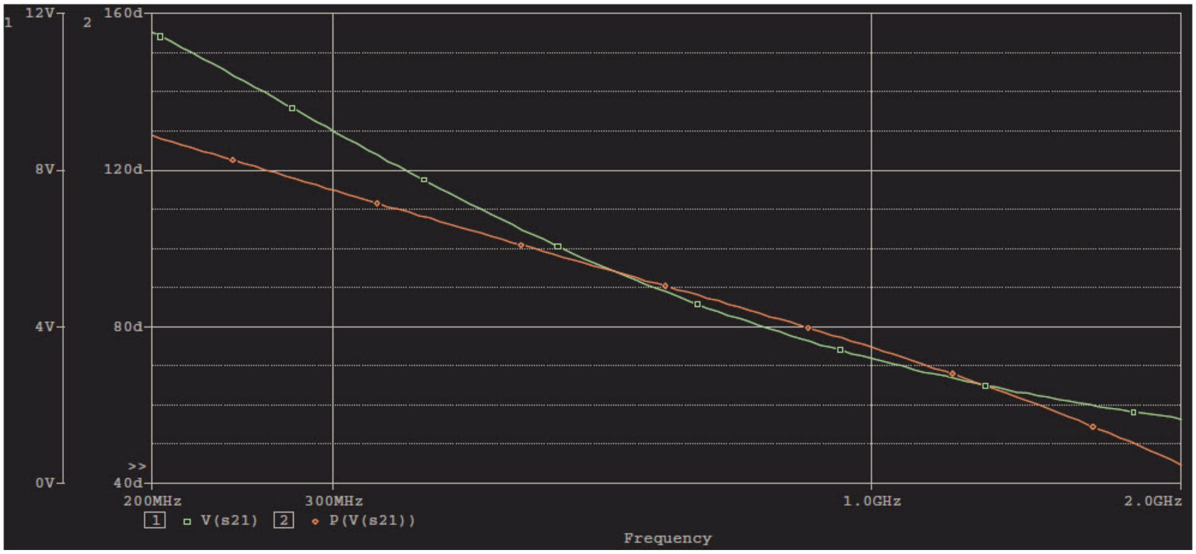

Figure 10: S21 magnitude and phase

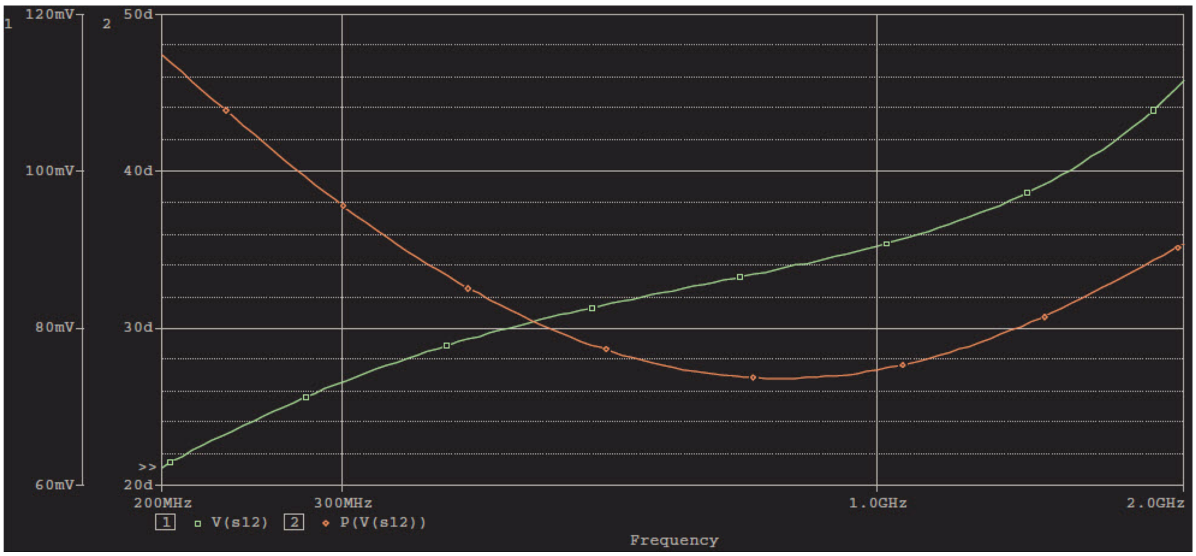

Figure 11: S12 magnitude and phase

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