APPLICATION NOTE

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What Will Digital Worst-Case Timing Simulation Do For You?

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With "digital worst-case timing simulation," you are able to use Cadence® PSpice® A/D to evaluate the timing behavior of your digital and mixed analog/digital designs as a function of component propagation delay tolerances.

Early versions of PSpice allow specification of component delay values (MINimum, TYPical, and MAXimum), and simulation using any one of these delays. With the introduction of the digital worst-case timing capability, you can now run your design in true "worst-case" mode, which simulates all devices with the full range of MIN through MAX delays.

```
.model T_BUF UGATE ( ; BUF timing model
+ TPLHMN=5ns TPLHTY=8ns TPLHMX=10ns
+ TPHLMN=9ns TPHLTY=10ns TPHLMX=15ns
+ )
```

Component propagation delays are expressed in the .model parameters associated with component types, with -MN, -TY, and -MX suffixes (e.g., **TPLHMN**) representing MINimum, TYPical and MAXimum delay values. Usual practice is to obtain these values from the manufacturer's specification sheets for the components used in your design. In cases where some of these parameters are unspecified, PSpice can establish the missing values by extrapolation. Provided below is an example of MIN and MAX propagation delay specifications for a BUF primitive.

For use with most families of logic, Cadence OrCAD® has simplified the use different timing models with the use of the property of MNTYMXDLY. This property, which can be set on a part by part basis, or on the design as a whole, and allows a simple method of determining the timing models being used in a simulation. The values for MNTYMXDLY are:

Value	Timing Models Used
0	Default for design as defined in the Simulation Profile, Options Gate-level simulations
1	Minimum Delay
2	Typical Delay
3	Maximum Delay
4	Worst Case Analysis

The normal default for each part is MNTYMXDLY=0, while the default setting for the simulation in Options/Gate Level Simulation is MNTYMXDLY=4, so the default timing for digital simulation is Worst Case Timing.

Digital worst-case timing simulation is perhaps best thought of as a tool that can tell you whether or not your digital design will operate as expected, under the worst possible combination of component delay tolerances. In this regard, worst-case is superior to separate MIN and MAX simulations, which rely on observing circuit behavior only at the extremes of specified tolerances. Consider the example in Figure 1: using only d = MIN (MNTYMXDLY=1) propagation delays. The same results would be seen using MNTYMXDLY=3 or MNTYMXDLY=2.

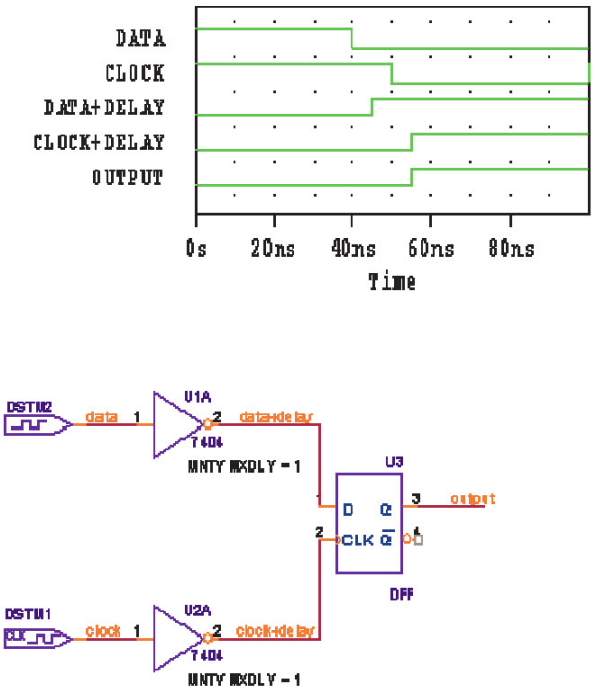

Figure 1: Example of MIN or MAX propagation delay for BUF primitive

Now, seeing that correct behavior is indeed observed at both extremes of the propagation delay range, consider the effects of having one of the components operating "slow" and the other "fast" as shown in Figure 2. Note that the output is now low instead of high!

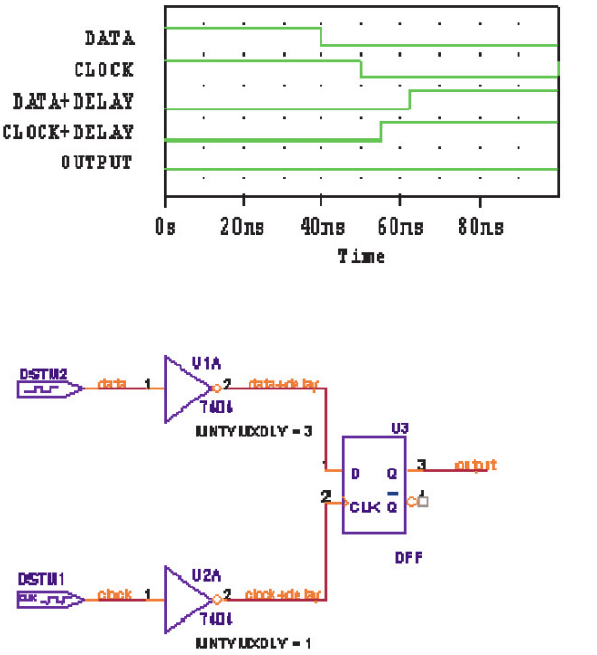

Figure 2: Effects of operation at one set of propagation delay extremes

Digital worst-case timing simulation will help you identify situations such as this, where the timing of signals is critical to the proper operation of the design. In a simple timing simulation (using one of MIN, TYP, or MAX delays), signal propagation through digital devices is normally represented as

"instantaneous" transitions, such as those in the examples above. But during worst-case operation, the effects of individual component delay ranges are propagated throughout the circuit. The "transitions" take both the MIN as well as the MAX delay characteristics of their propagation paths; therefore, transitions may be thought of as "regions of signal ambiguity." This is due to the uncertainty of which delay value (MIN, MAX, or somewhere in between) actually applies to each component used in the design. PSpice represents this type of signal ambiguity with "Rising" (R), and "Falling" (F) logic levels.

The worst-case operation of the previous example is illustrated in Figure 3.

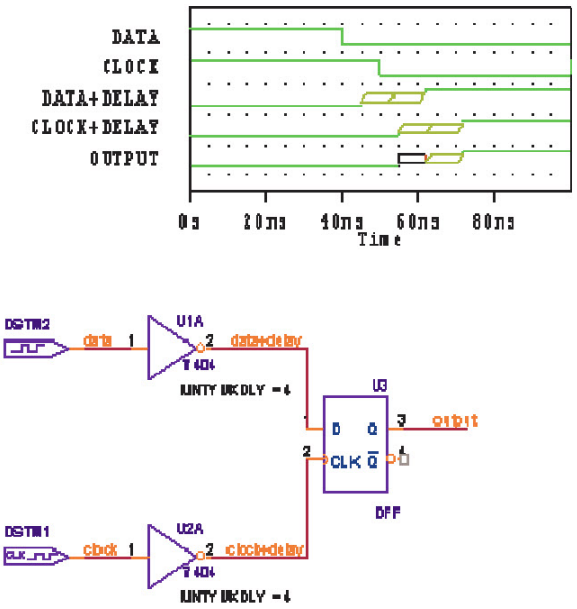

Figure 3: Worst-case timing operation with signal ambiguities

Note that, due to the uncertainty of the arrival time of both the data and the clock signals, a warning is generated by PSpice, and the output is marked as X' (unknown) from 50ns to 60ns. Other tools called "timing verifiers" are sometimes used in the design process to identify problems that are indigenous to circuit definition. They yield analyses that are inherently pattern- *independent*, and very often pessimistic, in the sense that they tend to find more problems than will truly exist. This is due to the fact that they do not consider the actual usage of the circuit under applied stimuli. PSpice does not provide this type of "static" timing verification. Digital worst-case timing simulation, as provided by PSpice, is a pattern-*dependent* mechanism that allows a designer to locate timing problems subject to the constraints of specific applied stimuli.

The PSpice A/D User's Guide, provided with the software package, contains a detailed description of the digital worst-case timing simulation mode, as well as a discussion of application methodology. By using digital worst-case timing simulation as an integral part of your design methodology, you can dramatically improve your chances of producing robust designs that have a high degree of immunity from the effects of varying combinations of individual component tolerances.

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