Ensuring Reliable and Optimal Analog PCB Designs with Allegro AMS Simulator

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1. Introduction

An analog/mixed-signal PCB design that has been functionally verified via basic SPICE simulation is not necessarily optimal in performance, nor is it known to be reliable or of sufficient yield to be worthy of production, because the design components have not been optimized for value, tolerance, and power rating. An integrated environment that allows the user to make the best design tradeoffs throughout the analysis process is needed.

This paper discusses the reasons to further analyze your designs and shows how Allegro AMS Simulator enables designers to develop their products in support of faster time-to-market, higher yield, improved reliability, and with reduced board spins and cost.

2. Previous Work

In the traditional design/simulation flow, a design is iteratively tested at typical values with a SPICE simulator and sent for PCB prototyping or manufacturing once the circuit operates with the intended behavior. This practice of prototyping or manufacturing a design that has merely been functionally verified often causes problems in the real world because it is not fully characterized. Under Harsh operating conditions, for instance, the design can malfunction due to violation of Safe Operating Limits (SOLs) of one or more components in the design. To prevent stress failures such as these, designers tend to make tolerances unnecessarily tight and use devices with high SOLs. This over-designing makes the end product less than optimal in performance and unnecessarily costly.

With traditional simulation tools, there is no facility for the designer to tweak some parameters and immediately determine whether the design still meets the specification, or to modify the specification and see the impact on the parameter values. When multiple specifications must be simultaneously met, there has been no integrated way to solve for the critical parameter values. Use of optimization and sensitivity point tools can help attain design goals, but in absence of a well integrated environment, the results are obtained piecemeal. Additionally, the resulting values may not be practically available.

3. Test Case

Figure 1 shows the test case for this paper. It is basically a one-transistor forward converter with an added flyback winding. The details of the switched-mode power supply (SMPS) are not critical to the subject matter of this paper, but an SMPS was chosen as the test case because it is an increasingly common target for SPICE simulation.

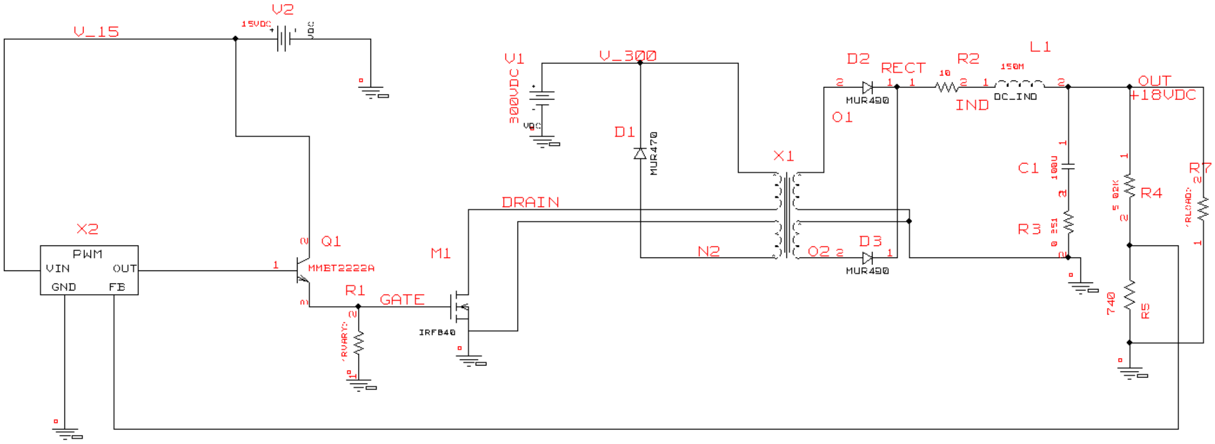


Figure 1 - Schematic diagram of the switched-mode power supply

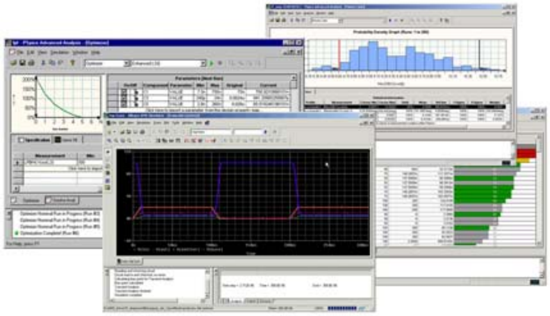
The SMPS schematic was entered using Allegro Design Entry HDL (aka Concept HDL), functionally verified with Allegro AMS Simulator (which included the creation of the transformer model using AMS Simulator’s Magnetic Parts Editor), and then analyzed and optimized using Allegro AMS Simulator Advanced Analysis.

4. Software Used

Schematic entry was performed using Allegro Design Entry HDL and simulation/analysis took place within the Allegro AMS Simulator environment. Below is an introduction to both products.

Allegro AMS Simulator:

Allegro AMS Simulator (Product code PS2200) combines the classic Cadence PSpice A/D simulator with the powerful Advanced Analysis™ tool set. AMS Simulator Advanced Analysis includes tightly integrated facilities for stress analysis, sensitivity, Monte-Carlo, automatic design parameter optimization, and parametric sweep, which make extensive use of *measurements*. These features are detailed below.



- **Measurements**

The concept of *measurements* finds broad use within Allegro AMS Simulator, and especially within the Advanced Analysis tools. Measurements allow a specific behavior or characteristic of a design (such as the -3dB bandwidth of a filter) to be captured into a single numeric value. Limits on these measurement results are then used to implement performance specifications, while the reported values indicate the design's current state.

- **Smoke**

Smoke automatically compares the simulation results from a transient simulation against the stress limits of the devices in the design and displays the stress information using an easy-to-read, color-coded bar graph.

- **Sensitivity**

Sensitivity determines the amount of influence that toleranced parts in the design have on the results of user-defined measurements. Each measurement can have its own simulation profile, and could thus be associated with a transient simulation, AC sweep, etc.

- **Monte Carlo**

Monte Carlo automatically uses the toleranced devices in the design, as well as their distribution types (flat, Gaussian, etc) to predict yield against the design performance specifications (measurements, and their associated limits) that you set.

- **Optimizer**

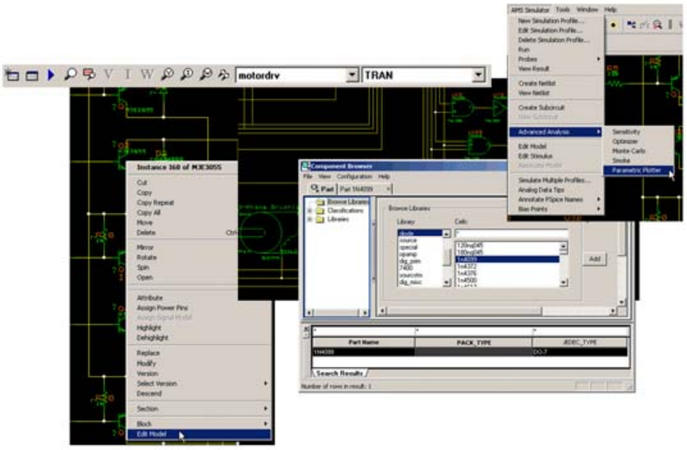
The optimizer allows the engineer to identify component parameters that Advanced Analysis can vary, in order to meet a set of performance specifications. The specifications can be in the form of limits on measurements, or a set of curves (such as gain and phase plots for a filter) to be considered as targets for the optimized design. The difference between the specifications and the current measurement results is the error, which the optimizer attempts to minimize. The optimizer includes a random engine, which will randomly vary the selected component values, yielding a wide range of potential seed points for a follow-up optimization run using one of the more deterministic engines, such as Least Squares (LSQ), for the final result. The random engine circumvents the possibility of optimizing into the wrong local minimum (in error) by determining error values across the entire value space of the components being optimized. The user is then free to pick any of those runs as the starting point (seed) for LSQ optimization.

- **Parametric Plot**

The Parametric Plotter allows you to easily sweep a selection of component parameters (nested) and view their impact on any number of measurements. Families of curves (plots) can also be generated, based on these sweep results.

Allegro Design Entry HDL:

Allegro Design Entry HDL is a complete and scalable solution for the design of PCB schematics. Tightly integrated with Allegro PCB Editor and Allegro Constraint Manager, Allegro Design Entry HDL provides a robust and highly customizable solution for constraint-driven PCB design. It is also completely integrated with Allegro AMS Simulator, which means that a single schematic can simultaneously drive the PCB, signal integrity, and analog/mixed signal analysis flows.



5. Analysis: Who cares?

Functionally verifying your analog/mixed signal design via SPICE simulation is a good thing, but thoroughly analyzing/optimizing it for best performance, reliability and yield should catch the attention of several organizations in your company. Many companies are guilty of a product development flow in which much of the analysis and design optimization is “backloaded”. Stress violations are found after initial product has reached the customer and has failed, yield is determined as product is rolled off of the production line and tested, and improvements/corrections to the design take a back seat to this timeline. This may be the result of the fact that analog and mixed signal design often gets less attention than other product design aspects. It’s not unusual to find that a company invests heavily in signal integrity simulation software for the high-speed digital portion of their product, but neglects the power supply, filters and amplifiers that they might see as cookie-cutter or too simple to need analysis beyond what is already provided in the application notes. Ironically, it is often the assumption by many signal integrity analysis processes that all underlying analog circuitry (e.g. power supply) is operating within specifications for its results to be valid.

Engineering Verification Testing (EVT) and Design Verification Testing (DVT) are too often seen as the primary debugging tools for the design before going to production, but it can easily be argued that even large quantities of tested units will show very little variation in component value and performance relative to their corner cases. Prototypes are often built using the same lots of components from the same manufacturer. It isn’t until the design goes to high volume production that significant shifts in resistor values and substitute components come into play, and the product is showing new behavior. EVT and DVT are essential tools, but are not a substitute for thorough and early circuit analysis.

The reasons that companies lull themselves into taking their analog designs for granted are probably too numerous to count, but costs due to rejected and failed product, extended time to market (shortened product lifespan), and poor performance can be staggering. Those costs can be brought under control by executing timely analysis on your designs in an efficient manner.

Figure 2 below is a table that lists many of the key product quality areas for electronic equipment, their associated tasks, and a mapping to the Allegro AMS Simulator Advanced Analysis tools that have some application to those tasks.

Organization	Tasks	Advanced Analysis Tools
Hardware ENG	WCCA, Electrical Stress Analysis & Derating	Smoke, Optimizer, Sensitivity, Monte Carlo, Parametric Plotter
Hardware QA	WCCA, Electrical Stress Analysis & Derating	Smoke, Sensitivity, Monte Carlo, Parametric Plotter
Reliability ENG	Reliability Prediction Analysis, FMEA	Smoke, Sensitivity, Monte Carlo
Test Dev. ENG	Test Coverage Analysis	Smoke, Sensitivity, Monte Carlo, Parametric Plotter
MFG ENG	Test Process Optimization	Smoke, Sensitivity, Monte Carlo, Parametric Plotter

Figure 2 - Organization/Tasks/Advanced Analysis Tools table

As the table above indicates, Allegro AMS Simulator Advanced Analysis has applicability across a wide range of quality areas, allowing you to “go wide” to the various organizations in your company with Advanced Analysis and the resulting data. In many cases where Advanced Analysis does not complete the picture for a given task, such as reliability/MTBF calculation, it can still provide key data, like the “stress ratios” file (produced by Advanced Analysis Smoke) in tab-delimited form, which can be used by many reliability calculation methods, such as MIL-STD-217, etc. The following is a brief description of each of the tasks listed above, as well as some of their benefits.

Worst Case Circuit Analysis (WCCA)

WCCA is the pre-production analysis of a design for the identification of weaknesses and their impact on its operation. It includes Monte Carlo, Root Sum Squared (+/- 3 sigma), and Extreme Value Analysis (EVA). Benefits include identification of conditions that could lead to immediate or premature failure, and determination of acceptance test modes and parameters.

Failure Modes & Effects Analysis (FMEA)

FMEA is the analysis of various failure modes and the resulting effects of the failure, and is a method of risk mitigation. Benefits include identification of design changes, failure warning/recovery systems and corrective action.

Electrical Stress Analysis

Electrical stress analysis determines a part’s performance under various stresses and environmental conditions, such as temperature. Induced stresses are commonly derived from the component datasheets and lab measurements or simulation results. This analysis produces component stress ratios for MTBF calculation, validation of component derating and correlation of failures of production units.

Electrical Design Component Derating

Electrical design component derating is the reduction of component specifications to decrease its failure rate with the goal of achieving the desired system reliability. This allows for component variations due to simple tolerance, aging, and alternate sources and results in improved reliability and customer satisfaction, and reduced service calls and repair costs. Although the immediate cost is higher, the bottom line (including support costs, etc) is usually less than without a thorough derating study.

Test Coverage Analysis (TCA)

TCA is the analysis of product functional verification (EVT/DVT) and other testing. It ultimately ensures sufficient and efficient testing, thus also avoiding redundancy at different stages.

6. Methodology using Allegro AMS Simulator Integrated with Design Entry HDL

Figure 3 shows a hardware engineer's Allegro AMS Simulator flow and methodology, which takes advantage of the interactions between the Advanced Analysis tools, including Sensitivity, Optimizer, Smoke and Monte-Carlo. This is also the process that was followed with the test case. Although the flowchart represents a fairly closed flow, the stars represent opportunities to involve the other organizations in your company.

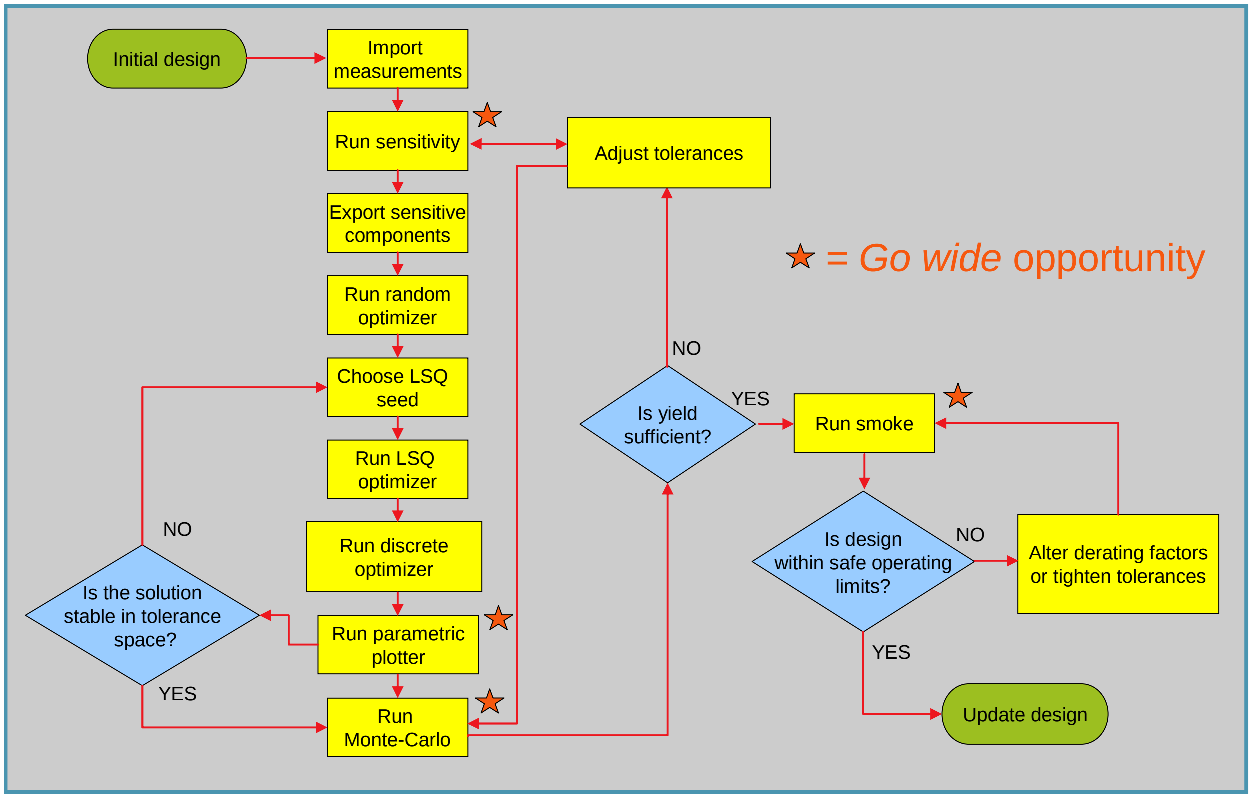


Figure 3 - Allegro AMS Simulator analysis flow diagram for the SMPS test case

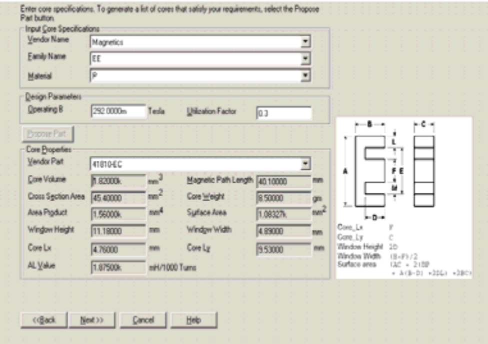
The following is a summary of the SMPS design, analysis and optimization process:

i. Basic Design Entry

The SMPS design was entered into Allegro Design Entry HDL using standard components from the install CDs.

ii. Transformer specification and model creation

The Magnetic Parts Editor (part of Allegro AMS Simulator) was used to select cores, determine turn count, wire type and ultimately, create the simulation model for the transformer. The Magnetic Parts Editor takes input such as SMPS topology, switching frequency, and number of windings, and iteratively (e.g. should the necessary windings not fit) determines the construction of the transformer.



Enter core specifications. To generate a list of cores that satisfy your requirements, select the Propose Part button.

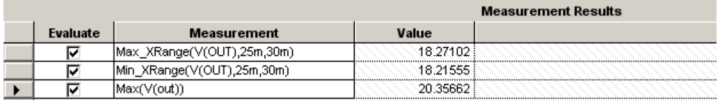
Input Core Specifications
Vendor Name: Magnetics
Family Name: EE
Material: P

Design Parameters
Operating B: 292.0000m Tesla
Utilization Factor: 0.3

Core Properties
Vendor Part: 41810-EC
Core Volume: 1.82000k mm^3
Magnetic Path Length: 40.10000 mm
Cross Section Area: 45.40000 mm^2
Core Weight: 8.50000 gm
Area Product: 1.56000k mm^4
Surface Area: 1.08327k mm^2
Window Height: 11.18000 mm
Window Width: 4.89000 mm
Core Lx: 4.76000 mm
Core Ly: 9.53000 mm
AL Value: 1.87500k mH/1000 Turns

iii. Setup for Simulation

This included the creation of simulation profiles, setting of error conditions (assertions - such as winding over-voltage), and defining global parameters. Also, measurements were defined for the design. Examples of measurements include min and max output voltage for control of output nominal and ripple voltage, as well as output voltage overshoot during startup.

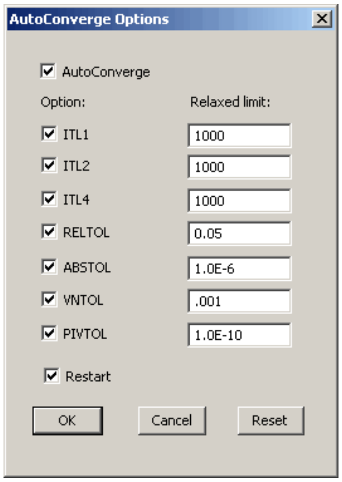


Measurement Results

	Evaluate	Measurement	Value
	☑	Max_XRange(V(OUT),25m,30m)	18.27102
	☑	Min_XRange(V(OUT),25m,30m)	18.21555
▶	☑	Max(V(out))	20.35662

iv. Functional verification and debugging

The design was simulated, and modified as necessary until operated to expectations. The new version 16.0 AutoConverge feature was helpful in quickly getting the design to simulate without having to manually tweak simulation settings.

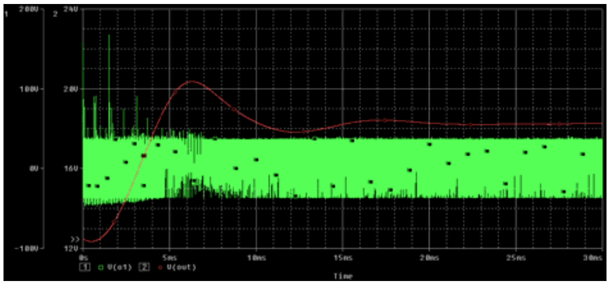


AutoConverge Options

☑ AutoConverge

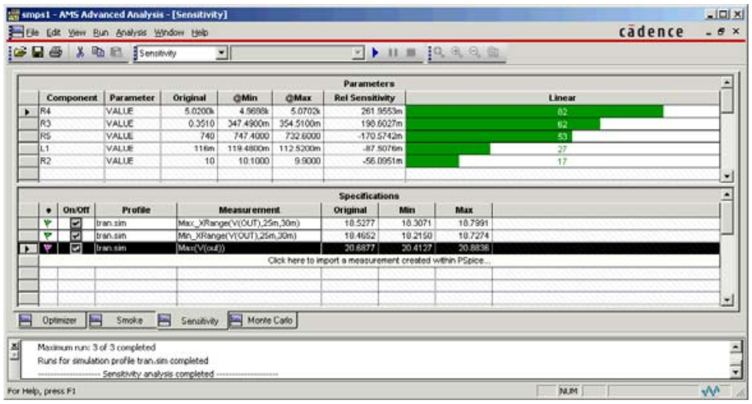
Option:	Relaxed limit:
☑ ITL1	1000
☑ ITL2	1000
☑ ITL4	1000
☑ RELTOL	0.05
☑ ABSTOL	1.0E-6
☑ VNTOL	.001
☑ PIVTOL	1.0E-10

☑ Restart



v. Sensitivity Analysis

Advanced Analysis Sensitivity identified the components that had the greatest impact on the measurements defined in step c above. The most influential components were ultimately seeded (right-click -> Send to Optimizer) into the optimizer, as they have the greatest ability to affect the measurement results. The tolerances of several components with little effect on the design's performance were relaxed as a cost reduction measure. Literally no setup was needed for Sensitivity beyond the selection of the measurements, and the simulation results were obtained in just a few minutes.



Parameters

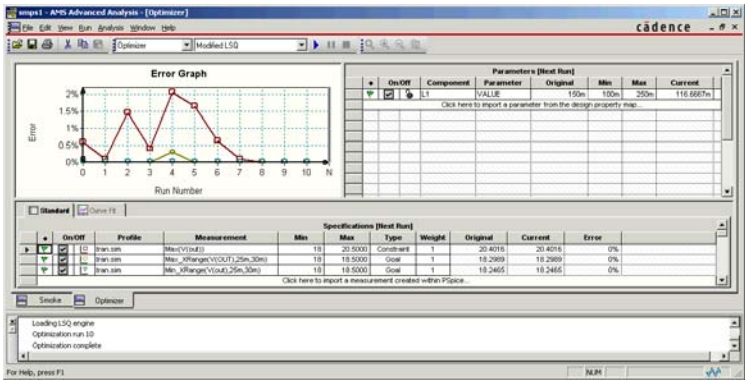
Component	Parameter	Original	@Min	@Max	Rel Sensitivity	Linear
R4	VALUE	5.0200k	4.9698k	5.0702k	261.9553m	82
R3	VALUE	0.3510	347.4900m	354.5100m	190.6027m	62
R5	VALUE	740	747.4000	732.6000	-170.5742m	53
L1	VALUE	116m	119.4800m	112.5200m	-87.5076m	27
R2	VALUE	10	10.1000	9.9000	-56.0951m	17

Specifications

●	On/Off	Profile	Measurement	Original	Min	Max
	☑	tran.sim	Max_XRange(V(OUT),25m,30m)	18.5277	18.3071	18.7991
	☑	tran.sim	Min_XRange(V(OUT),25m,30m)	18.4652	18.2150	18.7274
	☑	tran.sim	Max(V(out))	20.6877	20.4127	20.8836

Click here to import a measurement created within PSpice...

```
Maximum run: 3 of 3 completed
Runs for simulation profile tran.sim completed
------------------ Sensitivity analysis completed ------------------
```



Parameters [Next Run]

●	On/Off		Component	Parameter	Original	Min	Max	Current
	☑		L1	VALUE	150m	100m	250m	116.6667m

Click here to import a parameter from the design property map...

Specifications [Next Run]

●	On/Off		Profile	Measurement	Min	Max	Type	Weight	Original	Current	Error
	☑		tran.sim	Max(V(out))	18	20.5000	Constraint	1	20.4016	20.4016	0%
	☑		tran.sim	Max_XRange(V(OUT),25m,30m)	18	18.5000	Goal	1	18.2989	18.2989	0%
	☑		tran.sim	Min_XRange(V(out),25m,30m)	18	18.5000	Goal	1	18.2465	18.2465	0%

Click here to import a measurement created within PSpice...

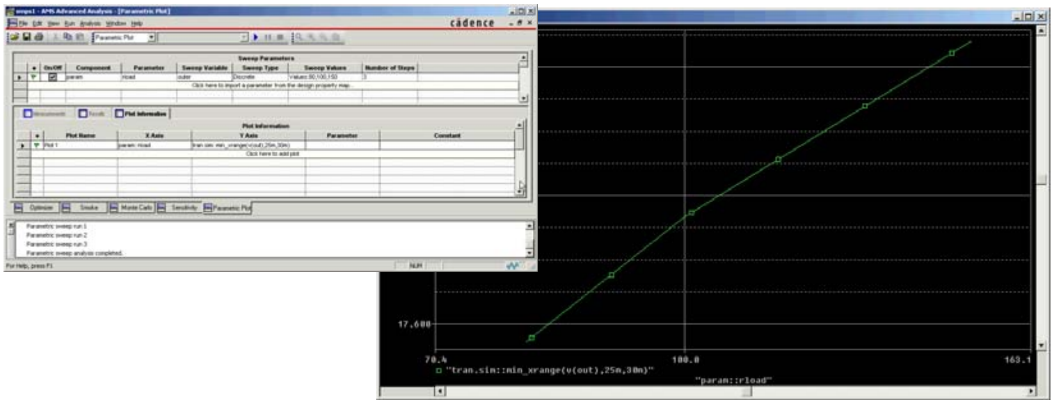
```
Loading LSQ engine
Optimization run 10
Optimization complete
```

vi. Optimizing the Design

As mentioned earlier in this paper, Optimizer allows the engineer to identify component parameters that Advanced Analysis can vary, in order to meet specific performance specifications (via limits on the measurements from step c above). The "Random" engine was used first, so that multiple error minima would be identified if they exist. Once a promising seed point (best run from the random engine) was identified, the "Modified Least Squares" engine was used from that point to converge on the optimized design. Finally, the "Discrete" engine was run to meet the same performance requirements while using only off-the-shelf standard values (e.g. 10% resistor values) for the optimized components. To set up Optimizer, specifications were entered, and parameters (component values or other parameters to vary/optimize) were selected from a list.

vii. Parametric Plotter

The parametric plotter was used to verify that the optimized components did not produce unexpected behavior over their practical range. Monte Carlo also has the ability to produce this type of result, but Parametric Plot allows us to concentrate on specific components and with more control. Selecting sweep parameters was straightforward, and plots (graphs) were defined via a wizard interface.



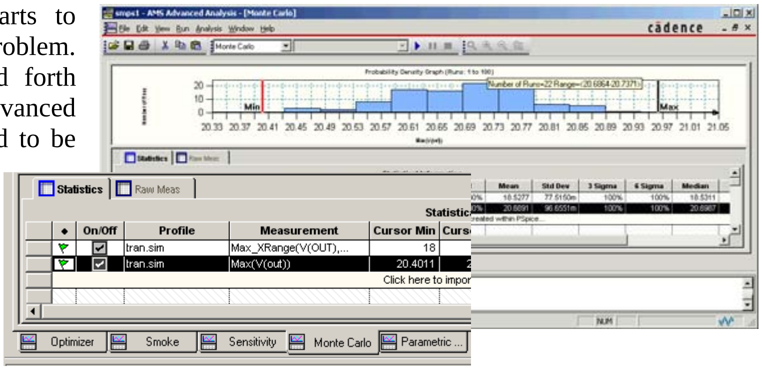
◆	On/Off	Component	Parameter	Sweep Variable	Sweep Type	Sweep Values	Number of Steps
▼	☑	param	rload	outer	Discrete	Values:80,100,150	3

◆	Plot Name	X Axis	Y Axis	Parameter	Constant
▼	Plot 1	param::rload	tran.sim::min_xrange(v(out),25m,30m)		

Parametric sweep run 1
Parametric sweep run 2
Parametric sweep run 3
Parametric sweep analysis completed.

viii. Monte Carlo

Via Monte Carlo, all toleranced components were varied with their distribution types taken into account to determine design yield against the specifications. Although not the case with this design, it's conceivable that yield (against one or more measurements and their limits) is not 100% at this point. Switching to the Sensitivity tab in Advanced Analysis would reveal the components that most greatly affected a specific measurement, and thus, which parts to concentrate on to correct the yield problem. The ability to "bounce" back and forth from one tool to another within Advanced Analysis (via selection tabs) proved to be very powerful at this stage.

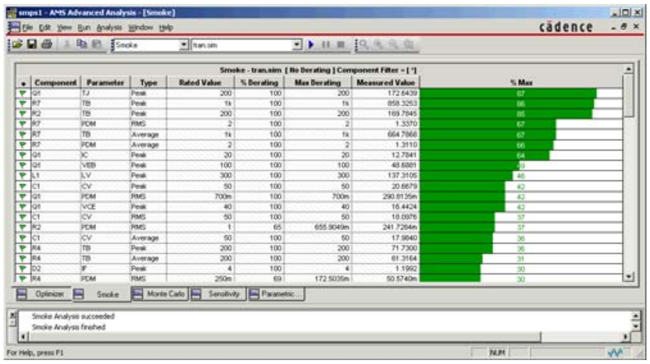


◆	On/Off	Profile	Measurement	Cursor Min
▼	☑	tran.sim	Max_XRange(V(OUT),...	18
▼	☑	tran.sim	Max(V(out))	20.4011

Mean	Std Dev	3 Sigma	6 Sigma	Median
18.5277	77.5150m	100%	100%	18.5311
20.6891	96.6551m	100%	100%	20.6987

ix. Smoke Analysis

Several components were found to be exceeding their stress ratings using Smoke. Adjustments to the design were made with regard to these devices. Some very-low-stress devices were identified and substituted with less expensive parts to reduce the product cost without negatively impacting performance, yield, or reliability. The stress ratings for the individual parts (such as the transistors) were already included in their model as part of the Advanced Analysis libraries on the install CDs. A major strength of Smoke is that with practically no setup, stress information is nearly immediately available for every component in the design, not just the parts that the engineer may be concerned about.



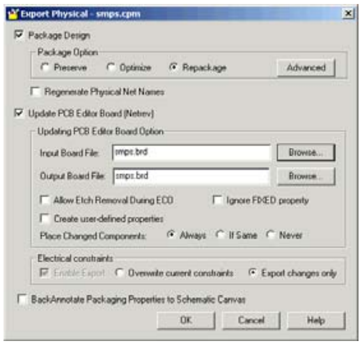
Smoke - tran.sim [No Derating] Component Filter = [*]

◆	Component	Parameter	Type	Rated Value	% Derating	Max Derating	Measured Value	% Max
▼	Q1	TJ	Peak	200	100	200	172.6439	87
▼	R7	TB	Peak	1k	100	1k	858.3253	86
▼	R2	TB	Peak	200	100	200	169.7845	85
▼	R7	PDM	RMS	2	100	2	1.3370	67
▼	R7	TB	Average	1k	100	1k	664.7868	67
▼	R7	PDM	Average	2	100	2	1.3110	66
▼	Q1	IC	Peak	20	100	20	12.7841	64
▼	Q1	VEB	Peak	100	100	100	48.6881	49
▼	L1	LV	Peak	300	100	300	137.3105	46
▼	C1	CV	Peak	50	100	50	20.6679	42
▼	Q1	PDM	RMS	700m	100	700m	290.8135m	42
▼	Q1	VCE	Peak	40	100	40	16.4424	42
▼	C1	CV	RMS	50	100	50	18.0976	37
▼	R2	PDM	RMS	1	65	655.9049m	241.7284m	37
▼	C1	CV	Average	50	100	50	17.9840	36
▼	R4	TB	Peak	200	100	200	71.7300	36
▼	R4	TB	Average	200	100	200	61.3164	31
▼	D2	IF	Peak	4	100	4	1.1992	30
▼	R4	PDM	RMS	250m	69	172.5035m	50.5740m	30

Smoke Analysis succeeded
Smoke Analysis finished

x. Export the design to Allegro PCB Editor

An “Export Physical” was performed on the design from Allegro Design Entry HDL to allow PCB layout to proceed.


Export Physical - smps.cpm
☑ Package Design
Package Option
○ Preserve ○ Optimize ● Repackage
☐ Regenerate Physical Net Names
☑ Update PCB Editor Board (Netrev)
Updating PCB Editor Board Option
Input Board File: smps.brd
Output Board File: smps.brd
☐ Allow Etch Removal During ECO ☐ Ignore FIXED property
☐ Create user-defined properties
Place Changed Components: ● Always ○ If Same ○ Never
Electrical constraints
☑ Enable Export ○ Overwrite current constraints ● Export changes only
☐ BackAnnotate Packaging Properties to Schematic Canvas

At this point the SMPS design was complete, and was known to be optimized in performance, reliability, yield, and cost, and was ready for PCB layout. The physical PCB would be edited and output to manufacturing using Allegro PCB Editor.

7. Conclusion

A methodology for designing safe, reliable and optimal analog/mixed signal products was introduced and used on an SMPS design. The example took advantage of an integrated flow (front-ended by Allegro Design Entry HDL) that supports analog and signal integrity simulation, as well as PCB design from a common schematic. Several reasons for “going wide” and taking analysis beyond the hardware engineer’s desk were given, and Cadence Allegro AMS Simulator Advanced Analysis was identified as being an enabler for effectively making that transition. The ability to quickly jump from one tool to another within Advanced Analysis, in addition to the ease of setup and speed of results makes Allegro AMS Simulator an easy choice for analog/mixed-signal design analysis, and offers the ability to reduce short and long term costs, while improving product yield and customer satisfaction.

8. Acknowledgments

Special thanks go to Paul Sandore, Technical Principal Program Manager - EMC Corporation, for his valuable input during the creation of this paper and presentation.