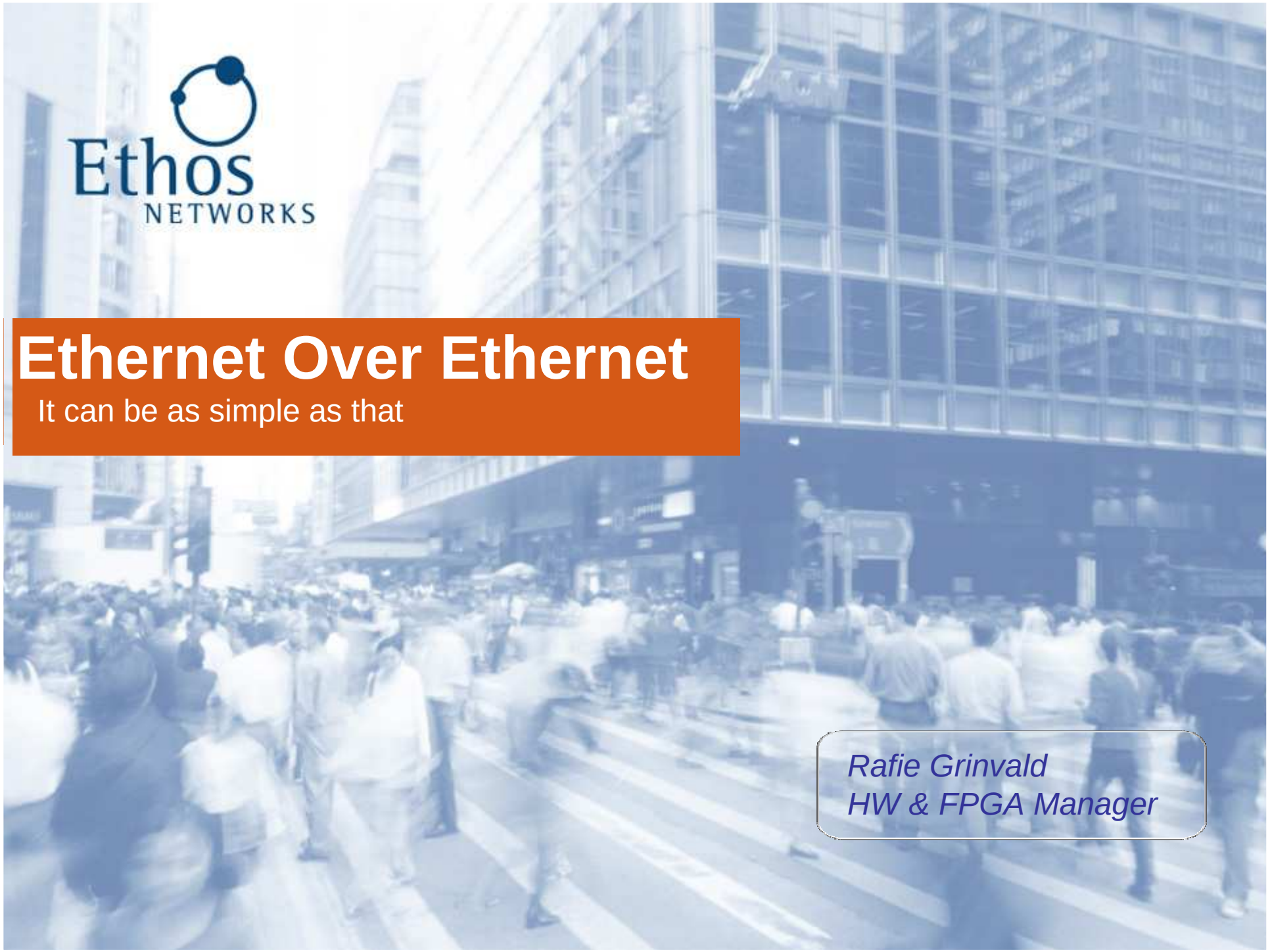


Ethernet Over Ethernet

It can be as simple as that

Rafie Grinvald
HW & FPGA Manager

Agenda

- *Ethos Networks Architecture*
- *Ethos 240Gbps Platform & Cards*
- *Design Flow using Concept*
- *Layout and Routing with Allegro Tools*
- *FPGAs Incisive Enterprise Verification*

Ethos NETWORKS

VoD

IPTV

Mobile Backhauling

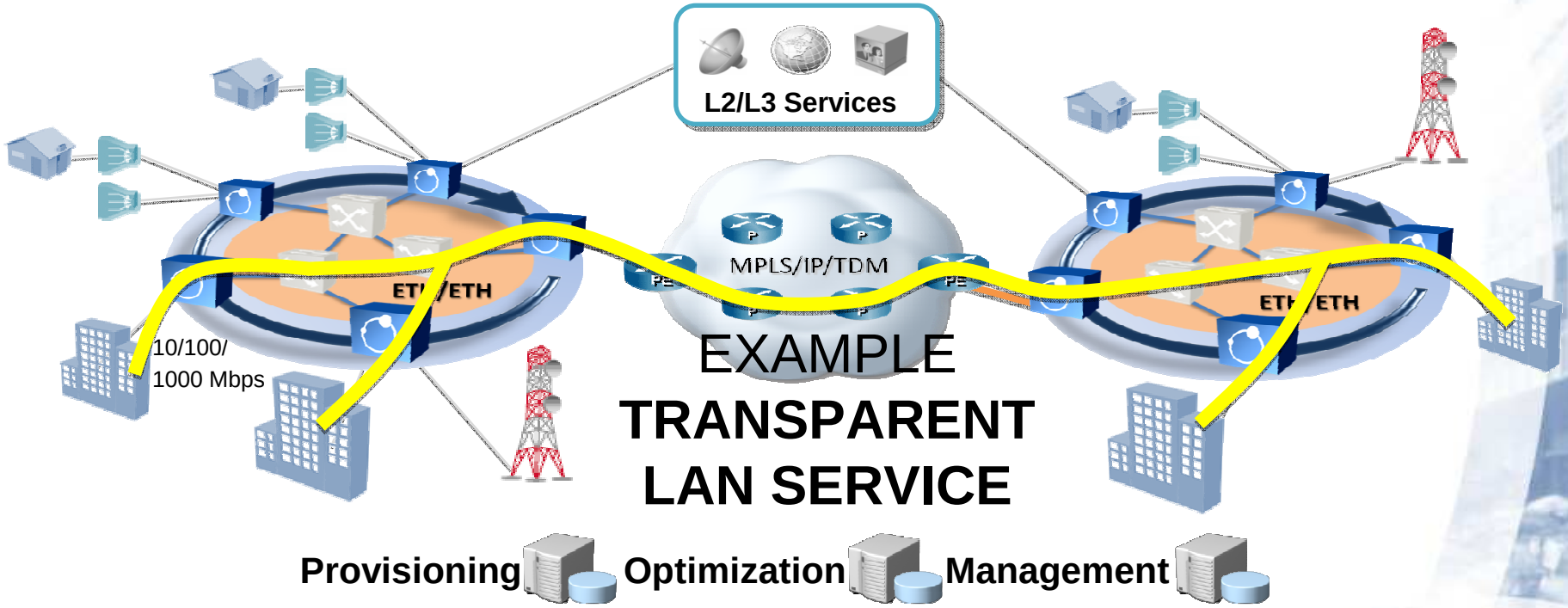
One network

Hundreds of SLAs

Ethos Architecture

Ethos NETWORKS

System View



Ethos NETWORKS

How does it work? Dynamic TE

1. Traffic admission is controlled at network edge…

2. … in real-time, based on traffic conditions across the network

3. Every edge holds an updated topology

4. Every edge holds per-flow service profiles

5. Edges communicate transmission intentions to each other every x ms…

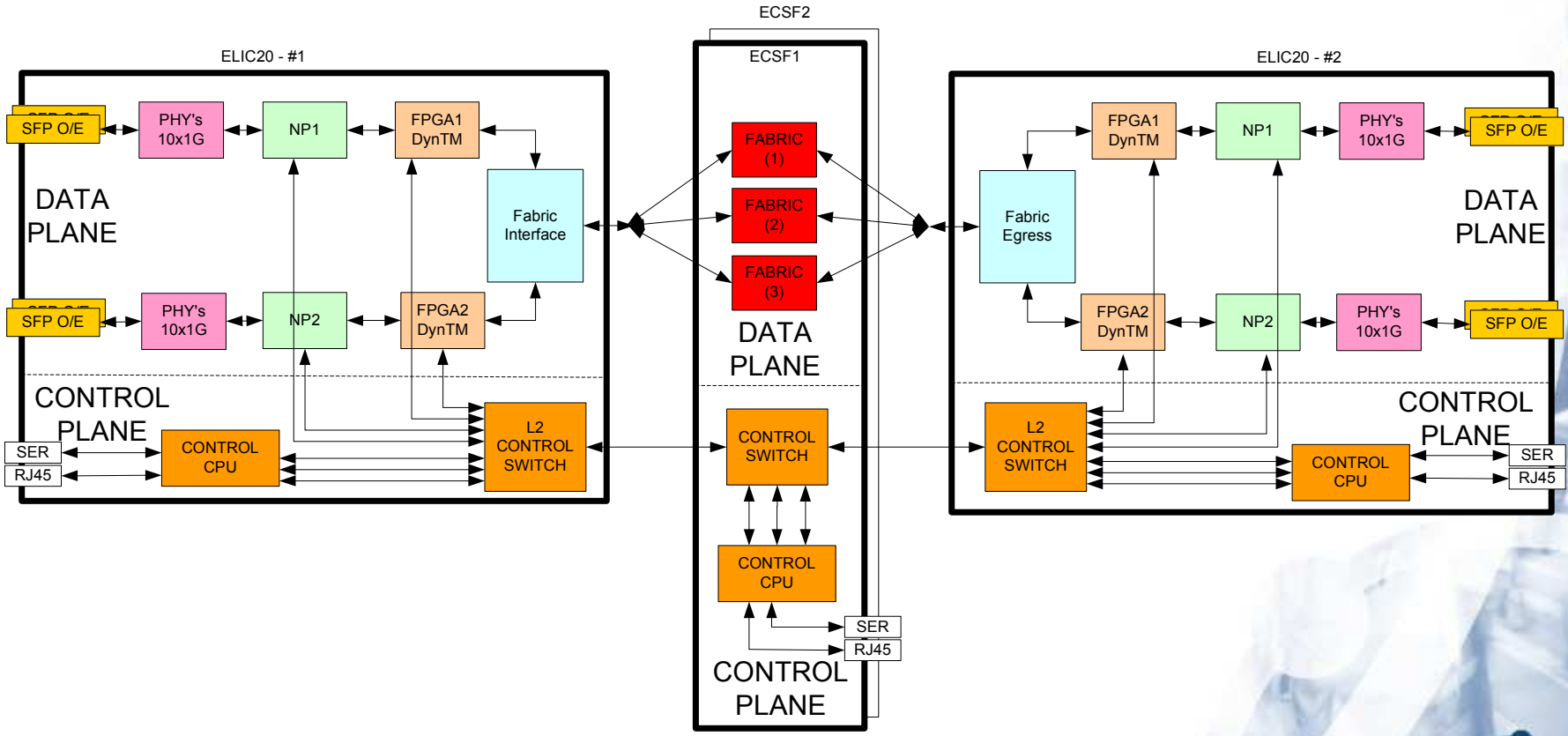
6. ..and perform concerted Admissions Control to ensure that SLAs are met

Ethos Solution

- ✓ ***Comprehensive Transport Solution***
- ✓ ***Connection-Oriented Ethernet , PBT***
- ✓ ***QoS guaranties per millions of flows***
- ✓ ***Ethernet efficiency, TDM reliability***
- ✓ ***Network capacity tripled***

Ethos NETWORKS

System Architecture



Ethos NETWORKS

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One network

Hundreds of SLAs

Ethos Platform

Ethos NETWORKS

Ethos Platforms

Ethos E-20

- 1-2 service slots
- 1-2 x 20 Gbps slots
- High-density GE and 10GE
- AC/DC power

Ethos E-60

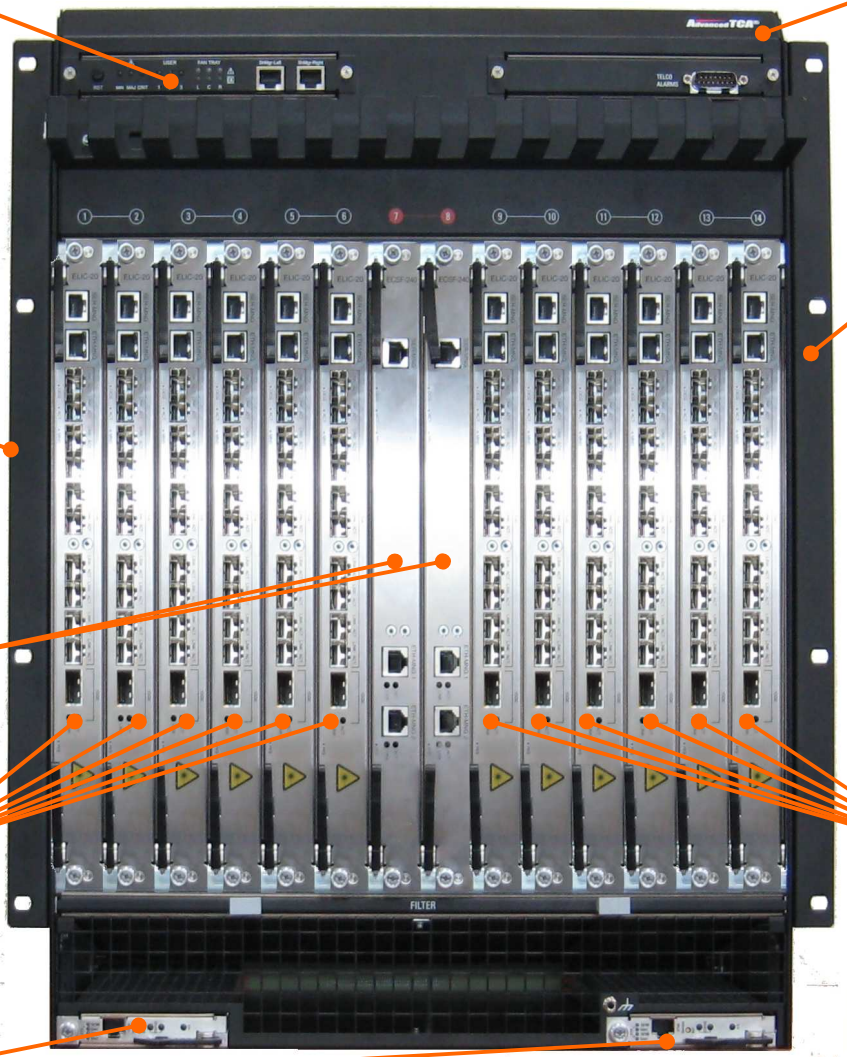
- 60 Gpbs switching
- 3 x 20 Gbps slots
- High-density GE and 10GE
- AC/DC power

Ethos E-240

- 280 Gbps switching
- 12 x 20 Gbps slots
- High-density GE and 10GE
- 2 systems per rack

Ethos NETWORKS

Chassis Architecture



Fan Tray &
Thermal Protection

240Gbps backplane

Central Switch Fabric
(ECSF) 1..2

Ethos Line Interface
Cards (ELIC) 1..6

Shelf managers

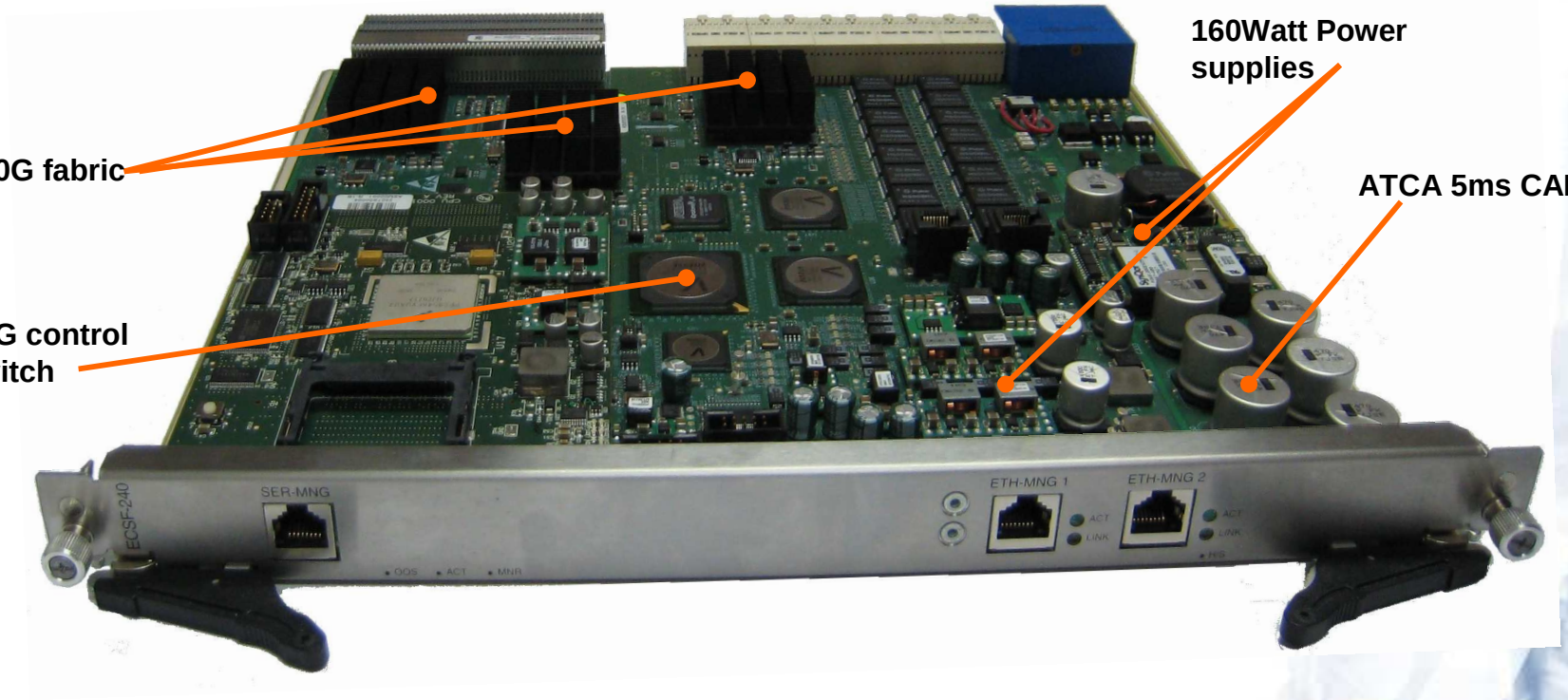
Non-Blocking
All-Ethernet
Architecture

Ethos Line Interface
Cards (ELIC) 7..12

AdvancedTCA®

Ethos
NETWORKS

ECSF 240G



Ethos NETWORKS

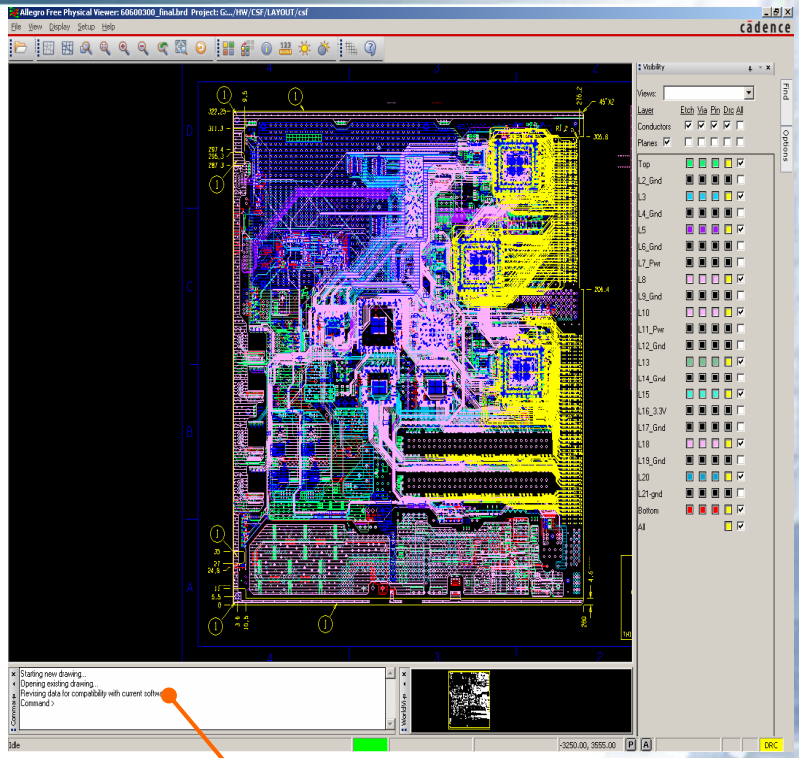
ECSF 240G Features

- *Switch fabric with 240Gbps capacity*
- *Base fabric 24Gpbs control switch (for Ethos management)*
- *160Watt power dissipation*
- *Ethos front panel management*
- *Centralized CPU unit*
- *Serial interfaces from front panel for debug and control*
- *Support ATCA Shelf Manager*
- *Complies to ATCA PICMG3.0*

Ethos NETWORKS

ESCF240G Electrical Features

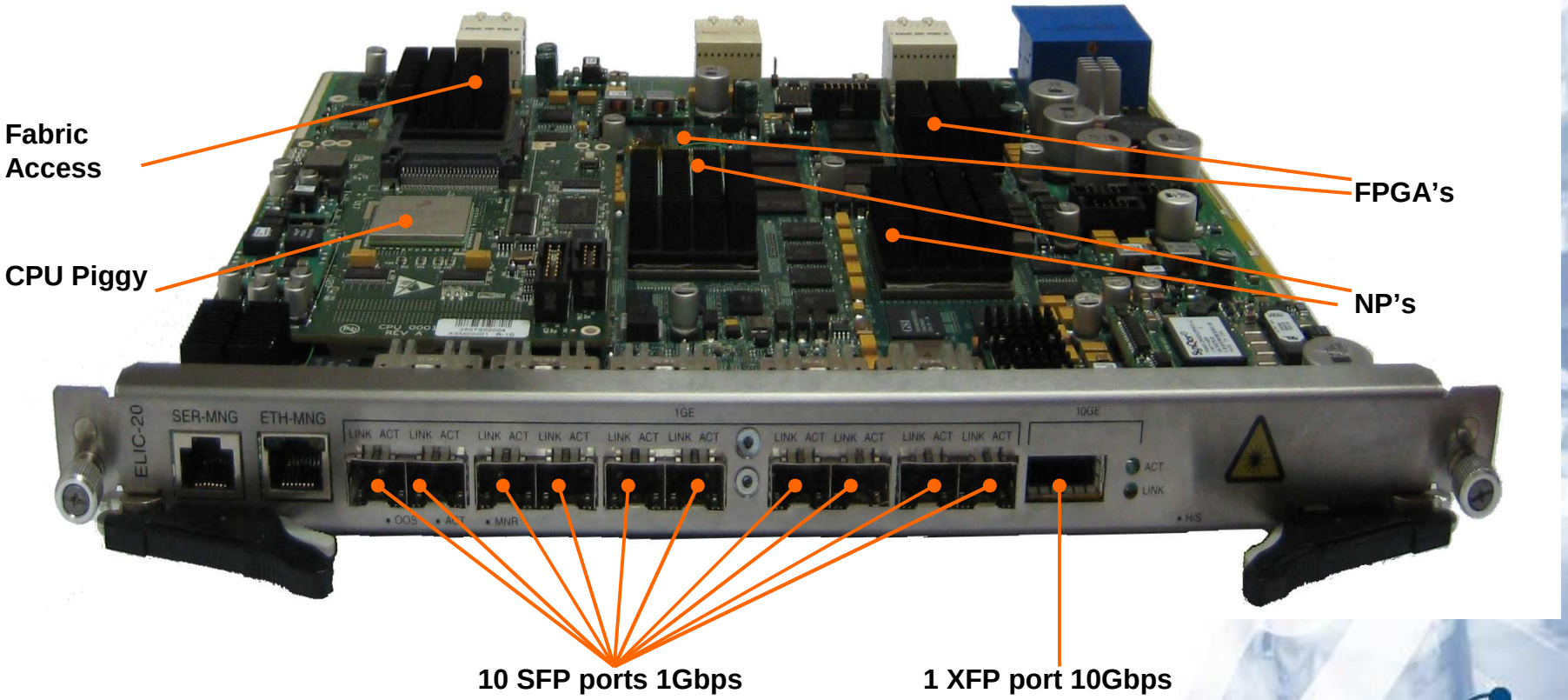
- *160 Watt per Line Card*
- *280mm x 300mm ATCA card*
- *22 Layers of PCB, Merix USA*
- *PCB thickness of 3.1mm*
- *~10,000 Via's*
- *~3,000 components*
- *3 FBGA's with more than 1300 ball grid pins*
- *80% of card is high speed differential signals*
- *20% of card is high speed single ended signals*
- *288 pairs of serial links at 3.125Gbps*



Allegro 16.0 Free Physical Viewer

Ethos NETWORKS

ELIC 20



Ethos NETWORKS

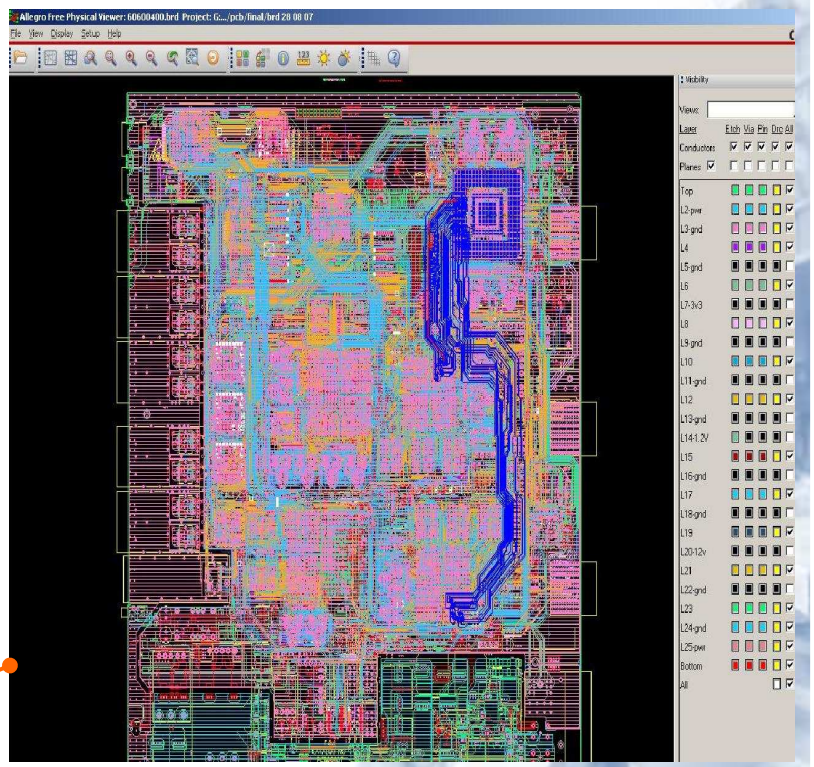
ELIC20 Features

- *20Gbps line card with inline Network Processors*
- *10 x 1Gb SFP copper (1000Base-T) or fiber interfaces*
- *1 x 10Gb XFP fiber interface*
- *20Gb fabric interface*
- *10/100/1000Base-T in front panel for OOB (Out Of Band) management (standalone)*
- *Serial interface from front panel*
- *Complies to ATCA PICMG3.0*
- *Ethos IP fully aware*

Ethos NETWORKS

ELIC20 Electrical Features

- *200 Watt per line card*
- *280mm x 300mm ATCA card*
- *26 Layers of PCB with cutting edge laser technology ,Merix USA*
- *PCB thickness of 3.2mm*
- *~49,000 Via's*
- *~7,000 components*
- *48Gbit DDR2 @ 667Mbps components*
- *5 FBGA's with more than 1300 ball grid pins*
- *20% of card is high speed differential signals*
- *80% of card is high speed single ended signals*



Allegro 16.0 Free Physical Viewer

Ethos NETWORKS

VoD

IPTV

Mobile Backhauling

One network

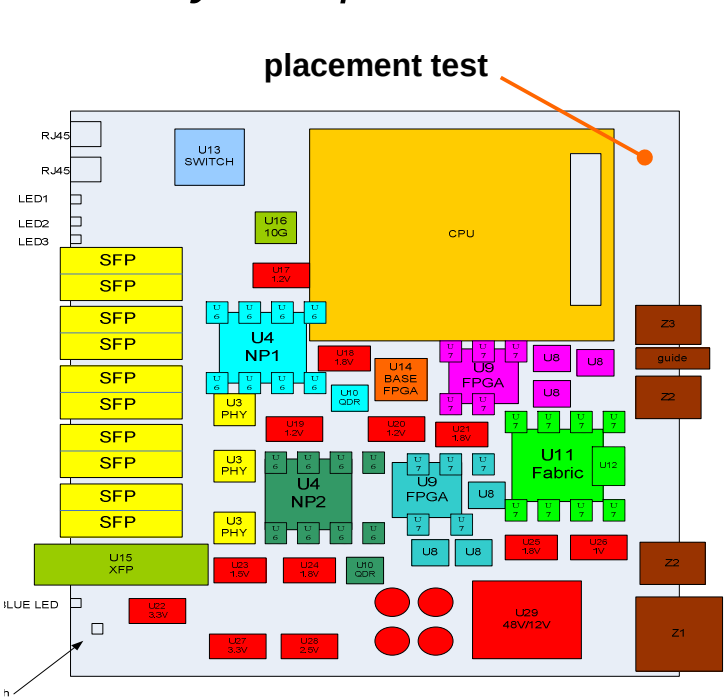
Hundreds of SLAs

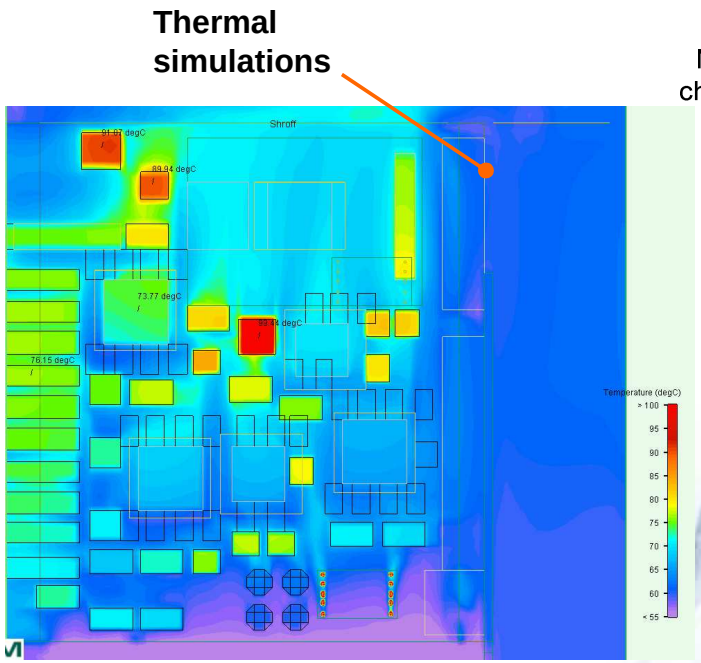
Ethos Design flow with Concept HDL

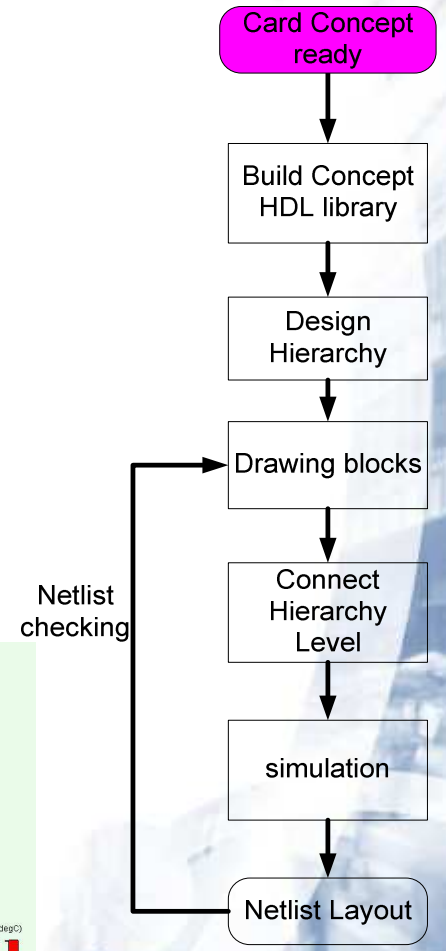
Design Flow with Concept HDL

Card Architecture:

- *Basic card architecture was ready after 2 months from green light*
- *All major components passed test benches prior to choosing IC vendors*
- *Physical placement tests were done after choosing IC vendors*
- *Physical placement led to thermal simulations tests*





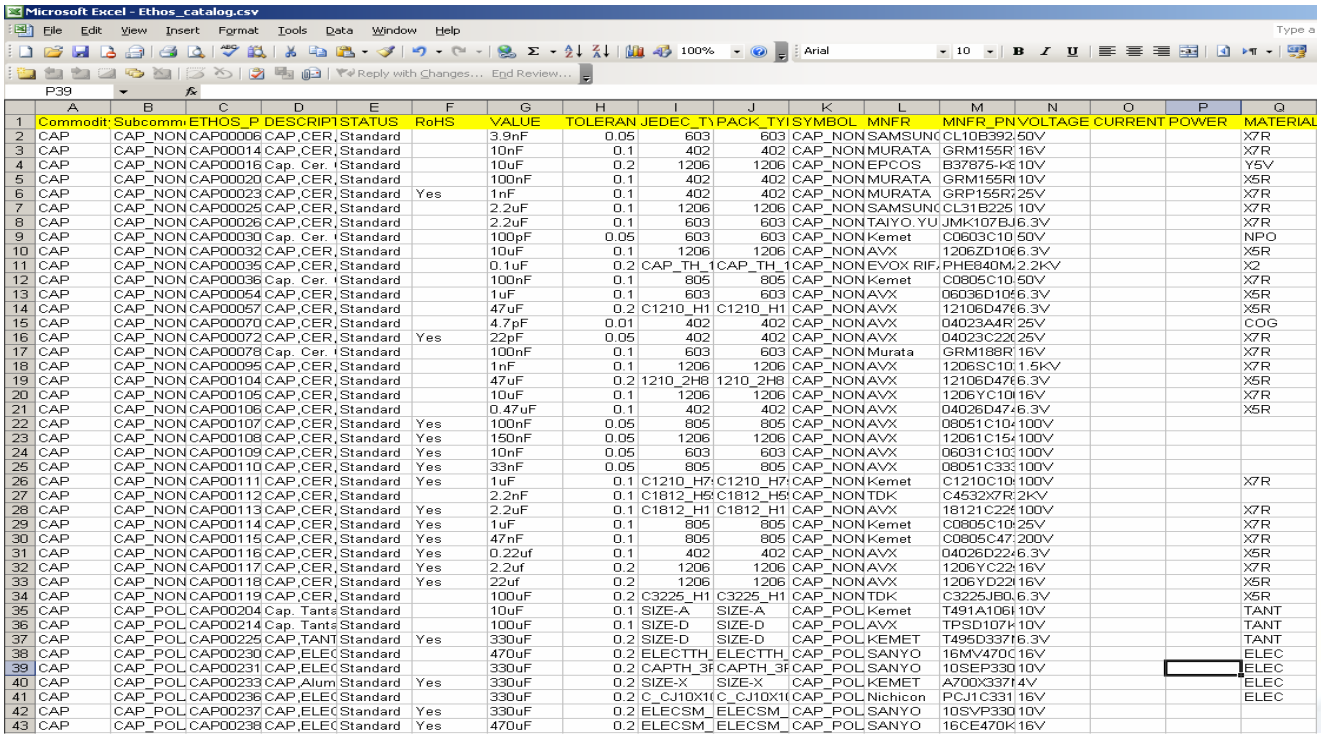


Ethos NETWORKS

Design Flow with Concept HDL

Concept HDL CAD Library:

- *Building around 150 different components*
- *All components include issues of layout and simulation aspects*
- *CAD library is in Excel format and can be imported to any operation database*



	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q
1	Commodit	Subcomm	ETHOS_P	DESCRIP	STATUS	RoHS	VALUE	TOLERAN	JEDEC_T	PACK_TY	SYMBOL	MNFR	MNFR_PN	VOLTAGE	CURRENT	POWER	MATERIAL
2	CAP	CAP_NON	CAP00006	CAP,CER,	Standard		3.9nF	0.05	603	603	CAP_NON	SAMSUNG	CL10B392	50V			X7R
3	CAP	CAP_NON	CAP00014	CAP,CER,	Standard		10nF	0.1	402	402	CAP_NON	MURATA	GRM155R	16V			X7R
4	CAP	CAP_NON	CAP00016	Cap. Cer.	Standard		10uF	0.2	1206	1206	CAP_NON	EPCOS	B37875-K	10V			Y5V
5	CAP	CAP_NON	CAP00020	CAP,CER,	Standard		100nF	0.1	402	402	CAP_NON	MURATA	GRM155R	10V			X5R
6	CAP	CAP_NON	CAP00023	CAP,CER,	Standard	Yes	1nF	0.1	402	402	CAP_NON	MURATA	GRP155R7	25V			X7R
7	CAP	CAP_NON	CAP00025	CAP,CER,	Standard		2.2uF	0.1	1206	1206	CAP_NON	SAMSUNG	CL31B225	10V			X7R
8	CAP	CAP_NON	CAP00026	CAP,CER,	Standard		2.2uF	0.1	603	603	CAP_NON	TAIYO. YU	JMK107BJ	6.3V			X7R
9	CAP	CAP_NON	CAP00030	Cap. Cer.	Standard		100pF	0.05	603	603	CAP_NON	Kemet	C0603C10	50V			NPO
10	CAP	CAP_NON	CAP00032	CAP,CER,	Standard		10uF	0.1	1206	1206	CAP_NON	AVX	1206ZD10	6.3V			X5R
11	CAP	CAP_NON	CAP00035	CAP,CER,	Standard		0.1uF	0.2	CAP_TH_1	CAP_TH_1	CAP_NON	EVOX RIF	PHE840M	2.2KV			X2
12	CAP	CAP_NON	CAP00036	Cap. Cer.	Standard		100nF	0.1	805	805	CAP_NON	Kemet	C0805C10	50V			X7R
13	CAP	CAP_NON	CAP00054	CAP,CER,	Standard		1uF	0.1	603	603	CAP_NON	AVX	06036D10	6.3V			X5R
14	CAP	CAP_NON	CAP00057	CAP,CER,	Standard		47uF	0.2	C1210_H1	C1210_H1	CAP_NON	AVX	12106D476	6.3V			X5R
15	CAP	CAP_NON	CAP00070	CAP,CER,	Standard		4.7pF	0.01	402	402	CAP_NON	AVX	04023A4R	25V			COG
16	CAP	CAP_NON	CAP00072	CAP,CER,	Standard	Yes	22pF	0.05	402	402	CAP_NON	AVX	04023C22	25V			X7R
17	CAP	CAP_NON	CAP00078	Cap. Cer.	Standard		100nF	0.1	603	603	CAP_NON	Murata	GRM188R	16V			X7R
18	CAP	CAP_NON	CAP00095	CAP,CER,	Standard		1nF	0.1	1206	1206	CAP_NON	AVX	1206SC10	1.5KV			X7R
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26	CAP	CAP_NON	CAP00111	CAP,CER,	Standard	Yes	1uF	0.1	C1210_H7	C1210_H7	CAP_NON	Kemet	C1210C10	100V			X7R
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28	CAP	CAP_NON	CAP00113	CAP,CER,	Standard	Yes	2.2uF	0.1	C1812_H1	C1812_H1	CAP_NON	AVX	18121C225	100V			X7R
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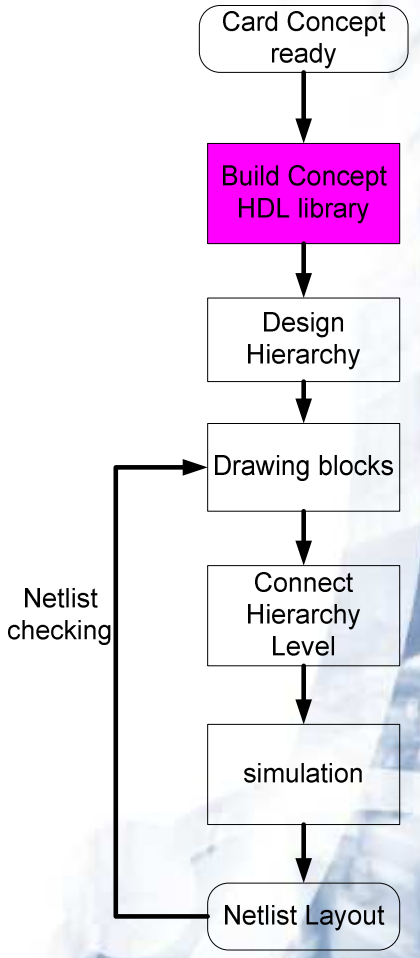
31	CAP	CAP_NON	CAP00116	CAP,CER,	Standard	Yes	0.22uf	0.1	402	402	CAP_NON	AVX	04026D224	6.3V			X5R
32	CAP	CAP_NON	CAP00117	CAP,CER,	Standard	Yes	2.2uf	0.2	1206	1206	CAP_NON	AVX	1206YC22	16V			X7R
33	CAP	CAP_NON	CAP00118	CAP,CER,	Standard	Yes	22uf	0.2	1206	1206	CAP_NON	AVX	1206YD22	16V			X5R
34	CAP	CAP_NON	CAP00119	CAP,CER,	Standard		100uF	0.2	C3225_H1	C3225_H1	CAP_NON	TDK	C3225JB0	6.3V			X5R
35	CAP	CAP_POL	CAP00204	Cap. Tant	Standard		10uF	0.1	SIZE-A	SIZE-A	CAP_POL	Kemet	T491A106	10V			TANT
36	CAP	CAP_POL	CAP00214	Cap. Tant	Standard		100uF	0.1	SIZE-D	SIZE-D	CAP_POL	AVX	TPSD107K	10V			TANT
37	CAP	CAP_POL	CAP00225	CAP,TANT	Standard	Yes	330uF	0.2	SIZE-D	SIZE-D	CAP_POL	KEMET	T495D337K	6.3V			TANT
38	CAP	CAP_POL	CAP00230	CAP,ELEC	Standard		470uF	0.2	ELECTTH_	ELECTTH_	CAP_POL	SANYO	16MV470C	16V			ELEC
39	CAP	CAP_POL	CAP00231	CAP,ELEC	Standard		330uF	0.2	CAPTH_3F	CAPTH_3F	CAP_POL	SANYO	10SEP330	10V			ELEC
40	CAP	CAP_POL	CAP00233	CAP,Alum	Standard	Yes	330uF	0.2	SIZE-X	SIZE-X	CAP_POL	KEMET	A700X337	4V			ELEC
41	CAP	CAP_POL	CAP00236	CAP,ELEC	Standard		330uF	0.2	C_CJ10X1	C_CJ10X1	CAP_POL	Nichicon	PCJ1C331	16V			ELEC
42	CAP	CAP_POL	CAP00237	CAP,ELEC	Standard	Yes	330uF	0.2	ELECSM_	ELECSM_	CAP_POL	SANYO	10SVP330	10V			
43	CAP	CAP_POL	CAP00238	CAP,ELEC	Standard	Yes	470uF	0.2	ELECSM_	ELECSM_	CAP_POL	SANYO	16CE470K	16V			



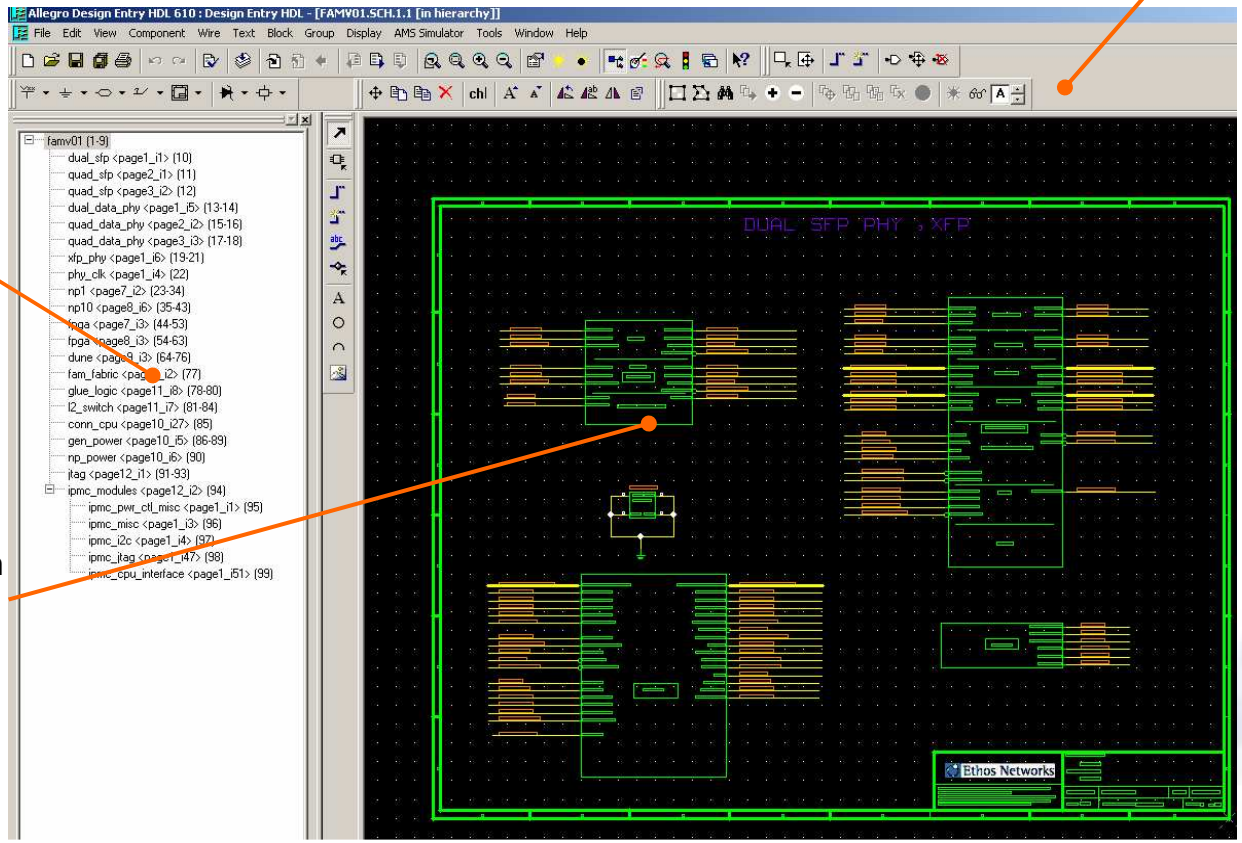
Ethos NETWORKS

Design Flow with Concept HDL

Design Hierarchy:

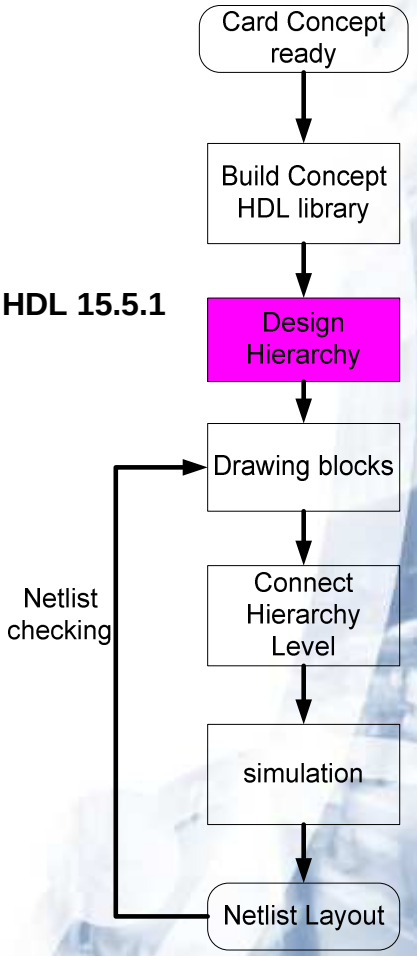
- *Top down hierarchy design*
- *Design comprised of over 100 pages*
- *Database of 500MB (in HDL format)*

Concept HDL 15.5.1



Hierarchy Tree

Top down Hierarchy

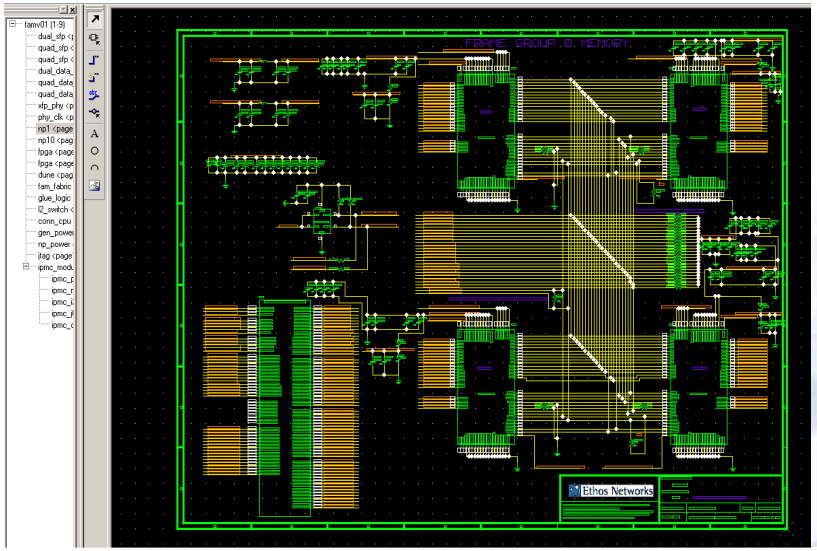


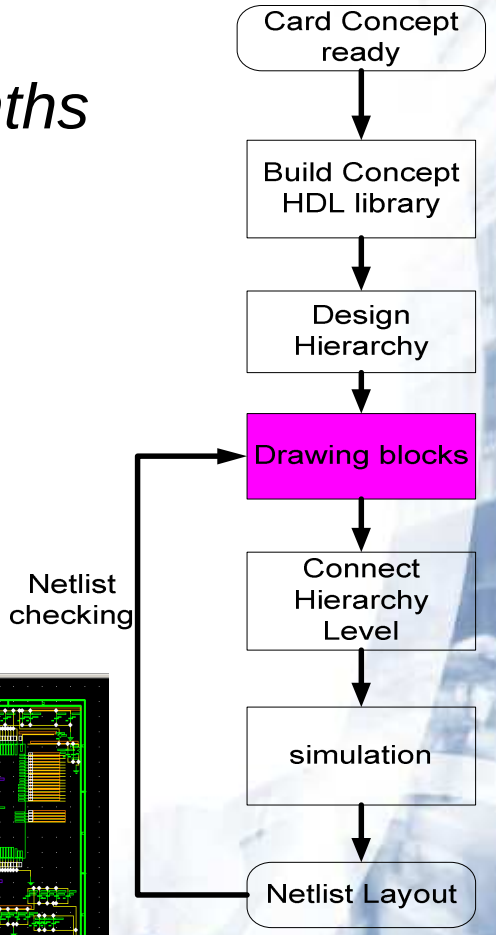
Ethos NETWORKS

Design Flow with Concept HDL

Drawing Blocks:

- *Design of ~7,000 components around 3 months*
- *~25,000 nets over the ELIC card drawn*
- *Design with layout consideration:*
  - *Designing power planes*
  - *Adding constrains*
  - *EMC considerations*
  - *Mechanical issues*



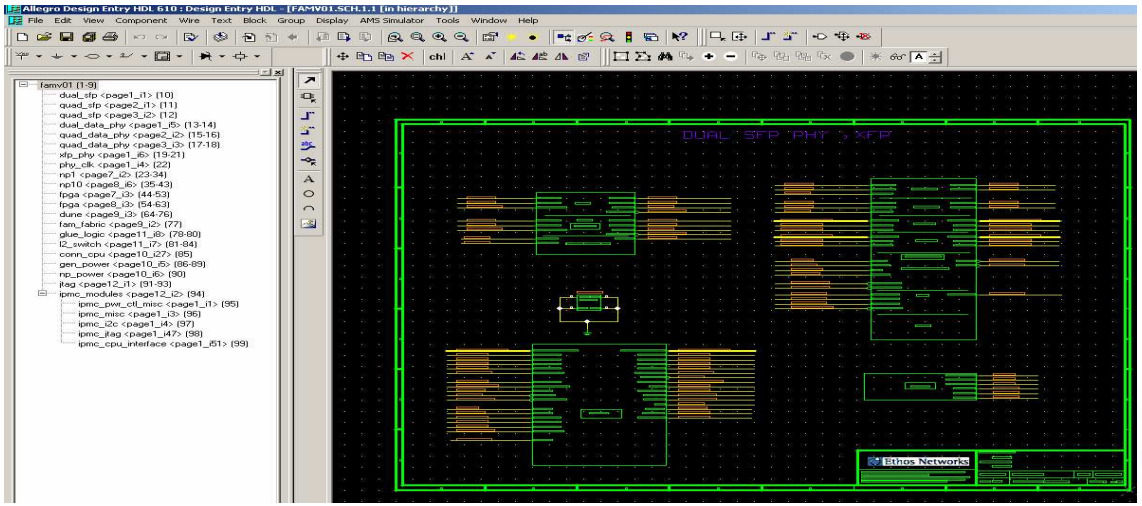


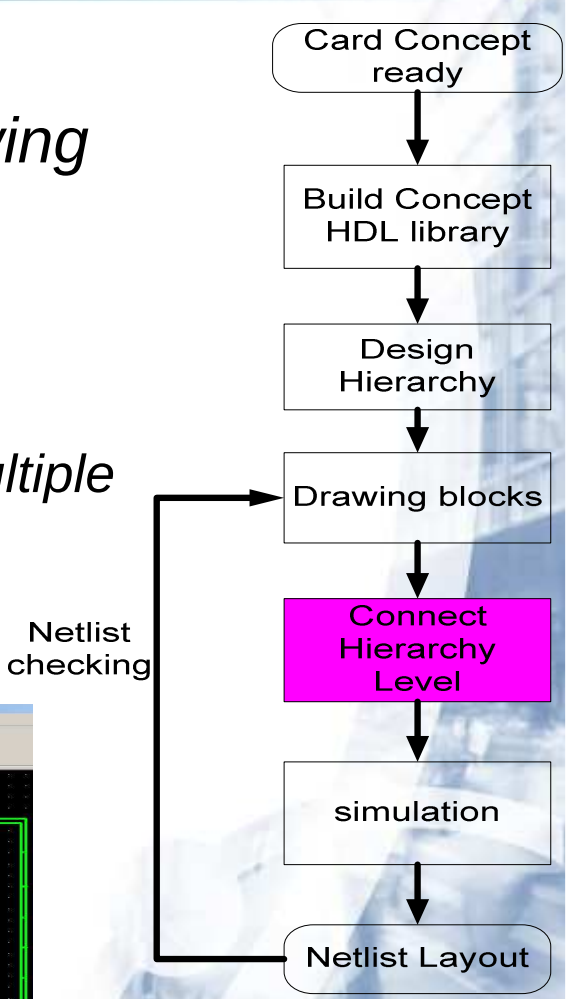
Ethos NETWORKS

Design Flow with Concept HDL

Integration Hierarchy:

- *The use of block instantiations reduced drawing cycle*
- *BOM (Bill Of Material) issues:*
  - *All components marked with N/A tag*
  - *BOM variants tool was implemented (including multiple assemblies)*
  - *BOM can be easily exported to excel and to any operational data base*



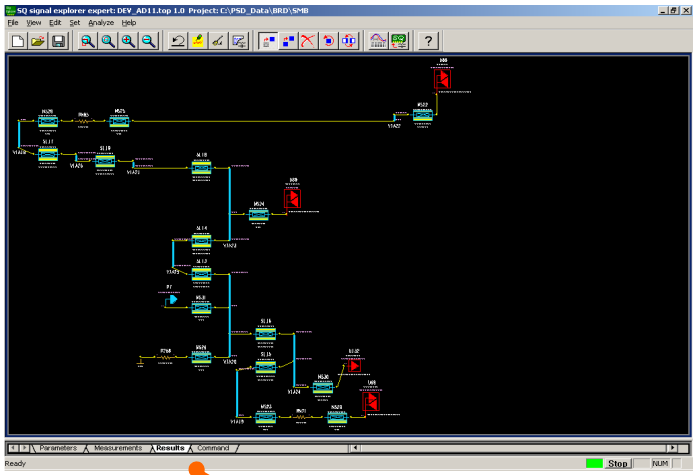


Ethos NETWORKS

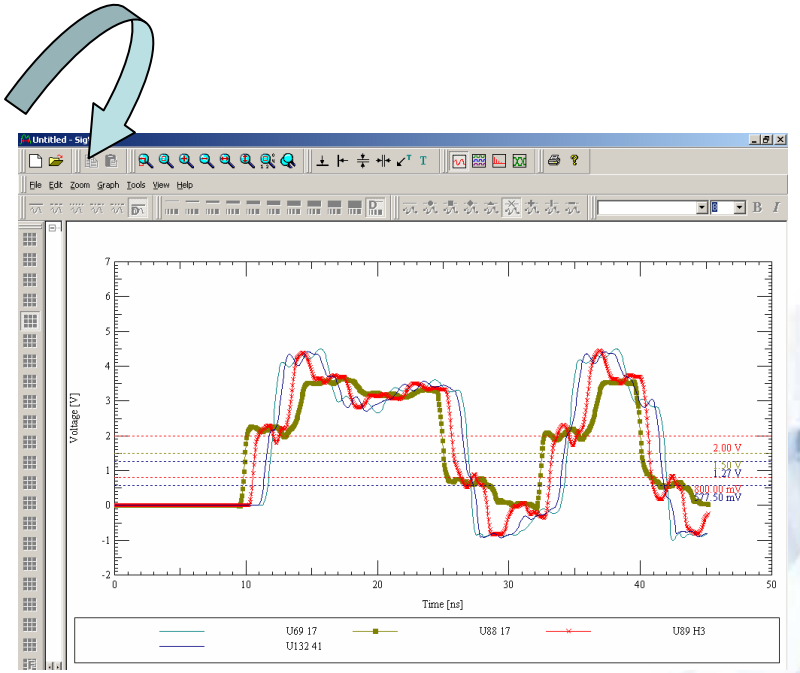
Design Flow with Concept HDL

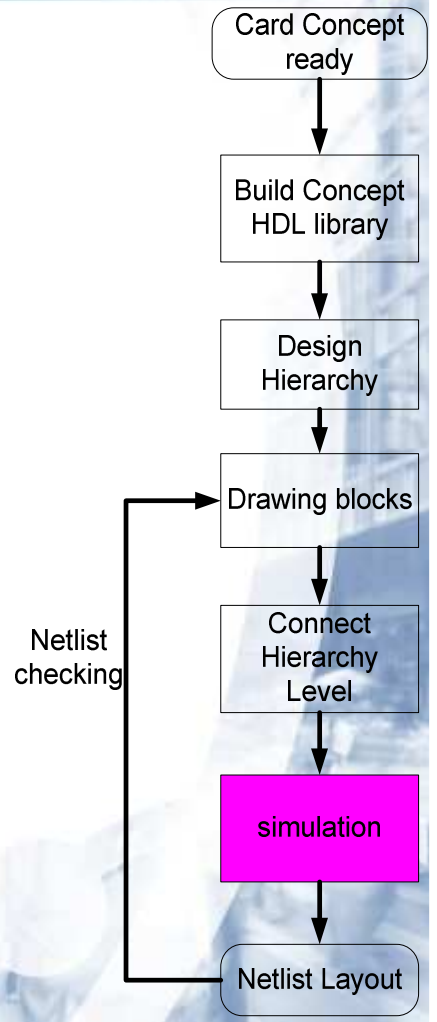
Simulations:

- *Only major items were tested at simulation phase (DDRII, differential lines)*
- *SigXplorer simulation suite was used*
- *IBIS up to 1GHz or SPICE models can be used*



SigXplorer Testing example



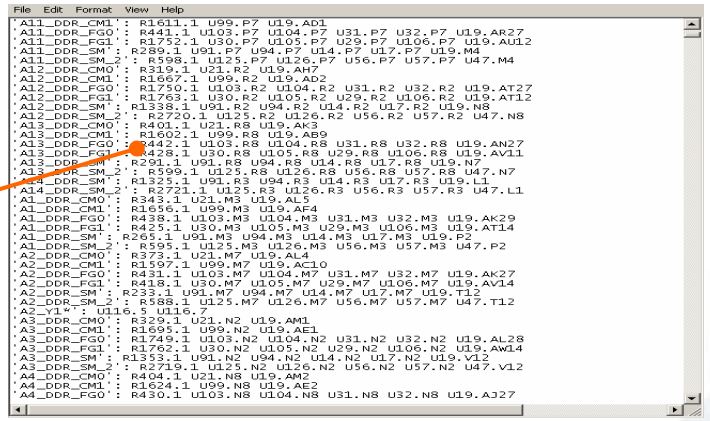


Ethos NETWORKS

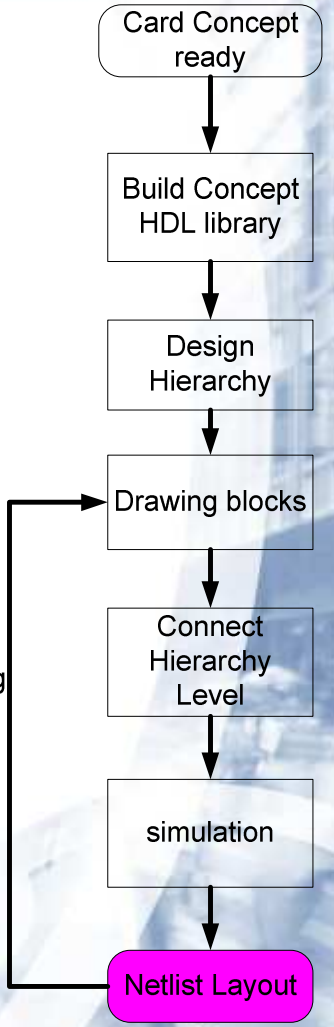
Design Flow with Concept HDL

Netlist Checking:

- *Only major components were tested*
- *DRC (Design Rule Check) running is recommended before Netlist checking*
- *No software application can test logical insights*
- *Bug fixing is done at drawing blocks phase*
- *Netlist checking takes around 1 month in parallel to routing (25,000 nets)*
- *All nets should include routing name*



Netlist checking with proprietary scripts



Ethos NETWORKS

Concept HDL Summary

Advantages:

- *Works well with large schemes (~500M)*
- *HDL/ASCII engine enables easy reading and block checking*
- *High integration with simulation and layout Software*

Possible Improvements:

- *Support of team work*
- *ConceptHDL unstable under Linux*
- *Limitations on back annotation from Layout tool to ConceptHDL with instantiations*

Ethos NETWORKS

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IPTV

Mobile Backhauling

One network

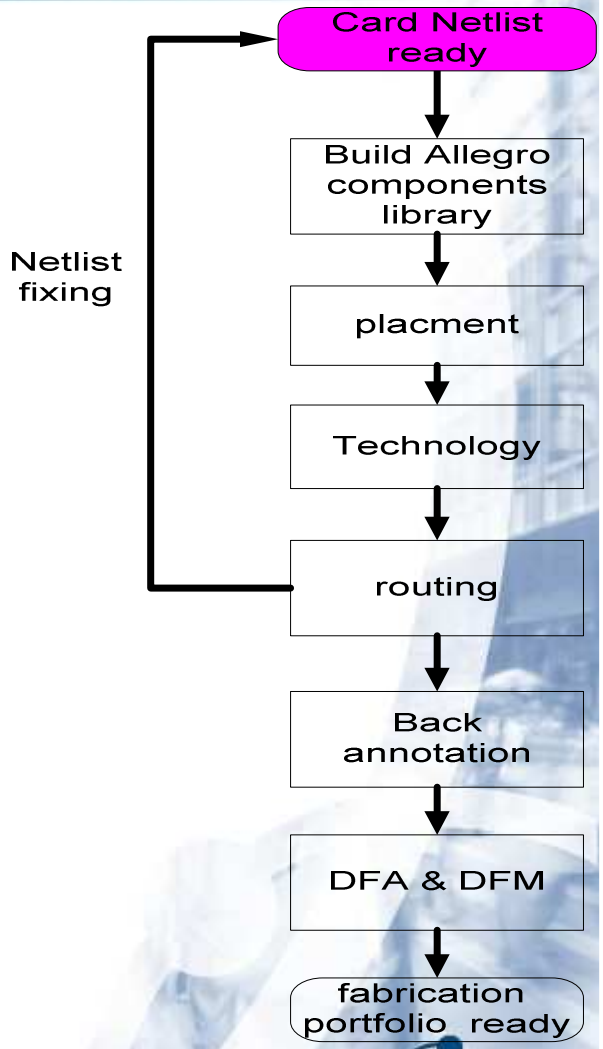
Hundreds of SLAs

Ethos Card layout with Allegro

Layout Flow with Allegro

Card Netlist Ready:

- *Netlist passed with bugs, but with full components count*
- *First Netlist draft passed after 3 months of scheme drawings*
- *Support of technologist engineer begins from netlist to fabrication portfolio*

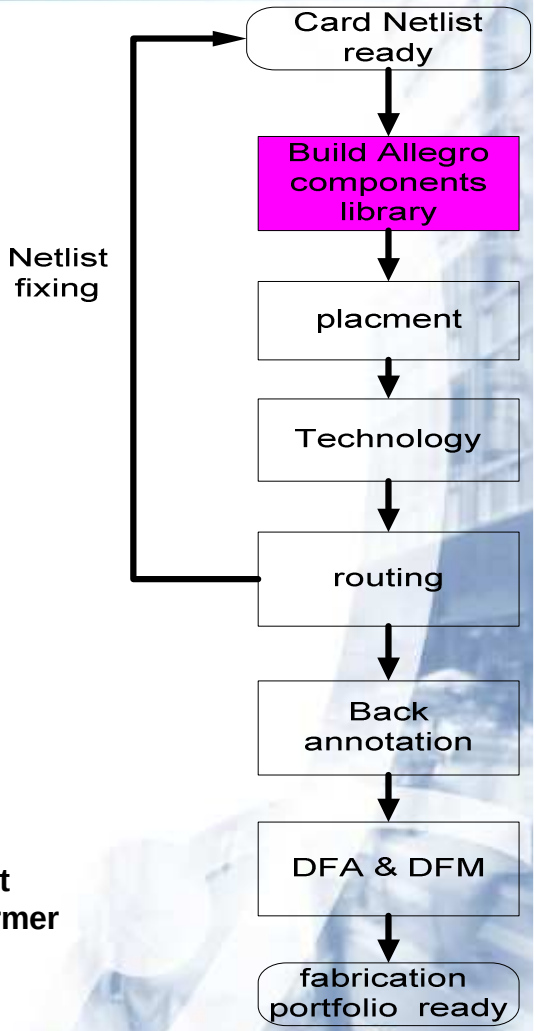


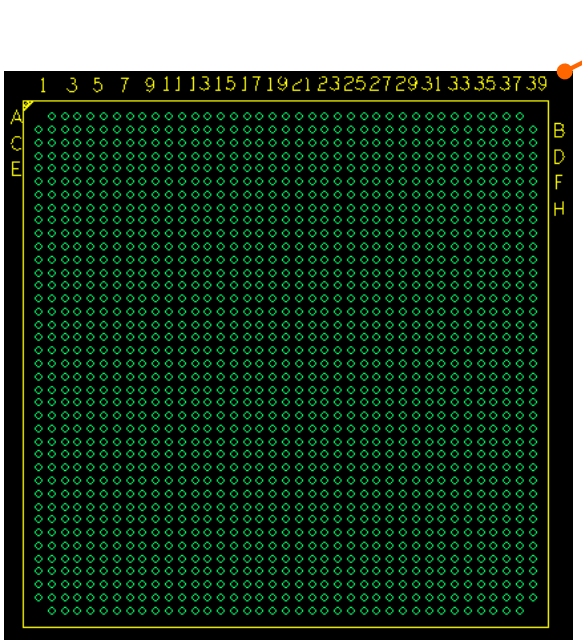
Ethos NETWORKS

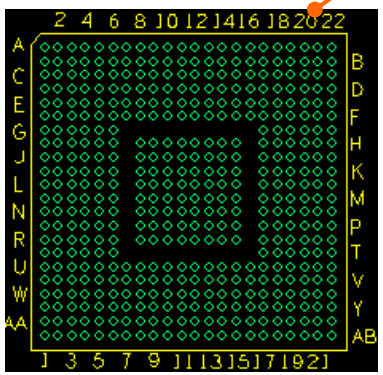
Layout Flow with Allegro

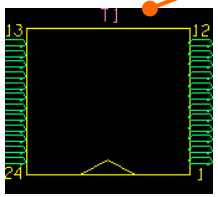
Components Building:

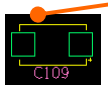
- *All datasheets should be ready before passing netlist*
- *All components were built with control of Ethos and checked to fit datasheets and part numbers*











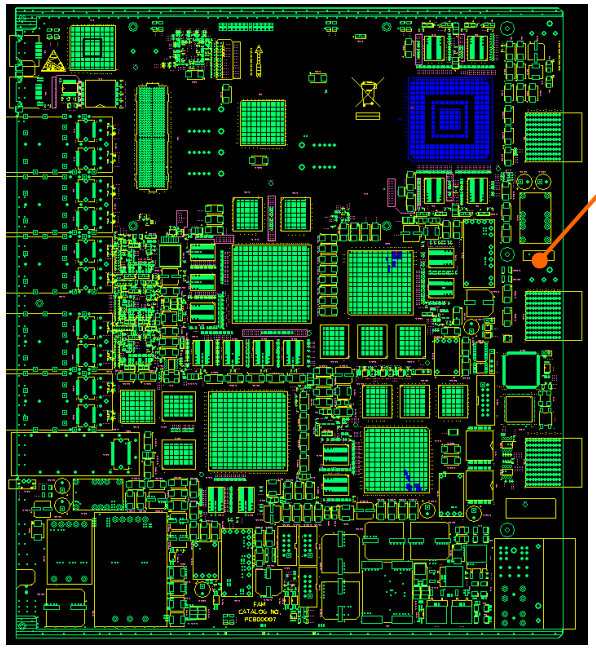
Ethos NETWORKS

** Layout pics courtesy of Oranit-PCB LLD*

Layout Flow with Allegro

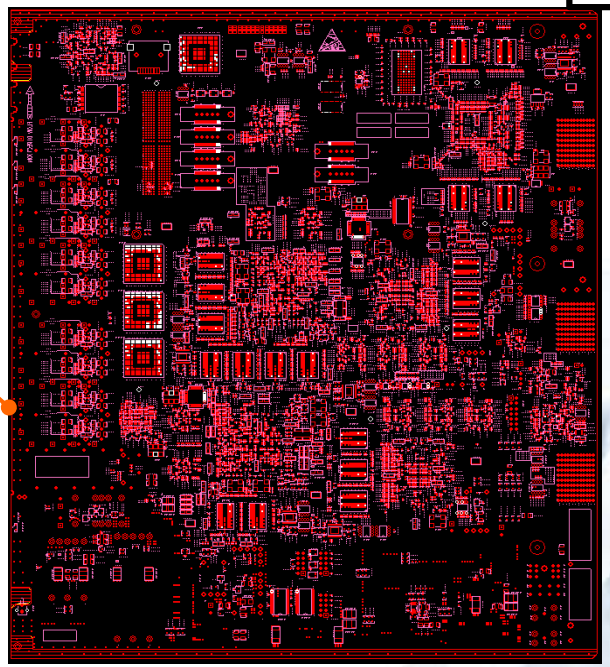
Card Placement:

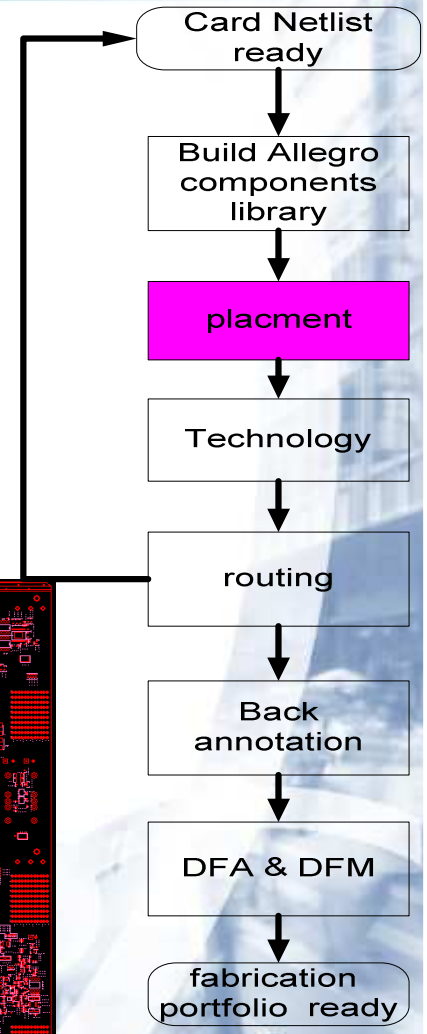
- *DXF should be ready prior to placement*
- *Placement according to thermal simulations*
- *Final placement to be confirmed by thermal, mechanical & technological engineers*



ELIC20 CS

ELIC20 PS



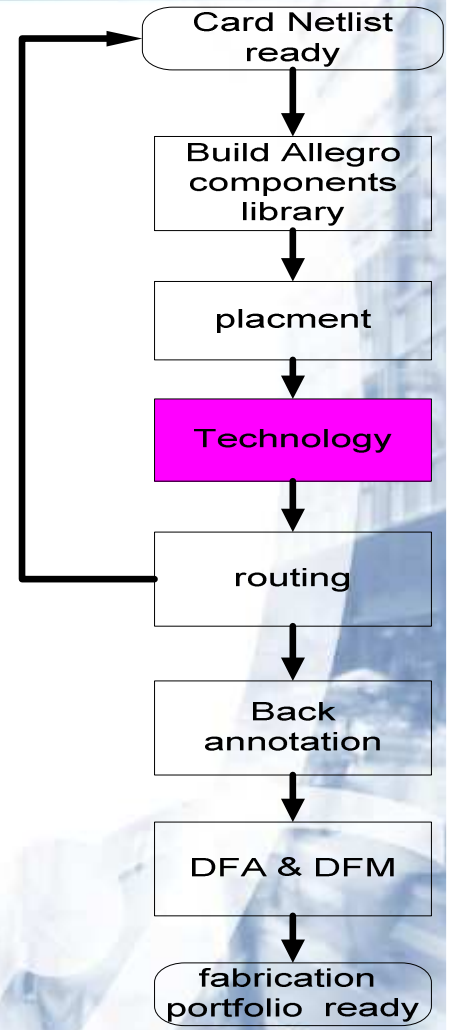


Ethos NETWORKS

Layout Flow with Allegro

Technology:

- *Stack-up should be ready before routing starts (including power planes and EMC issues)*
- *All library components checked by technologist to confirm pad size, etc…*
- *Simulation of microstrip, or stripline done for single ended and differential pairs of each layer.*
- *All technology aspects confirmed by PCB manufacturer and card assembly factory*

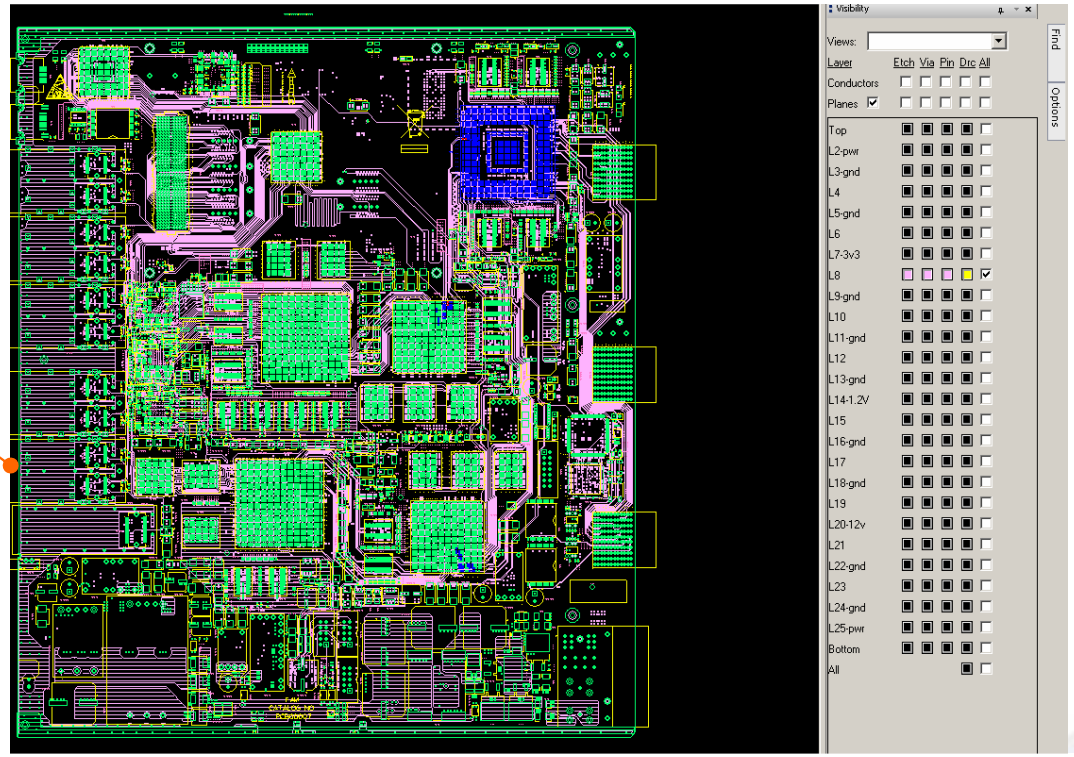


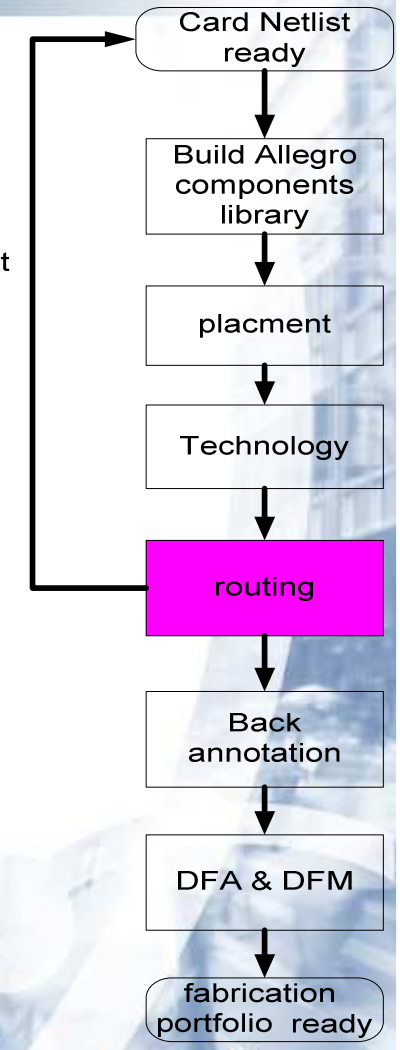
** Technology support by Invitech, Mr Victor Shimoni*

Layout Flow with Allegro

Routing:

- *25,000 nets routed manually ~ 3 months*
- *Routing starts at fan-out of all components at placement phase*
- *Routing takes into account netlist bugs*





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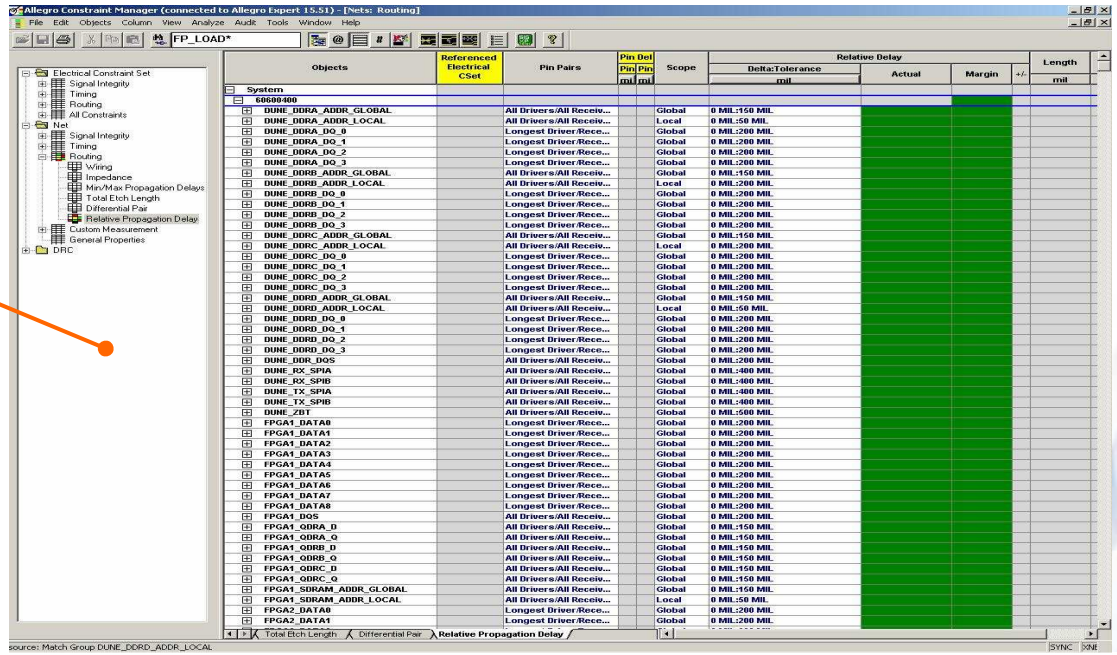
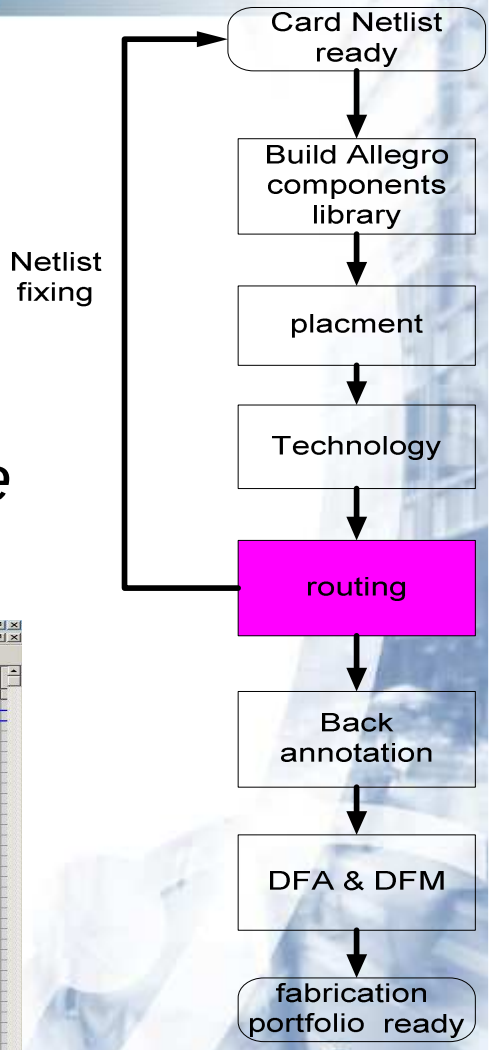
Layout Flow with Allegro

Routing & Constrains:

- *Around ~1,000 constrains made at schemes drawing phase*
- *Constrains help to control & find bugs at routing phase*
- *Fixing routing according to constrains can take around 3 weeks*





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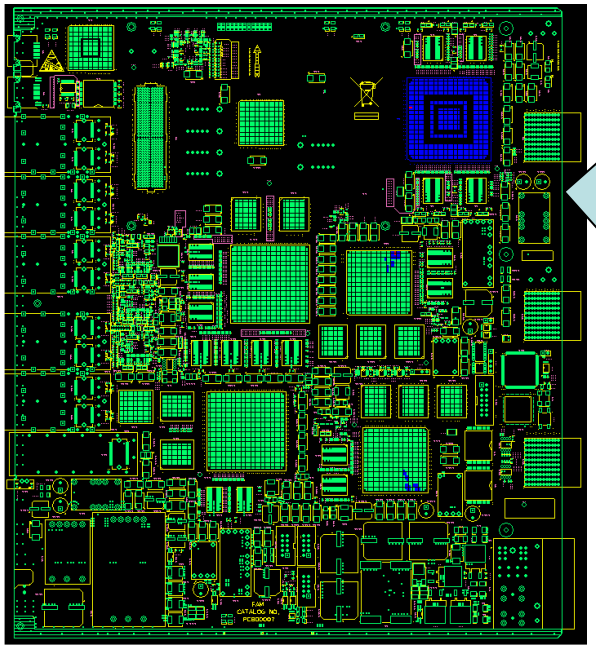
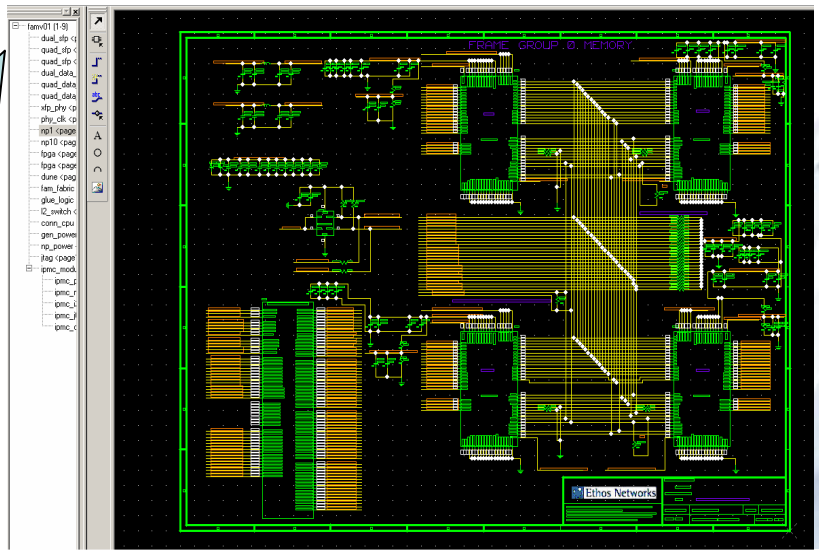
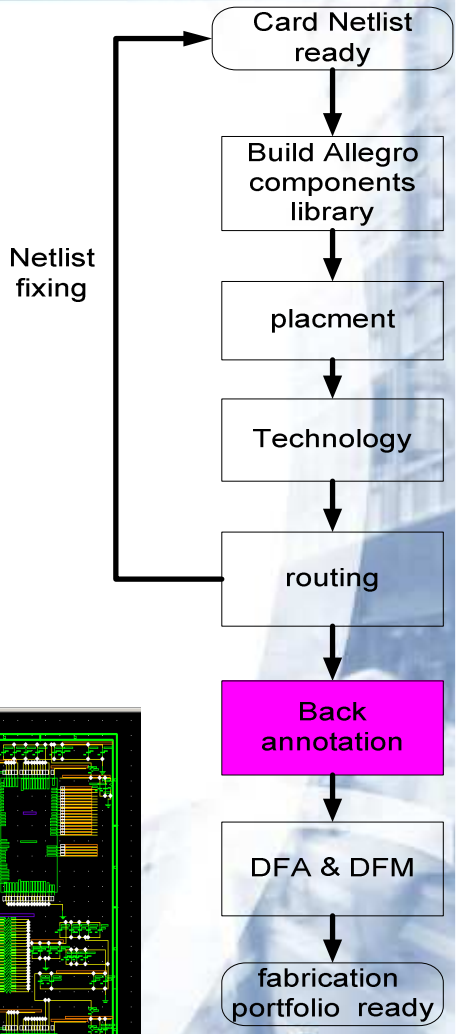
Layout Flow with Allegro

Back Annotation & Silk:

- *Silk & refdes should be back annotated to design Concept HDL*
- *Small areas of layout can be back annotated*
- *All 0402 components were removed from silk (hard to debug)*







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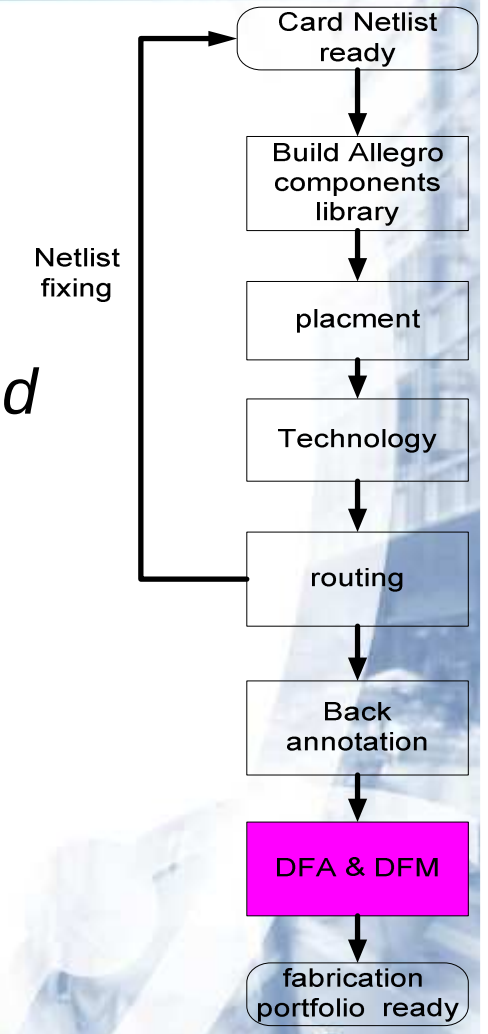
Layout Flow with Allegro

DFM (Design For Manufacturing):

- *All cards routing passed Valor manufacturing tests (net-to-via proximity, etc…)*
- *Around 12,000 errors where discovered & fixed*

DFA (Design For Assembly):

- *All cards passed Valor assembly checking for placement problems*
- *BGA keeps 2.5mm from all sides for possible conflicts at work around*



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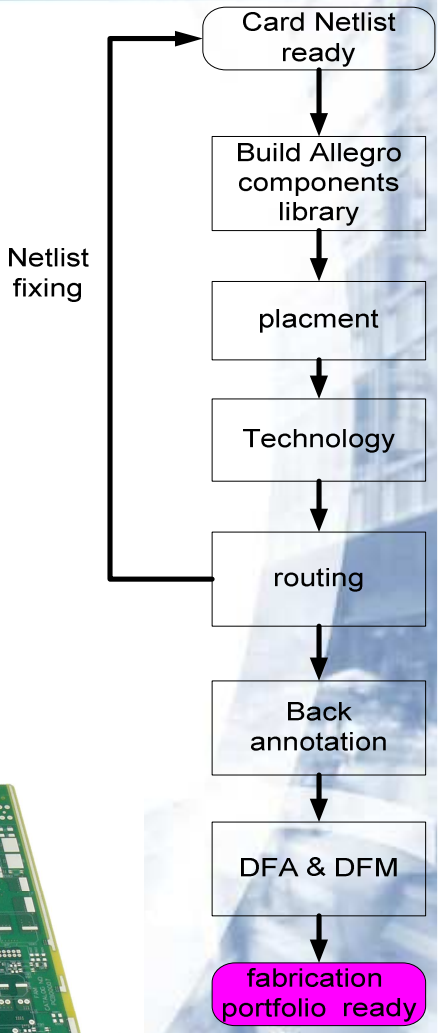
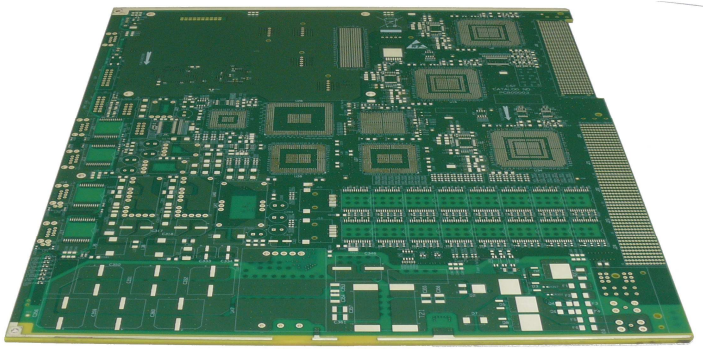
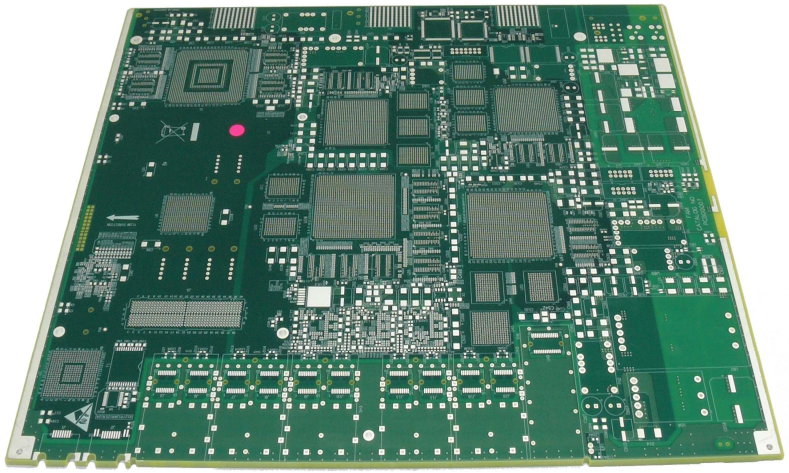
Layout Flow with Allegro

Fabrication Portfolio Ready:

- *All DFA, DFM, Thermal, Mechanics, Technology aspects tested and checked*
- *Gerbers, ODB databases sent to PCB and assembly manufactures*
- *Standard PCB (through VIA's) delivered within 5 working days*
- *Laser 1-2 ,1-3 PCB (HDI technology) delivered within 10-12 working days*







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Allegro Summary

Advantages:

- *Team sharing and integration (at peak time up to 8 layout designers worked together)*

Possible Improvements:

- *At final stages of layout ,large files were hard to manage*
- *Back annotation to Concept need to have better support of instantiations blocks*

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VoD

IPTV

Mobile Backhauling

One network

Hundreds of SLAs

Ethos FPGA Design with Incisive Enterprise

FPGA Design with Incisive Enterprise

DynTE™ (Dynamic Traffic Engineering) FPGA :

- *10Gbps full duplex SPI4.2 based interfaces*
- *5 x DDRII @ 667Mbps interfaces*
- *3 x QDRII @ 250MHz*
- *800 functional I/O's*
- *Equivalent of 4Mgates of ASIC*
- *All components written in Ethos and Ethos-IP*
- *Verification under Linux RH enterprise 4.0 x64bit version*
- *Incisive Enterprise 5.8 edition*

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FPGA Design with Incisive Enterprise

Block Functional Specification :

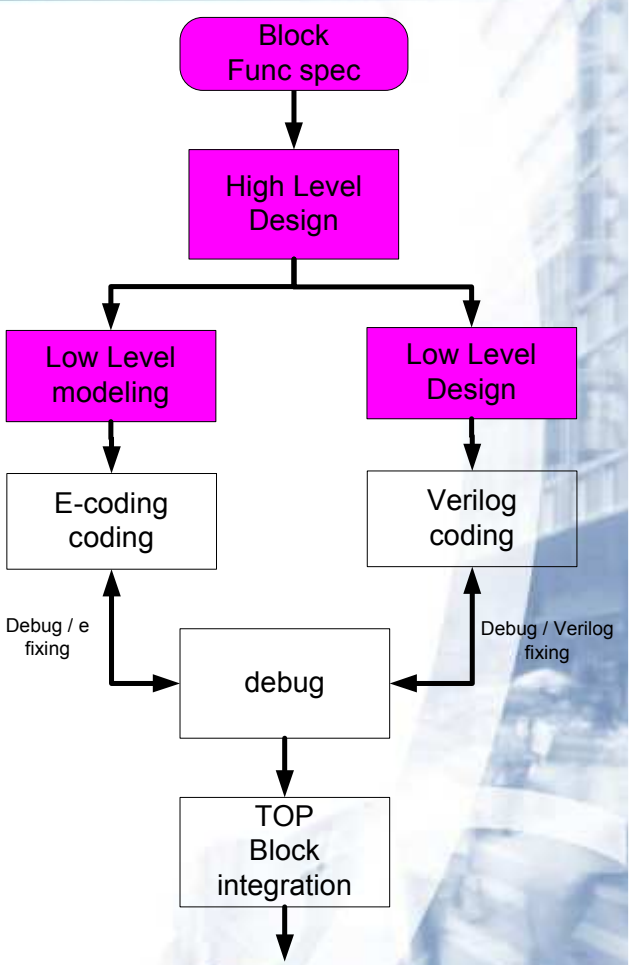
- *Functional specs were written for each block*
- *All blocks are part of TOP functional spec*

HLD (High Level Design) Documents :

- *HLD is written for each block*
- *From HLD each team writes the LLD*

LLD (Low Level Design) Documents:

- *LLD is detailed down to logical gates before code writing starts*
- *E-coding referring to block HLD only*



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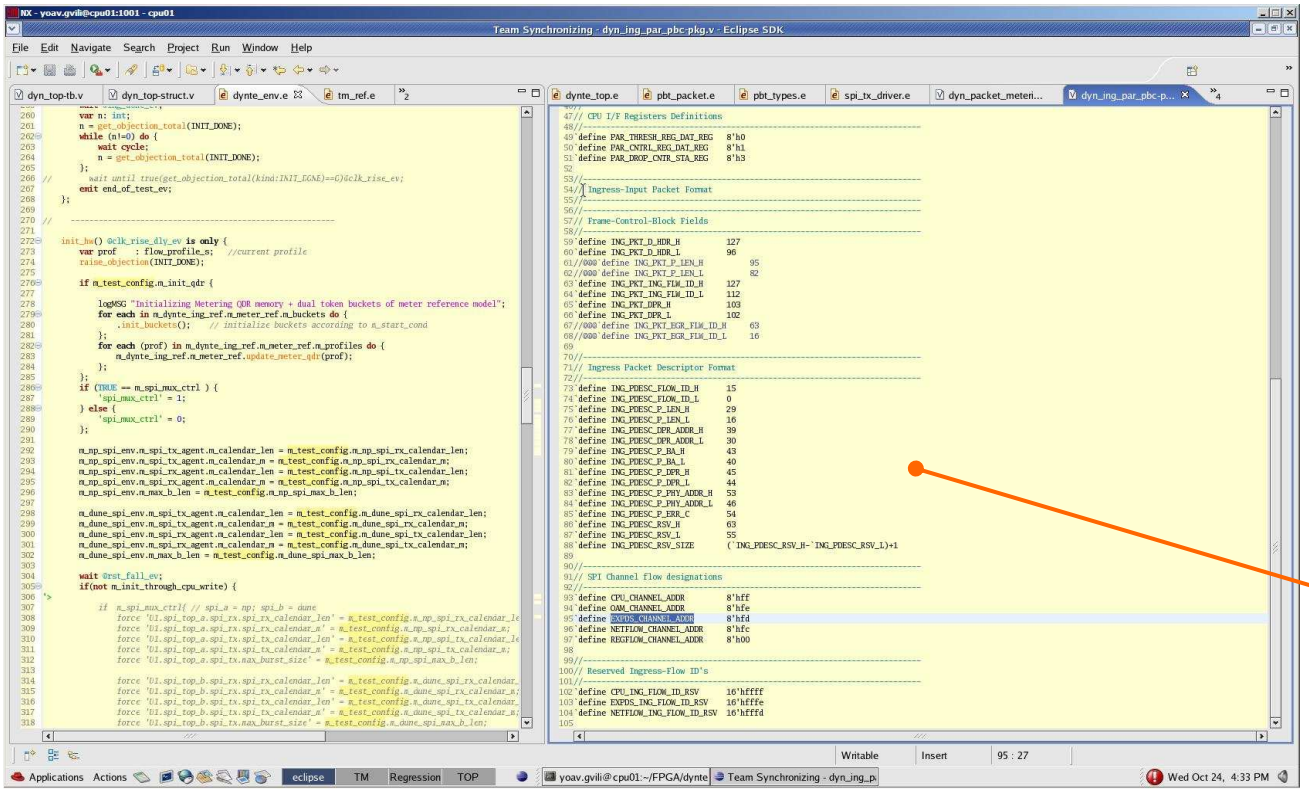
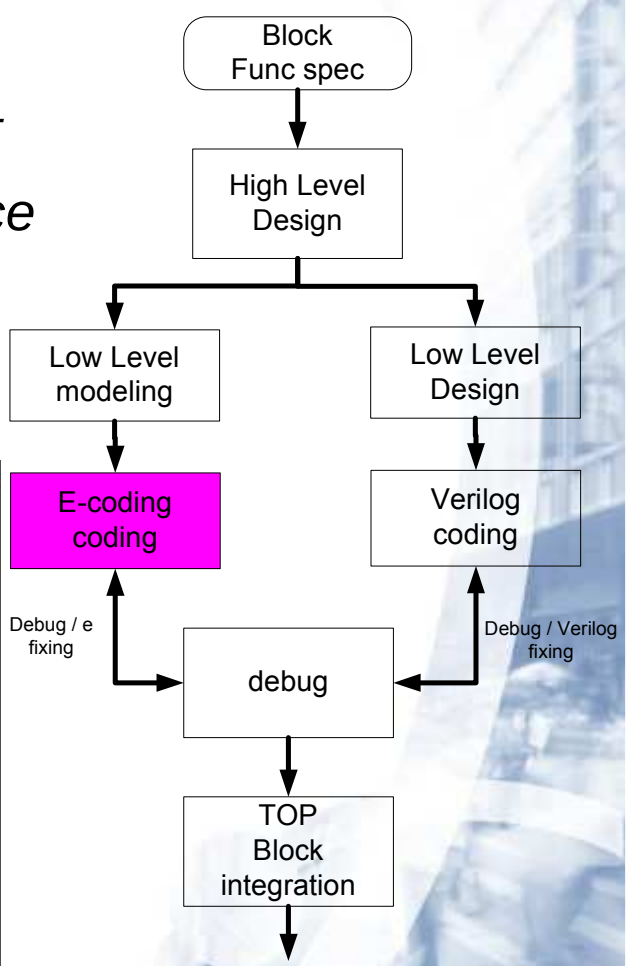
FPGA Design with Incisive Enterprise

E-coding:

- *E-code coded at Eclipse Open-source environment*
- *E-code is version controlled within SVN open source tool*
- *eRM methodology reduces coding time (interfaces, chip level reuse)*





Eclipse environment Support e-language color coding

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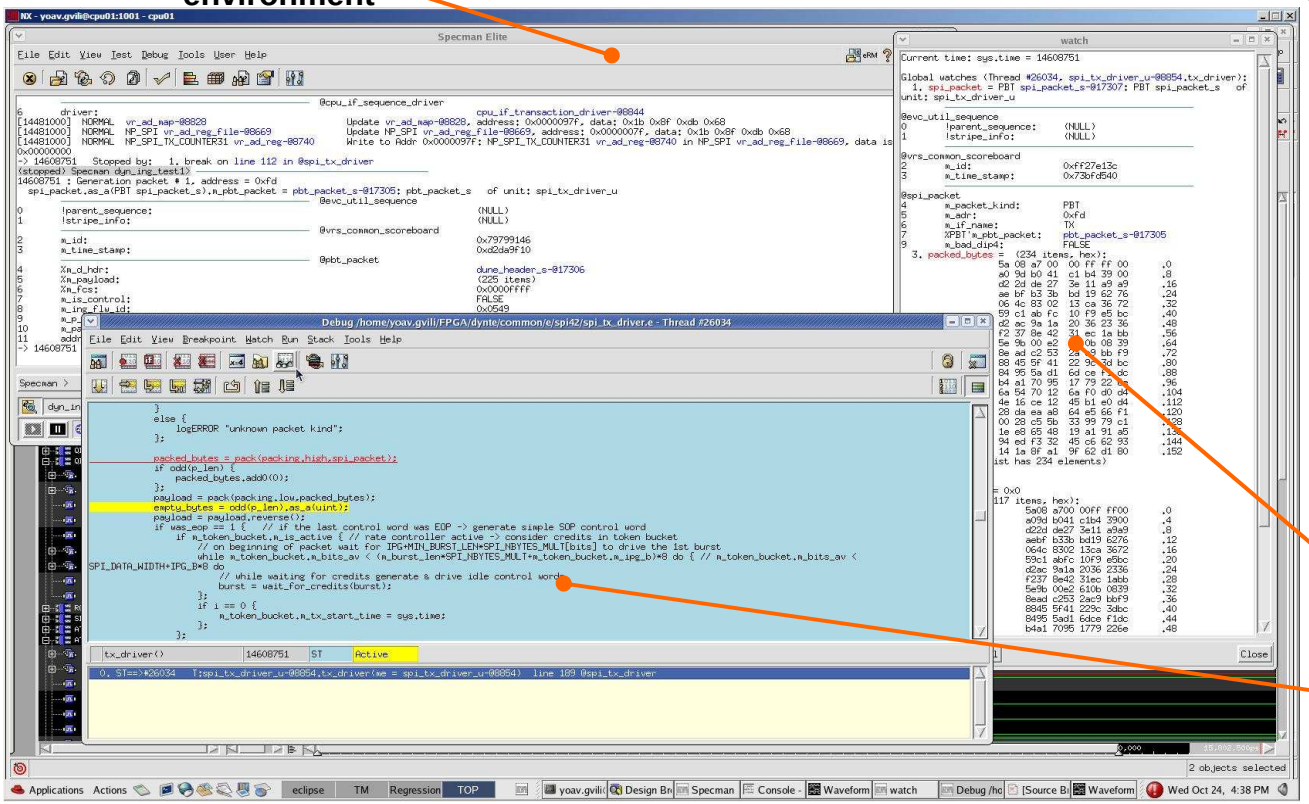
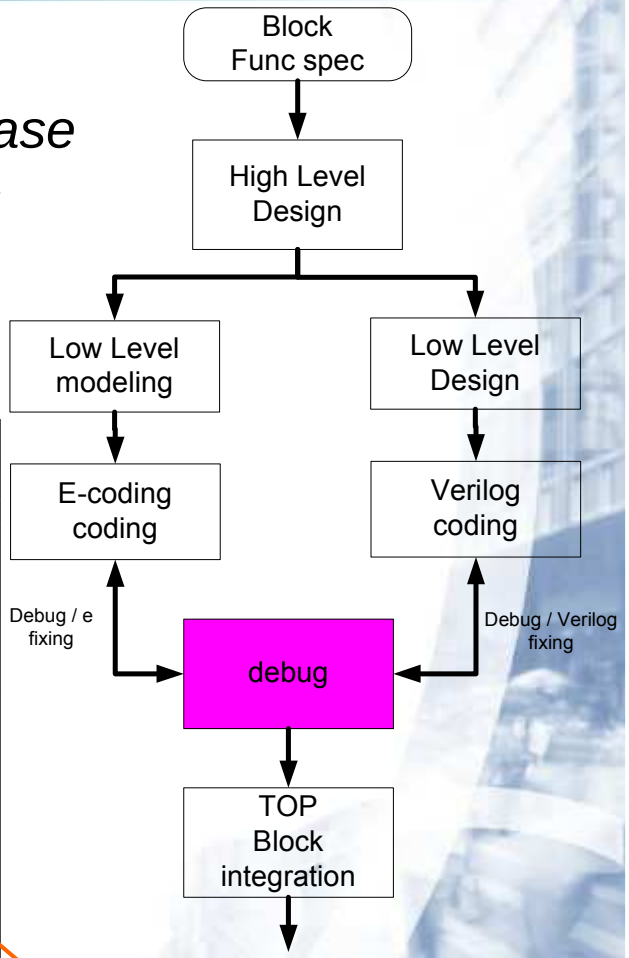
FPGA Design with Incisive Enterprise

Debug:

- *E-code and V-code are prepared prior to debug phase*
- *Bugs are documented in Bugzilla Open-source tool*
- *Debug of each block includes coverage function*





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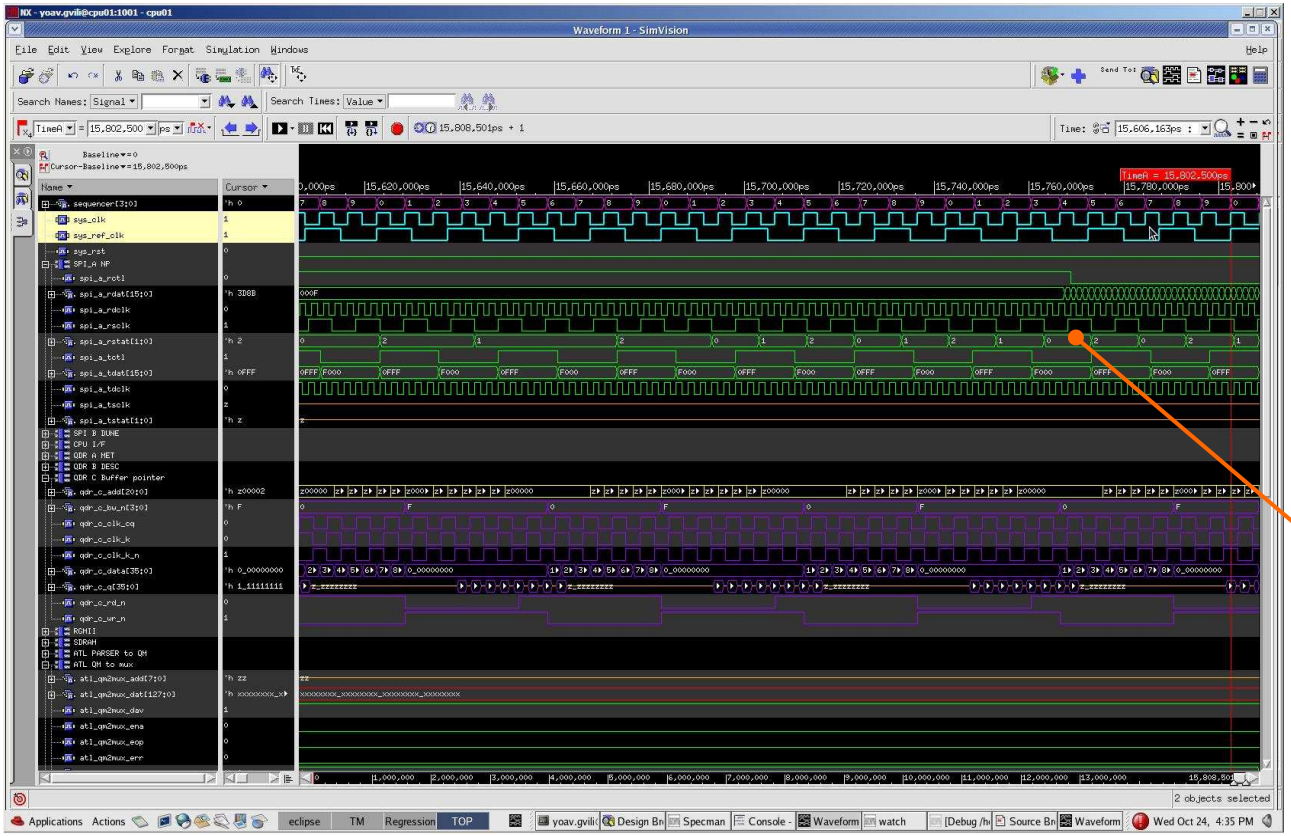
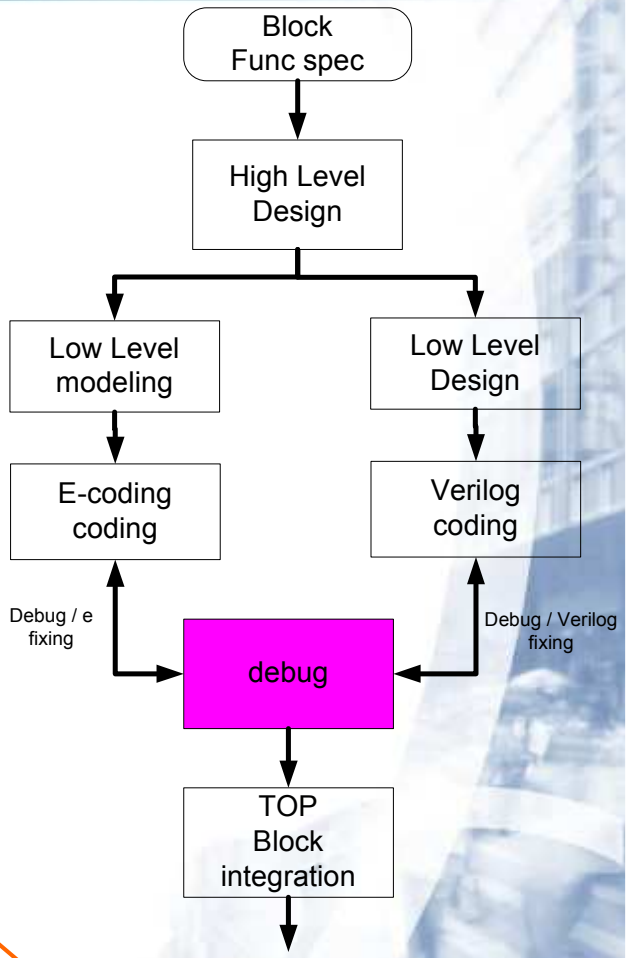
FPGA Design with Incisive Enterprise

Debug:

- *Integrated environment of ncVerilog & Specman helps reduce simulations cycles*
- *Full chip logical simulation run for 8 hours*





SimVision environment wave forms

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FPGA Design with Incisive Enterprise

Advantages:

- *Bugs found by verification reduce the lab debug cycle*
- *eRM writing methodology reduce coding time*
- *VR_AD of CPU (great model !!) reduced time and coding of CPU interface (register and memory model package)*
- *IE enable excellent team work methodology*

Possible Improvements:

- *Integration of IE tools will reduce time at simulation stage*
- *Support of IC (DDR, QDR etc..) models to improve simulation time*

Ethos NETWORKS

Thank You

Ethos - es [NL, fr. GK *ēthos*] character, sentiment, the guiding beliefs, standards, the spirit that motivates the ideas