

# An Advanced Fabrication Array Utility

Dave Elder CDNLive, September 2006



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# Agenda

- Introduction
- Definitions
- Advantages & Disadvantages of Arrays
- Possible Methods
- Array Tool Requirements
- Steps
- Tool Summary
- Demonstration
- Future Enhancements
- Q&A



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# Introduction

- An "Assembly Array" is an arrangement of one or more single PCBs on a single fabricated board.
- An array enables an assembly house to store and populate boards more efficiently than is possible with small individual boards.
- Who should design the Array?
  - Fab house?
  - Assembly house?
  - Mechanical?
  - PCB Designer?
- What tools are available?



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## Definitions

- PCB
  - Individual board.
- Array
  - Assembly array (or pallet). As opposed to a fabrication "panel".
- Panel
  - Fabrication panel. May be an "array of arrays".



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### **Advantages of Arrays**

- Standard assembly array sizes.
- Space for tooling holes and edge conveyors.
- Less need for carriers.
- Surface mount machines run at higher efficiency.
- Fewer handling issues



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## **Disadvantages of Arrays**

- Breaking-out individual boards can be difficult and add extra cost to the assembly process.
- Large arrays with many routed slots or v-scores become weak and can add to bow and twist problems.
- Less efficient use of the fabrication panel.



## **Possible Methods**

- Create a requirements document or diagram and ask the PCB fabricator to design an array accordingly.
- Use a 3rd-party tool such as GC-Cam CAM350 or Valor.
- Hand the problem over to the assembly house.
- Develop code in C++, Java etc.
- Develop Allegro Skill code.



## **Array Tool Requirements**

- The user interface should be familiar to designers who will probably only use it occasionally.
- Individual (embedded) boards within the array should reference the source board rather than be a copy.
- Quick design (and re-design) of arrays.
- Re-useable.



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# **Array Specification File**

A corporate "Array Specification" file stores design data common to board technologies.

- Preferred array size
- Array edge clearance requirements
- Default routing and v-score tool sizes
- Relative locations of tooling holes and fiducials



# **Step 1: Preliminary Array Layout**

Standard Skill Forms



Array Utility	
Design Array Boards V-Scores Routes\Tabs Fe	eatures Outputs
Array Specification File	Valor Folder for Array Re-use Load
Array Size Lower Left: X 0.0 mm Y: 0.0 mm Round Array Corners Radius: 4.0 mm	Length: 230.0 mm Width: 157.0 mm
Array Edge Rails Component Keepout Areas Ends Top: 0.0 mm Bot: 0.0 mm IT Ends Supported during reflow?	Sides Top: <u>5.0</u> mm Bot <u>5.0</u> mm I Sides Supported during reflow?
Reserved Side Strips       Left     10.0       Right     10.0       mm     Imm       Imm     Allow       C     Keep out	Top: 10.0 mm C Allow C Keep out Bottom: 10.0 mm C Allow C Keep out
Vertical Axis De-Panel Method	Horizontal Axis De-Panel Method
Router Tool Diameters Border Tool: 2.4 mm Inter-Board Tool: □ Plate array edge Copper Relief: 0.20 mm	2.4 mm Board Tool: 2.4 mm
Preferred Board Rotation: AUTO degrees Calculated Array 1 x 6 Total: 6 V Preview	Build F Keep board locations F Keep tooling holes Keep array fiducials F Keep all routes etc. Build Array
Default Layer View C	luit Save Design
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# **Step 2: Array Layout Optimisation**

#### • Preview alternatives



Array Utility	×
Design Array Boards V-Scores Routes\Tabs Fe Array Specification File tait-standard TeleBrowse Reload	atures Outputs Valor Folder for Array Re-use
Array Size Lower Left: X 0.0 mm Y: 0.0 mm ✓ Round Array Corners Radius: 4.0 mm	Length: 2000 mm Width: 157.0 mm
Array Edge Rails Component Keepout Areas Ends Top: 0.0 mm Bot 0.0 mm Ends Supported during reflow?	Sides Top: 5.0 mm Bot 5.0 mm I Sides Supported during reflow?
Reserved Side Strips       Left:     10.0       mm        • Allow       Right:     10.0       mm        • Allow       C     Keep out	Top: 10.0 mm   Allow C Keep out Bottom: 10.0 mm  Allow C Keep out
✓ Vertical Axis De-Panel Method         C Route         ✓ Score Parameters         ✓ Score       ☐ Jump score if required         Tool:       0.8       mm         ✓ Butt edges       Inter Board:       2.4       mm	Horizontal Axis De-Panel Method      Route      V Score Parameters      V Score I Jump score if required      Tool: 0.8 mm Relief: 0.20 mm      Butt edges Inter Board: 2.4 mm
Router Tool Diameters Border Tool: 2.4 mm Inter-Board Tool: ☐ Plate array edge Copper Relief: 0.20 mm	2.4 mm Board Tool: 2.4 mm
Preferred Board Rotation: AUTO ▼ degrees Calculated Array 1 x 6 Total: 6 ▼ Preview	Build F Keep board locations F Keep tooling holes Keep array fiducials F Keep all routes etc. Build Array
Default Layer View     Q	uit Save Design
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### **Step 3: Build Array**





## **Step 3: Add Routes**

😼 Array Utility 📃 📃 🔀
Design Array       Boards       V-Scores       Routes\Tabs       Features       Outputs         Automatic Add Routes
Hole: 1 mm Web: 0.5 mm Cnr Offset 0.5 mm
Set Breakoff Tab Parameters         Change Breakoff Tabs         Select Tab:       Clean edge       Holes:       4       Change Breakoff Tabs         Small Holes:       0.8       mm       Padstack:       U0MM8       Edge Dist       -0.125       mm       Pitch:       1.0       mm         End Holes:       1.2       mm       Padstack:       U1MM2       Edge Dist       0.25       mm       Pitch:       1.25       mm
Add Breakoff tabs       Add Tabs       Add Tabs       Add n Tabs       Distance between tab centres:       30
Edit     Add Route Line     Delete Route Lines       Delete Breakoff Tabs     Break Route Lines     Delete Route Segment
Move Breakoff Tabs     Image: Copy Tabs to other boards     Save All Breakoff Tabs       Replicate Breakoff Tabs     Save Tabs
Export Tab Keepouts for Checking Export Tabs
Default Layer View     Quit     Save Design



## **Step 3: Tidy Routes**





#### **Step 4: Add Features**





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# Step 5: Drill Legend

	Desting America Destroy Take [ Destroy Take ]
Allegro PCB Performance option L: 220-01720-05A_array.brd Project: H: /Designs/arrays	Design Array   Boards   V-Scores   Routes ( ) abs   Features   Outputs
File Edit. View Add Display Setup Shape Logic Place Route Manufacture Tools Valor Array Tools Help System Admin	Array Dart Number
	Array IPN: 123-45678-0001 🗹 Auto-update array IPNs
الهيبوغسفا المسافا لتربيها التعسيم فمفقة تربيهما الكفكيتي فتعمقه فمعمقه فيبرونه المساف	
	Documentation
	Add Drill Legend(s) Add Array Dimensions Dimension units:
	Paste Stencil Border(s)
	Add Top Stoppil Porder
لوسوعت المسالي الموسية المتقدية ومستنا والمحاوية والمحاوية ومستنقد ومستعيني والمحاوية وال	
	Array Outputs
	Full ODB++ Outputs M Include Paste Film(s)
· · · · · · · · · · · · · · · · · · ·	Stongil ODB++ Outpute
ALL UNITS ARE IN MILLIMETERS	
HOURE STEE TOLERANCE PLATED OTF	
0.9 .15/.15 PLATED 108	
● 1 0 + 15/	
6 1.0 →.15/15 PLATED 2	
→ 1.6 +.15/15 PLATED 24	
© 2 2 + 20/20 PLATED 6	
• 0.6 +.057-105 NON PLATED 120	
€ 2.4 +.05/05 NON PLATED 4	
▲ 3.0 +.05/05 NON PLATED 8	
▲ 33 + 05/05 NON PLATED 24	
Loading extcore.cxt Command >	
	L Detault Layer View Utilt Save Design



# Step 6: ODB++ Outputs

🚹 Valor Universal Viewer: 220-01720-05a_array [Styp: array]	Design Array   Boards   V-Scores   Routes\Tabs   Features   Outputs
<u>File View Selection Actions Options Step Windows Help</u>	Array Part Number
<b>□ □</b> <u>▲</u> <b>□</b> <del>•</del>	Array IPN: 123-45678-0001 🔽 Auto-update array IPNs
<pre> sst sst sst sst sst ssb ssb ssb ssb ssb</pre>	Documentation         Add Drill Legend(s)       Add Array Dimensions       Dimension units:       mm         Paste Stencil Border(s)         Add Top Stencil Border       Add Bottom Stencil Border         Array Outputs       Include Paste Film(s)         Stencil OpB++ Outputs       Include Paste Film(s)         Stencil OpB++ Outputs       Include Paste Film(s)
x = 0.413022", y = 6.534080" Selected : 0	Default Layer View     Quit     Save Design



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## **Tool Summary**

#### Output is ODB++

- Handles nested boards
- Generally accepted format
- Open source standard
- Embedded in Allegro
- Creates a Mechanical symbol (bsm) for each design used in the array.
- Other features added or changed using standard Allegro User Interface.



#### **Demonstration**





### **Future Enhancements**

- Nested arrays
  - Would enable several arrays to be used in a single fabrication panel. This could reduce PCB fabrication CAM set up costs.

#### Improved help and documentation

Currently very little documentation exists for the flow or features.



