Full Chip Verification Flow with AMS Methodology

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Introduction

The combined Top-down/Bottom-up AMS methodology has been successfully used in SanDisk ASIC group for full chip verification. This full chip includes analog blocks, Verilog functional views and 3rd party IPs (CDL netlists). AMS methodology enables engineers to use the components of the design in its native form, whether it be Verilog, schematic or CDL. "Schematic on Top" and "Verilog on Top" verification methodology have been tested and applied in this project. This mixed AMS methodology can help customer to catch up the design problems in early stage, enable customers to run analog/mixed-signal full chip functional verification instead of power up sanity check thanks to the performance of AMSUltra simulator. This AMS methodology will be used to improve SanDisk internal CAD methodology flow, for easier CAD support and higher productivity. This paper provides details about our old flow and newly implemented AMS flow, together with experimental results.

1. The Old Flow

The original flow was to use VerilogIn to convert gate level Verilog code into schematics. From here the in-house pure analog blocks were stitched into the design. The 3rd party IP left as empty schematics only having ports. The schematics need to be converted into a spice netlist to work with the CDL files, and this requires pin order correction (manually or by script). This is a three stage conversion process before even getting to the simulator; four stages if starting form RTL. RTL→Gate-Level Verilog→Schematic→CDL.

The overhead for conversion alone goes exponentially when chip designs become more complicated. Automated conversion is not always 100%, something will be lost in translation. Therefore the design becomes less pure. Bigger designs take a longer time to simulate, even with FastSpice simulators. Time overhead + design purity loss + trade-off between simulation time and accuracy = Risk.

2. The Newly Implemented AMS Methodology

What is new is the methodology to utilize the tools. The first stage is to understand your own design then break up the design into smaller libraries. Cells that are used by other designs should be in their own library, such as standard cells and primitives. Large digital only or analog only cells should have their own libraries. When done right, these libraries only need to be complied once, and can be excluded when having to re-compile the top design. Once a layout has been made the import process can begin. Do not use VerilogIn; instead use ncvlog. ncvlog will add a functional view to the Library Manager. The functional view is a link to the Verilog file that was read. If the functional view is open within Cadence environment, a text editor will come up.

Symbol views can be used as a medium among the Verilog, schematic, and CDL designs, but only create symbols were they are needed. This comes in handy when using the Hierarchy Editor (HED) -- a powerful tool. For example, a symbol for a nand gate may be placed in a schematic. This cell has no schematic view of its own, but it does have a functional view. The symbol is used to declare the cell is being called and how to connect it to the rest of the schematic. HED can be used to decide what view to be used,

in this case functional. Another example would be to have the parent cell as Verilog. Using the HED we can switch the simulation view to use schematic or symbol views. If the view is set to symbol, the AMS will use the CDL definition of the cell that it found in the attached Analog Models. The HED and ncvlog together minimizes the need of convertion, plus the flexibility and freedom to create variations of the same design. Examples of variations can be found in Table 1.

Table 1: Configuration Examples

Config	Analog	In-House IP	3rd Party IP	Other IP
ConfigA	Schematic	RTL	IP (Functional)	RTL
ConfigB	Schematic	Verilog Gate	Verilog Gate	RTL
ConfigC	Schematic	Verilog Gate	CDL	RTL
ConfigD	Schematic	RTL	CDL	RTL

AMS uses connect modules to translate the signals between analog and digital cells allowing them communicate. There are 3 types of connect modules: Analog-to-Digital, Digital-to-Analog, and Bi-Directional. Connect modules are automatically inserted when they are needed. Cadence provides the common connect modules that would be used, and users have the option of creating new modules for customization purposes. Figure 1 is an example of Analog-to-Digital of the signal VDD. The signal VDD_$flow is the current of the VDD. The analog devices that are powered by VDD still affect its current and can be monitored.

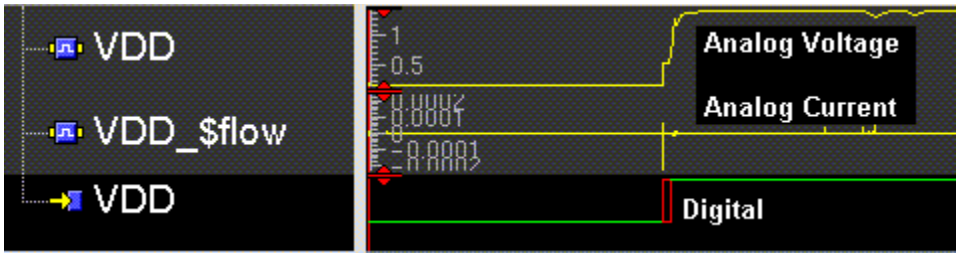

Figure 1: AMS Analog & Digital VDD

Digital simulations are faster than analog simulations, but analog simulations are more accurate than digital. AMS allows users to decide how and where to manipulate the views, accuracies and speeds via the Hierarchy Editor. With the proper mix of analog and digital components, a full chip can be simulated quickly with accuracy where it is needed. Table 2 shows the simulation times of the same chip design using different simulators and the condition that they were simulated in.

Table 2: Simulation Results (one million gate design)

Simulator	Simulation Time	Notes
(Other Simulator)	4 *Days*	Full Chip Transistor
Ultrasim	9 Hours	Full Chip Transistor + VR[1]
AMSUltra	5.3 Hours	Verilog + Transistor

Simulation time is not the only benefit. The time that a full chip simulation can begin is dramatically sooner. In the old methodology full chip simulations needed to begin after the design is ready. With AMS methodology full chip simulations can be started the moment the first preliminary netlist is made. Swapping in newer and final components as they are created is all that is needed before being able to run all the necessary tests and

[1] VR is an Ultrasim option that specifies one block as a voltage regular circuit so that Ultrasim will not partition it during simulation. This option helps to speed up simulation in circuit that contains voltage regulator.

verifications. By the time the final netlist is completed debugging should also be completed. Figure 2 shows a timeline comparison of the older methodology versus AMS in relation to the start and tap-out of a design.

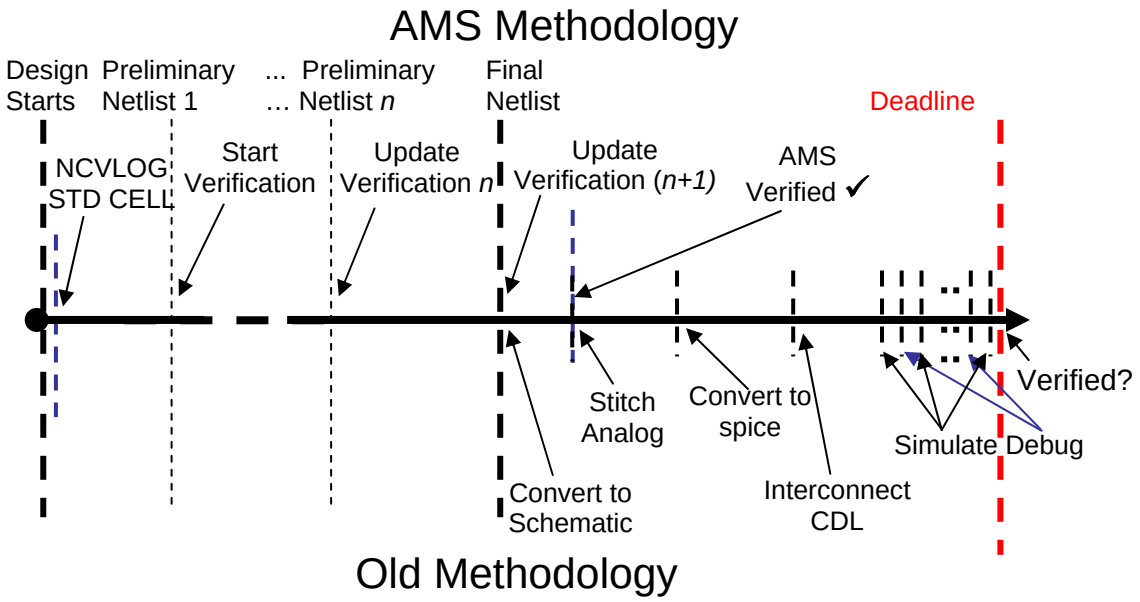

Figure 2: AMS Methodology Timeline

3. Summary

We successfully applied the AMS methodology in re-simulating old projects. Using the same Verilog and CDL files that we stated with the old project, we started the project as though they were new. Using the new mythology we bought-up the full chip with a mix of analog and Verilog, and then compared the AMS results with our original results. We verified the performance improvement and confirmed that the AMS methodology will be our mixed signal verification solution.

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