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# Constraint Manager

## Moving designs from 15.2 to 15.7

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Session # 7.15

Presented at

**cadence designer network**



**Silicon Valley 2007**

## Introduction

*Harry Bartley has supported Cadence schematic capture tools for Tektronix for the past 15 years. He has worked in various aspects of CAD/CAE for over 30 years.*

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### Focus of the Paper

*The information presented in this paper is based upon design processes at Tektronix that have evolved over a period of years with assistance from Cadence.*

*Cadence has been introducing the Constraint Manager over the past several years. With each release, new features have been added and old features have been modified. In this constantly changing environment, our designs and design processes have had to change to take advantage of the new features without losing design data or capabilities.*

*The focus of this paper is on the unique problems associated with releases 15.2, 15.5, and 15.7, and the process steps required to move a constrained design from release 15.2 through release 15.5 to release 15.7.*

*To understand the process, it is helpful to understand Schematic States, Schematic Styles, and*

*the interaction of Occurrence Editing and the Constraint Manager. Additional related reference information is placed at the end of this article.*

### The Question

*How do you move a design from and earlier release, 15.2 or 15.5 into release 15.7? What problems are being left behind, and what new problems have emerged?*

### A Little History

*In the old Concept SCALD designs; all of the properties had to be placed on the schematic. The process was called "Correct by Design", and it allowed the EE to control critical trace layout as the schematics were being created. At Tektronix we typically used the following properties: delay\_rule, matched\_delay, differential\_pair, net\_physical\_type, and net\_spacing\_type.*

*To handle the ever increasing number of constraints, Cadence added the Constraint Manager. The Constraint Manager recognized properties that existed on the schematics, and allowed the addition and modification of properties in the Constraint Manager. The winning constraint value was stored in the Occurrence Property File "OPF".*

## **Basic Problems**

*This combination of tools had problems with speed and synchronization. The Constraint Manager worked well with simple designs, but was very difficult to use with complex designs. Using the same block more than one time in a design created problems with `relative_propagation_delay` group names (`matched_delay`), `differential_pair` names, and reference designators used in pin pairs for `propagation_delay` properties (`delay_rule`). Shared designs were limited to one Constraint Manager at the top.*

### **Release 15.2**

*In the 15.2 release, there were many problems. Constraints could be placed as properties on the schematics, or they could be entered in the Constraint Manager. If the syntax of the property on the schematic did not read correctly into the Constraint Manager the property would not be "pushed" into the Constraint Manager. This would be reported one time, and then the information was stored in a `deleted.opf` file in the `constraints` directory. The problem still existed, but would not be reported unless you removed the `deleted.opf` file from the `constraints` directory.*

*The schematic contained constraint properties, but the schematic was not the master for the constraints.*

*Constraints could be entered into the Constraint Manager, and constraints could be changed in the Constraint Manager. Changes did not get pushed back to the schematics unless you performed `Constraints > Update Schematics`. Even then there were problems with bus signals. Properties attached to bus names would not be updated on the schematics.*

*The Constraint Manager was not the master for constraints.*

*The Occurrence Property File (OPF) was the master for constraints. This binary file could not be easily viewed, but it contained the last word for information that would be passed to layout. It was difficult to keep the schematic, Constraint Manager and OPF information in sync, and it took time. Occasionally it was necessary to delete a net from the schematics to get the constraint properties deleted from both the Constraint Manager and the OPF. Then the net could be added back to the design and assigned new properties.*

*These were general problems with all designs in 15.2.*

*What specific problems were associated with complex hierarchical designs?*

## **Complex hierarchical designs**

*The Constraint Manager would only read constraints from the top level of the design. If a block contained constraints, they had to be placed as properties on the schematics. You could not use the Constraint Manager on a block and then have those constraints recognized at the top design level.*

*If our design, Block A, has relative\_propagation\_delay, differential\_pair, and propagation\_delay properties, What can go wrong?*

*Each of these properties contains information that needs to be unique for each instance of the block. The group name in relative\_propagation\_delay is the same in every instance of the block. In layout, all of the nets from multiple instances of the same block are matched, not just the nets in a specific instance of the block.*

*The differential pair for two nets in the block becomes the name for four nets in two blocks. The differential pairs try to become one differential pair, and are incomplete, or incorrect.*

*Pin pairs used in propagation delay contain incorrect reference designators when the block exists multiple times. U14.1 becomes U14\_1.1 and U14\_2.1.*

## **Solutions / Limitations**

*How could these problems be resolved in the 15.2 release?*

*Several approaches were devised. Some Engineers created only flat schematics, even though the design had over 100 pages of schematics. They eliminated problems with bus names, blocks, and in general tried to avoid the Constraint manager entirely.*

*Others used simple hierarchy. They named each block uniquely. They had to carefully control multiple changes in multiple blocks. All of the groups avoided using Occurrence Edit as the primary method of making changes to the block constraints. The process was too manual, and the results were too hidden in ordinary usage.*

*A few complex designs forced the issue, and came up with involved processes to change and package their designs. In some cases this involved up to 37 steps and additional scripts to package the entire design. One project used multiple properties that were renamed as the schematic sheets were edited at the block level or at the design level. There was nothing easy or straight forward in the creation or maintenance of these designs.*

*The Constraint Manager in 15.2 would not read lower level constraints, so Engineers working on a common design had to place properties on their schematics. When their schematic block was incorporated into the master design, the properties were read into the Constraint Manager.*

### **Release 15.5**

*How did release 15.5 help, or hurt?*

*In release 15.5, the Constraint Manager could read lower level design constraints. That eliminated the need to have the properties on the schematics. The Engineer could use the Constraint Manager on his block schematics, and those same constraints would be read at the top level of the design. This also eliminated the problems with the differential\_pair names, the relative\_propagation\_delay group names, and the reference designators in the propagation\_delay pin pairs.*

*The 15.5 release still reads properties from the schematics, still has the OPF, and still has synchronization issues. The improvements in 15.5 allowed us to simplify our processes, eliminating some scripts, and eliminating the use of multiple properties.*

### **Problems 15.5**

*There were still some problems. The Constraint Manager would not update the values on the schematic properties. Running Tools > Constraints > Update Schematics at any time would destroy the schematic properties. We had to ignore the schematic properties if any changes were made in the Constraint Manager.*

*The Engineers had grown used to the properties, and were using them in design reviews. The values displayed on the schematics could be wrong.*

*Deleting a property from the schematic would delete the information associated with that net in the Constraint Manager. In 15.2 the schematic property could be deleted without affecting the Constraint Manager.*

*In 15.5 we could make the properties invisible, ignore the properties, or make all changes on the properties, and not open the Constraint Manager. These options were also limited by the type of design.*

*Knowing the limitations and risk, we moved some projects to the 15.5 release. The benefits were significant for those designs. We then discovered that there was a problem reading all of the properties into the Constraint Manager.*

## **Validation**

*We needed a way to verify that the constraints existing in a design in one release were still there when we moved to another release. We needed a method of validating the information.*

*We wanted to validate the packaged information. We felt that would limit problems that could be introduced by netrev, or PCB Editor. Working with Cadence, we could not find a file on the schematic side that contained the information in a format that could be compared from one release to the next.*

*Cadence helped identify a process we could use to validate constraints as we moved between different releases. In this process we create reports from PCB Editor. The number of steps involved makes it more difficult to perform. Here is an outline of the steps required to check a design created in 15.2 or 15.5 against the same design in 15.7.*

*Steps:*

1. Import logic into an empty board

*Using the existing packaged files from the older release, Import logic into an empty board. Problem solutions require PCB Editor knowledge.*

2. Create a Report file

*Open Tools > Reports load the customized report files*

*Cadence supplied a special report format that reduced the number of properties reported, eliminating a large number of blank columns. I reduced that to just the specific properties I know we are using. To create a report using the special report format, load the customized report files.*

3. Write a report

*Write a report by selecting a customized report as the template.*

4. In the 15.7 release  
File > Save Hierarchy  
This will indicate if there are any errors before you start working on the design.

*Tools > Constraints > Synchronize  
This step changes constraint properties on the schematic to placeholder properties.*

*Package the design – Export Logic*

*Import logic into an Empty board  
Run and save a report.*

5. Use VIM Diff, or your preferred editor, to compare the two reports. VIMdiff highlights differences.

*In complex hierarchical designs, there are differences in the group names automatically created for the relative\_propagation\_delay property. Look for any missing properties.*

*Even though this is not a simple straightforward process, it has helped identify specific problems, and has enabled designs to move forward with more confidence. There has been a need to do this type of verification when moving to new releases, or to new ISRs in the same release. Cadence has indicated they will have this as part of their testing in the 16.0 release.*

### **Release 15.7**

*Why move to the 15.7 Constraint Manager?*

*Most of the basic problems have been resolved in the 15.7 release. The Constraint Manager is the master for the constraints. Constraints are no longer stored in the OPF. After the initial synchronization of the design, constraints are no longer read from properties on the schematics. The schematic*

*may use placeholder properties to display the constraint values. Bus signals ownership of constraints has changed from the bit level to the top bus vector signal level.*

### **Problems**

*Even with the improvements, there are still some problems. The signal name used in the Constraint Manager will be the bus name at the root level of the design. If an unnamed signal connects two blocks, the constraints are associated with the unnamed signal.*

*When a net name is changed, and this happens constantly, the Constraint Manager makes the old name obsolete and attaches no properties to the new name. The tool available for moving properties from obsolete nets to new nets is unusable. The tool should be made smart enough to recognize the changed name and carry the constraints to the new name.*

*When a design has many blocks the tabs are not readable.*

*I know there are more changes coming. Our Engineer's fear is that with so many constraints, a few can be easily lost. They need a quick simple check to verify their designs, maybe something similar to the pxl.chg file that indicates constraints adds and deletions.*

*We have also been using Design Compare to track differences between the schematic and layout, but the information presented is not easily understood.*

### **Conclusion**

*The move to 15.7 and the 15.7 Constraint Manager has been beneficial. The process has been simplified. The tools run faster. The tools are stable.*

*The following steps are the basic steps used to move a design to 15.7. Additional steps are required to verify that the designs contain the same constraints.*

- 1. File > Save Hierarchy*
- 2. Tools > Constraints > Synchronize*



## **Reference Information Follows:**

### *Moving a constrained design from release 15.2 to release 15.5*

#### *Steps:*

1. *Using the existing packaged files from the old release (15.2), Import logic into an empty board.  
Problems encountered here require knowledge of the PCB Editor.*
2. *Open Tools > Reports  
Cadence supplied a special report format that reduced the number of properties reported, eliminating a large number of blank columns (net\_prop\_report\_tektronix.txt). To reduce the report to fewer specific properties, we created additional special report formats (see the following "short" reports).  
  
The customized reports are not part of the basic tool set, so they must be loaded each time they are used.*
3. *After loading the reports, select the report from the list and write the report.*
4. *In the 15.5 release File > Save Hierarchy -this will indicate if there are any errors before you start working on the design.*
5. *Tools > Constraints > Edit  
check for errors reading constraints*
6. *Package the design – Export Logic*
7. *Open an Empty board*
8. *Run a property report*
9. *Use VIM Diff to compare the two reports. VIM Diff highlights differences.  
In complex hierarchical designs, there are differences in the group names automatically created for the relative\_propagation\_delay property. We were specifically looking for missing properties, typically net\_physical\_type and net\_spacing\_type properties.*

## *Moving a constrained design from release 15.2 or release 15.5 to release 15.7*

### *Steps:*

1. *Using the existing packaged files from the old release (15.2 or 15.5), Import logic into an empty board. Problems encountered here require knowledge of the PCB Editor.*

2. *Open Tools > Reports*  
*Cadence supplied a special report format that reduced the number of properties reported, eliminating a large number of blank columns (net\_prop\_report\_tektronix.txt). To reduce the report to fewer specific properties, we created additional special report formats (see the following "short" reports).*

*The customized reports are not part of the basic tool set, so they must be loaded each time they are used.*

3. *After loading the reports, select the report from the list and write the report.*

4. *In the 15.7 release File > Save Hierarchy -this will indicate if there are any errors before you start working on the design.*

5. *Tools > Constraints > Synchronize -this changes constraint properties on the schematic to placeholder properties.*

6. *Package the design – Export Logic*

7. *Open an Empty board*

8. *Run a property report*

9. *Use VIM Diff to compare the two reports. VIM Diff highlights differences.*

*In complex hierarchical designs, there are differences in the group names automatically created for the relative\_propagation\_delay property. We were specifically looking for missing properties, typically net\_physical\_type and net\_spacing\_type properties.*

## ***Moving a design to 15.7, Synchronization***

*The following steps are the basic steps used to move a design to 15.7. Additional steps are required to verify that the designs contain the same constraints.*

- 1. File > Save Hierarchy -this will indicate if there are any errors before you start working on the design.*
- 2. Tools > Constraints > Synchronize - changes constraint properties on the schematic to placeholder properties*

*After you synchronize the design, the Constraint Manager is the master for constraints. Additions and modifications of constraints are then done through the Constraint Manager.*

*Example of a schematic property before synchronization*  
`net_physical_type=100_OHM`

*Example of a schematic property after synchronization*  
`$net_physical_type=?`

*Schematic modes are now important. The mode "in-hierarchy" means you are seeing only the information on the schematic sheet that is currently displayed. The placeholder values will appear a "?". Use Tools > Expand to display the Constraint Manager value. In the expanded mode, you are seeing information from all sheets in the design, and information from the Constraint Manager. You will see the value 100\_OHM.*

*Plot with the design in the expanded mode to have the Constraint Manager properties visible on the plotted sheets.*

*The differential pair properties are still recognized as properties on the schematic, and in the Constraint Manager. This creates some problems when you delete or modify the value of a differential\_pair property.*

## **Validation Steps**

***In the old release (15.2 or 15.5) package the design.***

*Open PCB Editor and import the schematic packaged files*

*Select Tools > Reports*

*In the Reports window, select the New/Edit button*

*In the Extract UI window, select the Load button*

*In the Open window, use the pull down to browse to your Reports directory*

*Select net\_prop\_report or other appropriate template file*

*Select the Open button*

*In the Extract UI window, select the Close button*

*In the Reports window, locate the net\_prop\_report in the Available Reports pane. Double click to select.*

*Select the Write Reports check box.*

*Select the Output File text box, and type the save name for your report.*

*Select the Report button.*

*Select the Close button.*

*The report of the constraints contained in the older design has been generated, and automatically saved in your Reports directory.*

***In the 15.7 release.***

*Save Hierarchy.*

*Synchronize the constraint properties.*

*Select Tools > Constraints > Synchronize*

*Package the design.*

*Open PCB Editor and import the 15.7 schematic packaged files*

*Select Tools > Reports*

*In the Reports window, select the New/Edit button*

*In the Extract UI window, select the Load button*

*In the Open window, use the pull down to browse to your Reports directory*

*Select net\_prop\_report or other appropriate template file*

*Select the Open button*

*In the Extract UI window, select the Close button*

*In the Reports window, locate the net\_prop\_report in the Available Reports pane. Double click to select.*

*Select the Write Reports check box.*

*Select the Output File text box, and type the save name for your report.*

*Select the Report button.*

*Select the Close button.*

*The report of the constraints contained in the 15.7 design has been generated, and automatically saved in your Reports directory.*

*Open the two reports in VIM Diff and look for differences and missing properties.*

## *Net\_prop\_report\_tektronix.txt*

```
# This is an extract command
file
# generated by the Extract UI.
#
NET
NET_NAME != ''
NET_NAME_SORT
NET_NAME
NET_BUS_NAME
NET_SPACING_TYPE
NET_PHYSICAL_TYPE
NET_ELECTRICAL_CONSTRAINT_SET
NET_ECL
NET_DRIVER_TERM_VAL
NET_LOAD_TERM_VAL
NET_FIXED
NET_RATSNEST_SCHEDULE
NET_NO_RAT
NET_NO_GLOSS
NET_NO_PIN_ESCAPE
NET_NO_RIPUP
NET_NO_ROUTE
NET_NO_TEST
NET_PROBE_NUMBER
NET_ROUTE_PRIORITY
NET_ROUTE_TO_SHAPE
NET_SAME_NET
NET_MIN_BVIA_GAP
NET_MIN_BVIA_STAGGER
NET_MAX_BVIA_STAGGER
NET_MIN_BOND_LENGTH
NET_MAX_BOND_LENGTH
NET_MIN_LINE_WIDTH
NET_MIN_NECK_WIDTH
NET_DIFFERENTIAL_PAIR
NET_DIFFP_COUPLED_MINUS
NET_DIFFP_COUPLED_PLUS
NET_DIFFP_GATHER_CONTROL
NET_DIFFP_MIN_SPACE
NET_DIFFP_NECK_GAP
NET_DIFFP_PHASE_CONTROL
NET_DIFFP_PHASE_TOL
NET_DIFFP_PRIMARY_GAP
NET_DIFFP_UNCOUPLED_LENGTH
NET_TS_ALLOWED
NET_STUB_LENGTH
NET_IMPEDANCE_RULE
NET_PROPAGATION_DELAY
NET_RELATIVE_PROPAGATION_DELAY
NET_MAX_PARALLEL
NET_MAX_XTALK
NET_MAX_PEAK_XTALK
NET_MAX_INTER_XTALK
NET_MAX_INTRA_XTALK
```

```
NET_MAX_EXPOSED_LENGTH
NET_TOTAL_ETCH_LENGTH
NET_MIN_NOISE_MARGIN
NET_MAX_OVERSHOOT
NET_MIN_FIRST_SWITCH
NET_MAX_FINAL_SETTLE
NET_MIN_HOLD
NET_MIN_SETUP
NET_MAX_SSN
NET_MAX_SLEW_RATE
NET_PULSE_PARAM
NET_FIRST_INCIDENT
NET_EDGE_SENS
NET_CLK_2OUT_MAX
NET_CLK_2OUT_MIN
NET_CLK_SKEW_MAX
NET_CLK_SKEW_MIN
NET_CLOCK_NET
NET_TIMING_DELAY_OVERRIDE
NET_ASSIGN_TOPOLOGY
NET_TOPOLOGY_TEMPLATE
NET_TOPOLOGY_TEMPLATE_MAPPING_MODE
NET_TOPOLOGY_TEMPLATE_REVISION
NET_VOLTAGE
NET_SUBNET_NAME
NET_TESTER_GUARDBAND
NET_SHORT
NET_SHORTING_SCHEME
NET_WEIGHT
LAYERSET_GROUP
DIFF_PAIR_GRP_NAME
MATCH_GROUP_GRP_NAME
XNET_GRP_NAME
END
```

### *Short\_net\_prop\_report\_tek.txt*

```
# This is an extract command
file
# generated by the Extract UI.
#
NET
NET_NAME != ''
NET_NAME_SORT
NET_NAME
NET_BUS_NAME
NET_SPACING_TYPE
NET_PHYSICAL_TYPE
NET_ELECTRICAL_CONSTRAINT_SET
NET_DIFFERENTIAL_PAIR
DIFF_PAIR_GRP_NAME
NET_PROPAGATION_DELAY
NET_RELATIVE_PROPAGATION_DELAY
MATCH_GROUP_GRP_NAME
NET_VOLTAGE
XNET_GRP_NAME
NET_RATSNEST_SCHEDULE
NET_ROUTE_PRIORITY
END
```

### *Short\_rel\_prop\_report\_tek.txt*

```
# This is an extract command
file
# generated by the Extract UI.
#
NET
NET_NAME != ''
NET_NAME_SORT
NET_NAME
NET_BUS_NAME
NET_RELATIVE_PROPAGATION_DELAY
MATCH_GROUP_GRP_NAME
XNET_GRP_NAME
END
```

### *Short\_physical\_net\_prop\_report\_tek.txt*

```
# This is an extract command
file
# generated by the Extract UI.
#
NET
NET_NAME != ''
NET_NAME_SORT
NET_NAME
NET_BUS_NAME
NET_SPACING_TYPE
NET_PHYSICAL_TYPE
NET_ELECTRICAL_CONSTRAINT_SET
NET_VOLTAGE
XNET_GRP_NAME
END
```

## ***What are Schematic States?***

*A schematic may be in one of three different states, or modes, [in hierarchy], [expanded], or [occurrence edit]. The default state of a schematic is [in hierarchy].*

### **[in hierarchy]**

**: Design Entry HDL - [SPEEDWAY\_MAIN.SCH.1.1 [in hierarchy]]**

Block Group Display AMS Simulator Tools Window Help

- Limits searching to the current active display
- You may display and search one page in the design.

### **[expanded]**

**: Design Entry HDL - [SPEEDWAY\_MAIN.SCH.1.1 [expanded]]**

Block Group Display AMS Simulator Tools Window Help

- Compiles information from all sheets in the design
- Temporary files allow searching through all pages of the design.
- Some processes require expansion of the design.
- Constraint Manager and all global search commands require design expansion.

### **[occurrence edit]**

**: Design Entry HDL - [SPEEDWAY\_MAIN.SCH.1.1 [occurrence edit]]**

t Block Group Display AMS Simulator Tools Window Help

- The occurrence state stores information that cannot be stored on the schematic page.
- When a property is attached to a bus, ADDR<15..0>, the property is inherited by each member of the bus. The schematic displays information at the bus bit level, not at the highest bus signal level.
- Use occurrence edit to change the property on one bus bit. The occurrence change will be stored in the OPF. OPF has the primary value, or winning value.
- You may view the OPF values with the ATTRIBUTE command when the design is in the expanded mode.
- In a complex hierarchical drawing, when the same block is used multiple times, each occurrence of the drawing will have unique signal names, and unique reference designators.
- In the occurrence edit mode, the unique occurrence values will display when you descend into the schematic pages of a block. You may make additional property modifications in the occurrence edit mode.



## ***What are Schematic Styles?***

*A schematic may be created using one of three different styles: Flat, Simple Hierarchy, or Complex Hierarchy. The default state of a schematic is flat. A general understanding of the capabilities and limitations of schematic styles is necessary.*

***Flat Schematics***, the simplest schematic style.



### **FEATURES OF A FLAT DESIGN**

- A flat design uses one name for all of the schematic sheets.
- The only difference in the names of the sheets will be the sheet, or page number.
- All of the page files reside in the same directory.
- Signals are connected by name, no special name syntax or ports are required
- Every symbol instance exists on the schematic pages
- All reference designators and pins may be annotated on the schematic
- Each schematic page is unique.
- Occurrence edit will always affect bus signals.
- If the OPF is deleted, the schematics still contain all of the information required to recreate the information stored in the OPF.  
(If you have not edited properties in the occurrence edit mode.)
- When Constraint Manager is used, it will read constraint properties, of correct syntax, from the schematic.

When constraints are created in the Constraint Manager, the property information is stored in the constraint directory *<drawing>.dcf*. The Constraint value may be seen in the ATTRIBUTE form when the schematics are expanded. To annotate the property on the schematic, you must have a placeholder property on the schematic net.

# What is hierarchy?

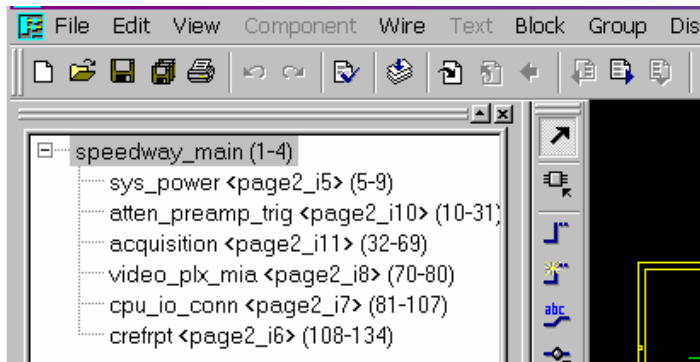
*Simple hierarchy and complex hierarchy*

## FEATURES OF HIERARCHICAL DESIGNS

- A hierarchical design usually has a block diagram at the top level, with one or more schematic sheets under each block.
- A block is similar to a library symbol, but the information related to pin usage is provided by schematics instead of through a chips file. **Block names may not contain spaces.**
- A block and supporting schematic sheet will have the same name, and be located in the same directory.
- Individual blocks will have different names, and the sheets will be saved in separate directories.

## *Simple Hierarchy*

Simple hierarchy is a block symbol and underlying schematics, when the block is used just one time in the design. A simple hierarchical design and a flat schematic design are very similar. Both types of designs have a single instance of each schematic symbol. Backannotation will place reference designators and pin numbers on each symbol.



- A simple hierarchy uses each block only once
- Every symbol is represented on the schematics

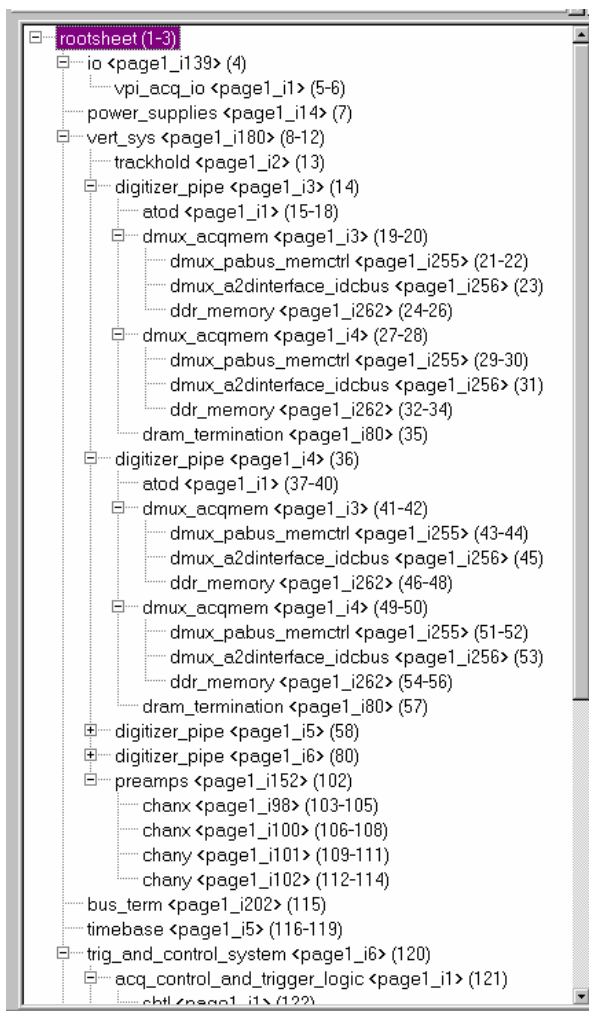
## *Complex Hierarchy, the most difficult style of schematics*

A complex hierarchical design uses one or more blocks more than one time. Whenever the same block is reused within a design, the design is a complex hierarchy. The same set of schematic pages is referenced each time the block is used. When the design is packaged, and the first instance of a block is encountered, the schematics under the block are packaged. Reference designators are assigned in sequence. When the

packager comes across another instance of the same block, the schematics are again packaged and reference designators are assigned in sequence. Now, each symbol on the block level schematic has two different reference designators. The reference designators are stored in the Occurrence Property File. One set of reference designators for each block occurrence.

To view or plot each occurrence of the reference designators, the design must be placed in the Occurrence Edit Mode. There will be no similarity of reference designators, to easily identify the same part, used in different instances of the same block.

To maintain some similarity in the reference designator assignments, the block may be packaged as a subdesign. This creates a reference designator "root" that is made unique by appending a suffix.



- Any time the same block is used more than one time in a schematic design, the design is a complex hierarchy.
- A block used multiple times always calls the same schematic page or pages.

- Each part in the design is not uniquely represented on the schematics.
- Reference designators unique to each instance of the block are stored in the OPF. The schematic can only store one value for each property.
- With multiple use of the same block, all unique property information for each instance of the block is stored in the OPF. Unique information for each page instance is viewable in Occurrence Edit Mode.
- Property passing, macros, may be used in Complex Hierarchical designs, but it is very limited, and totally disabled if you use the Constraint Manager.
- Packaging a complex hierarchy is a multi-step process.

#### General Information for hierarchical designs

- Local signals are recognized only within individual blocks of the hierarchy.
- Interface signal names must match block pin names
- The PINNAMES command creates a symbol with matching signal names.
- Interface signals must be identified by a port symbol, or a \I suffix on the signal name.
  - INPORT
  - OUTPORT
  - IOPORT
  - or FLAG
- Global signals are identified by the HDL\_POWER property attached to the power symbols, or by a \G suffix attached to the signal name.
- Global signals are recognized by name throughout the entire design, no port symbols are required.
- The same signal name may not be used with more than one signal scope.

## Occurrence Editing

The occurrence editor stores information that is not stored as part of the schematic page. The value of a property edited in occurrence edit mode is stored in the OPF, not on the schematic page. If you view the schematic page in hierarchy mode, you will see the unedited value of the property. If you view the schematic page in the expanded mode, you will constraint values displayed where you have placeholders. The ATTRIBUTE command will display the schematic value of the property and the net value of the property. When you view, or plot, the schematic in the occurrence edit mode, you will see the value of the property as changed in the occurrence edit mode.






- Some occurrence properties are automatically created and stored in the OPF.
- In occurrence edit mode, you may create or modify information stored in the OPF.
- In a flat design, occurrence editing may lead to problems with “phantom” property values. The value stored in the OPF takes precedence over the value stored on the schematic page.
- Occurrence editing may be used with complex hierarchical designs to manually create unique property values for different instances of a block that has been used multiple times.  
NOTE: If there are several changes, this can be a very repetitive manual process.
- If you modify property values in occurrence edit mode, deletion of the OPF will cause you to lose all of your modifications.
- File contention is not controlled for occurrence editing.
- The OPF is a design file. If a page is copied, the OPF information is not copied to another design.

## Constraint Manager

The Constraint Manager is a spreadsheet tool used to create and modify design constraint properties. This replaces the older practice of placing constraint properties directly on wires in the schematic pages. Constraints typically used at Tektronix are: propagation delay, relative propagation delay, differential pair, net physical type, and net spacing type properties.

The constraint information is stored in a .dcf file located under the constraints directory. The root design contains the master constraints directory, and each subdesign contains the constraints directory for that subdesign. The Constraint Manager now reads information from lower level constraint directories. When the same subdesign is used multiple times, the same subdesign constraint information is read each time. Suffix numbers are automatically added to keep group names, reference designators used in pin pairs, and differential pair names unique. It is confusing that the suffixes used have no relationship to any suffixes you have assigned.

### CONSTRAINTS DIRECTORY

 deleted.opf	1 KB	OPF File
 last_update.dcf	1,009 KB	DCF File
 speedway_main.dcf	1,715 KB	DCF File
 speedway_main.dcf,1	1,009 KB	DCF,1 File
 speedway_main.dcf,p	1 KB	DCF,P File

- Constraint properties are created in the Constraint Manager spreadsheet.
- Tools > Constraints > Synchronize reads properties from the schematic pages, if the syntax is correct. The message “failing to push constraints” indicates a problem with the syntax or content of a schematic property.
- Constraint properties are stored in the constraints directory, project.dcf file.
- Constraint properties may be seen in the ATTRIBUTE form when the schematic has been expanded.
- Constraints may be annotated on the schematic in the expanded mode, if there is a placeholder property.

- If a net name is changed, the constraints associated with the old net name will be lost.
- Obsolete nets are not automatically flushed you must Audit Obsolete Objects, and identify the obsolete objects to be deleted.
- The schematic Constraint Manager does not recognize power pins identified in the chips.prt file, or the power\_group property. Only visible signal pins may be used in pin pairs.
- Deletion of the constraints directory will eliminate all constraints except those that exist as properties on schematic nets.
- File contention is not controlled for the Constraint Manager.
- Constraint files are not copied with individual pages of the design.