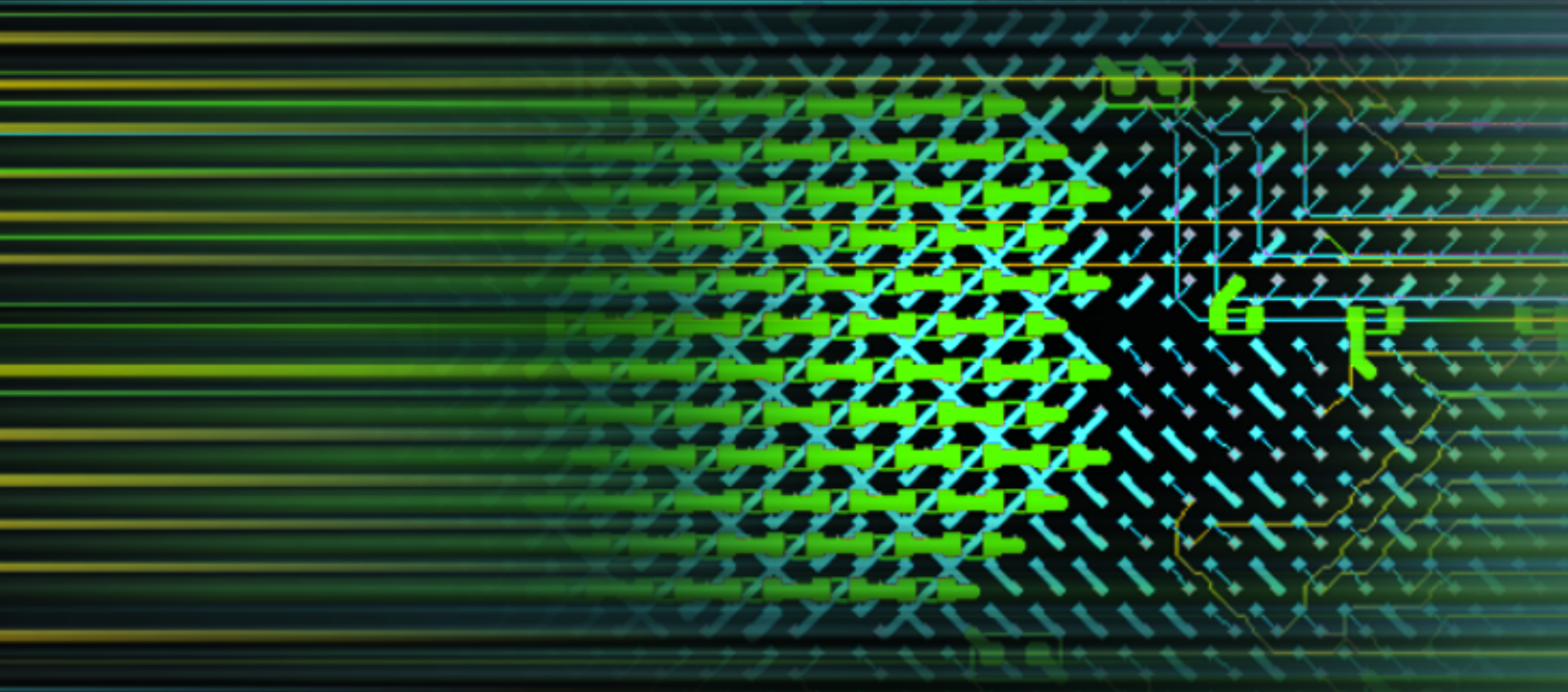
PLATFORM OVERVIEW

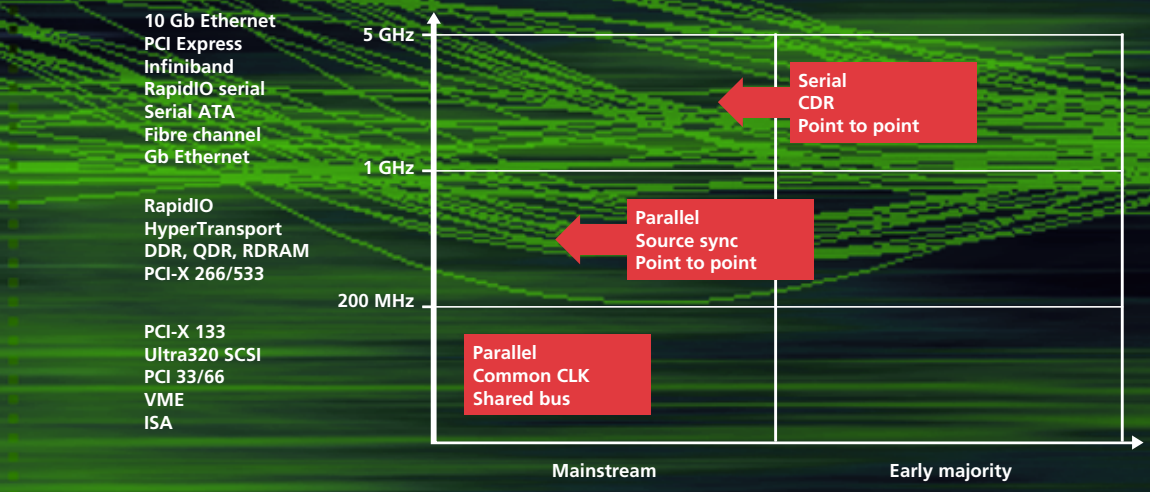
CADENCE ALLEGRO SYSTEM INTERCONNECT DESIGN PLATFORM

ON TARGET, ON TIME
SYSTEM INTERCONNECT

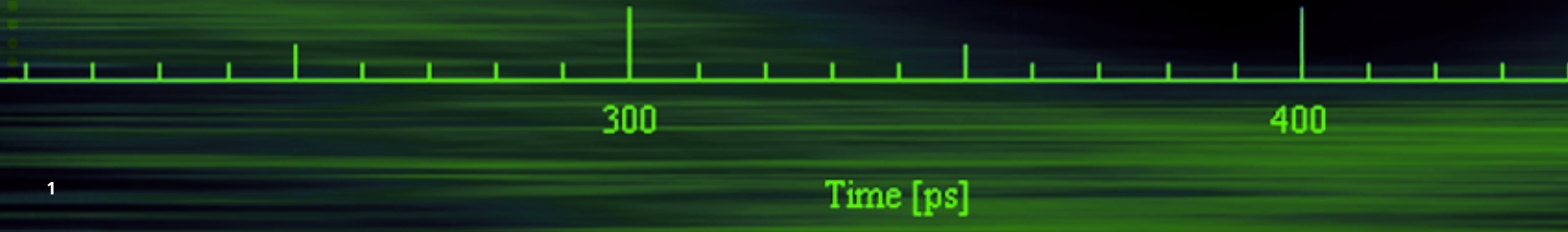


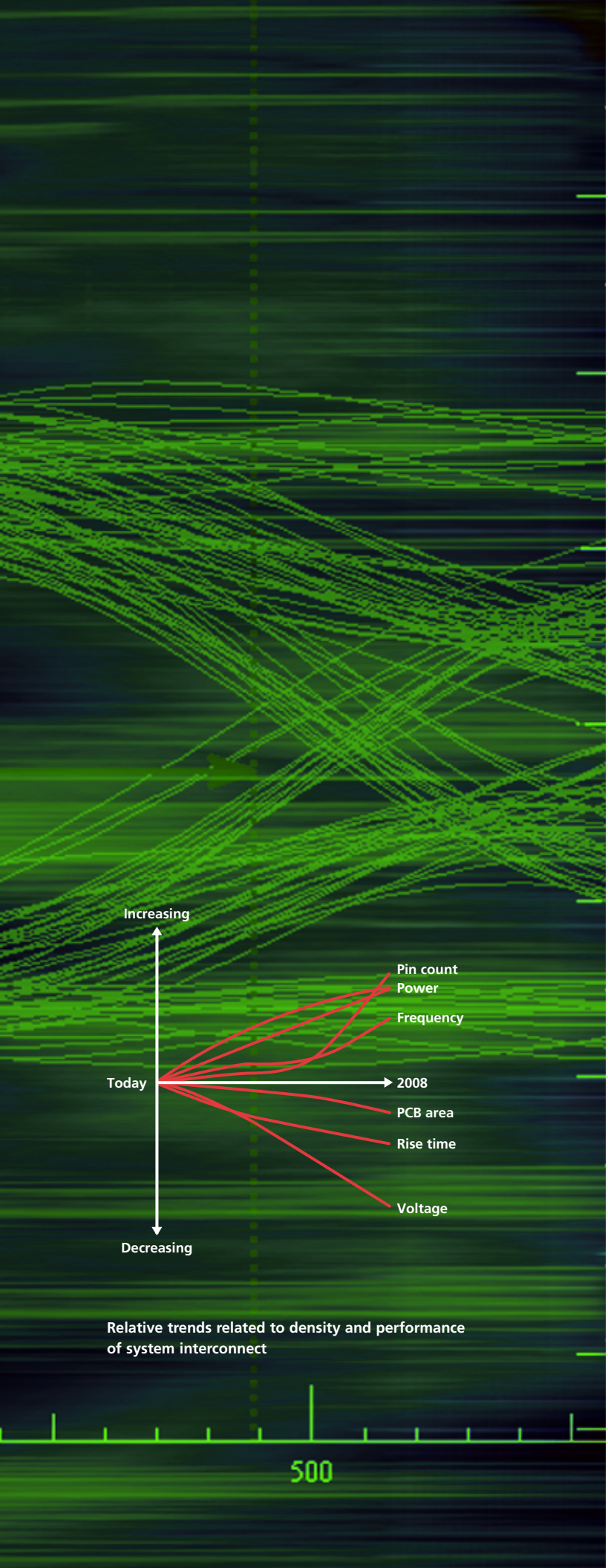
CADENCE ALLEGRO SYSTEM INTERCONNECT DESIGN PLATFORM

ON TARGET, ON TIME
SYSTEM INTERCONNECT



Data rates are moving into the multigigahertz range, requiring new approaches to the modeling and analysis of system interconnects to avoid signal integrity and power delivery issues





Relative trends related to density and performance of system interconnect

THE FAST TRACK TO WORKING HIGH-SPEED SYSTEM INTERCONNECT

IC and systems design teams face unprecedented challenges in designing today's high-speed systems. Chip I/Os and package pin counts are rapidly increasing. Gigahertz-speed data rates translate into blisteringly fast PCBs and systems. At the same time, the average PCB size is decreasing and power delivery requirements are heating up as chip transistor counts explode. Solving these complex problems requires a new generation of technologies and methodologies. The Cadence Allegro® system interconnect design platform enables collaborative design of the interconnect from I/O buffer to I/O buffer—across ICs, packages, and boards. This integrated approach enables electronics companies to achieve a competitive advantage with faster time to market, reduced costs, and improved system performance.

SYSTEM INTERCONNECT CO-DESIGN METHODOLOGY

Created to help IC and systems companies achieve their cost and time-to-market goals, the Allegro technology platform and associated co-design methodology:

- Eliminates design iterations and reduces design cycles between IC, package, and PCB design domains
- Reduces the risk of IC mask re-spins
- Decreases the cost of IC packages and eliminates package re-spins
- Accelerates the time required to successfully design-in complex ICs
- Limits the number of PCB prototypes needed to get boards ready for production

THE SYSTEM INTERCONNECT

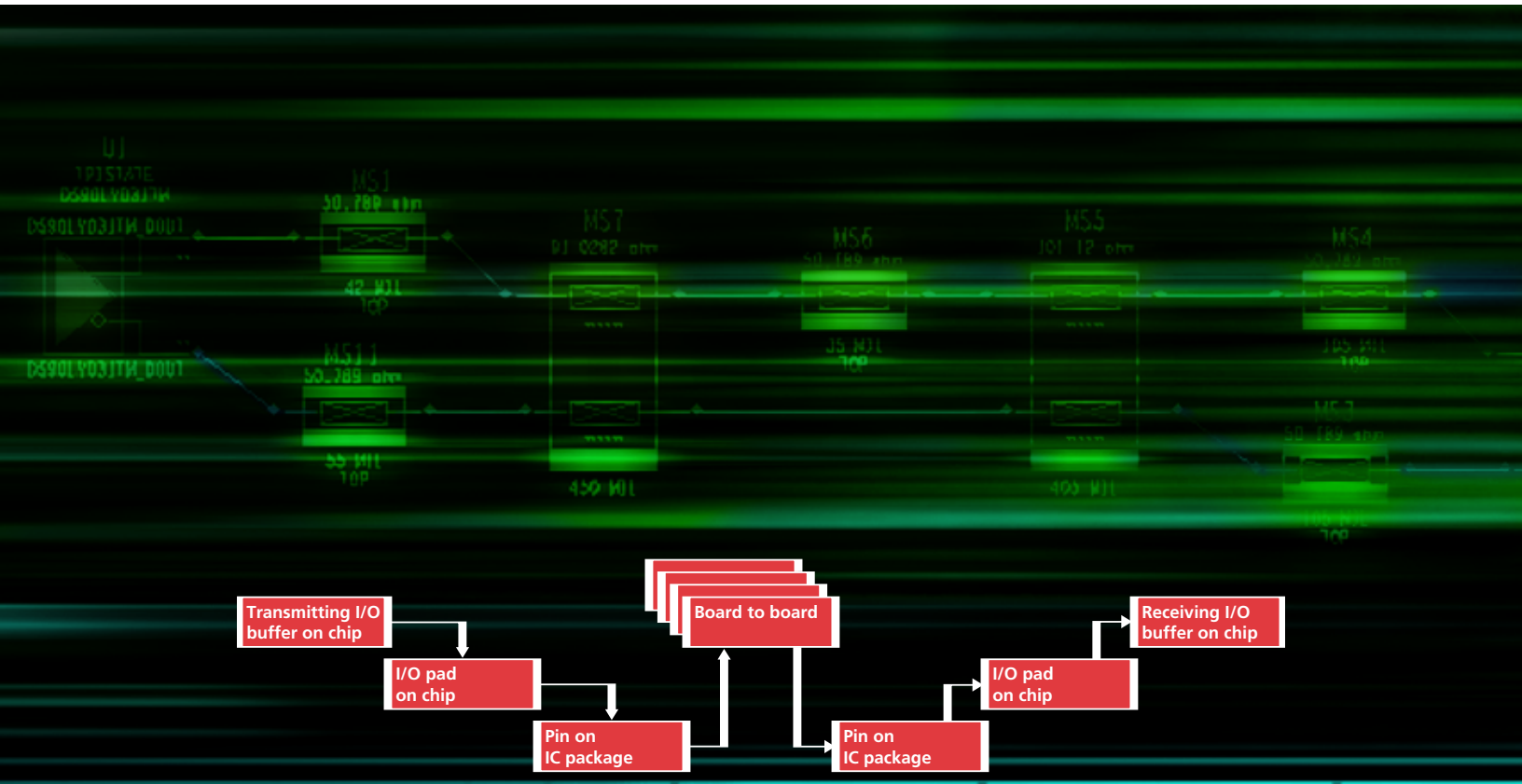
The term "system interconnect" refers to the logical, physical, and electrical connection of a signal, its associated return path, and the power delivery system. The system interconnect travels from an IC I/O buffer through a bump and package substrate to a package pin; across a PCB or multiple PCBs and connectors; back to a package pin; and through a package substrate and bump to another IC I/O buffer.

Looking at how a system interconnect is designed today illustrates the need for a new approach. It is a fragmented, lengthy, and costly process that involves at least four players: an I/O buffer designer, IC designer, IC package designer, and a PCB designer. Working in dissimilar domains, they implement their designs using different design tools — each tailored for the materials, properties, and feature sizes of the respective fabrics in these three system domains.

THE NEW METHODOLOGY

The Cadence co-design methodology links these fragmented design processes through a common interconnect database and a unique process for creating an abstract, or virtual system interconnect (VSIC) model, which enables complete modeling and analysis of the interconnect across the IC, its package, and the PCB.

The VSIC model is essentially a topology that describes the entire system interconnect. It describes the physical, logical, and electrical properties of the interconnect, including the power delivery system. It also captures and validates



The system interconnect is designed across the domains of IC, IC package, and PCB

certain design assumptions and specifications, and it can mature throughout the design process.

The VSIC model is created by a systems integrator and then distributed to design team members. The diagram below shows how each designer can test the VSIC model and feed back information to the systems integrator on the viability of the design. Any necessary trade-offs can then be made and the VSIC model updated so that all team members have access to the same data. In this manner, designers discover and address problems early in the design process, dramatically reducing design iterations and helping to ensure first-time design success.

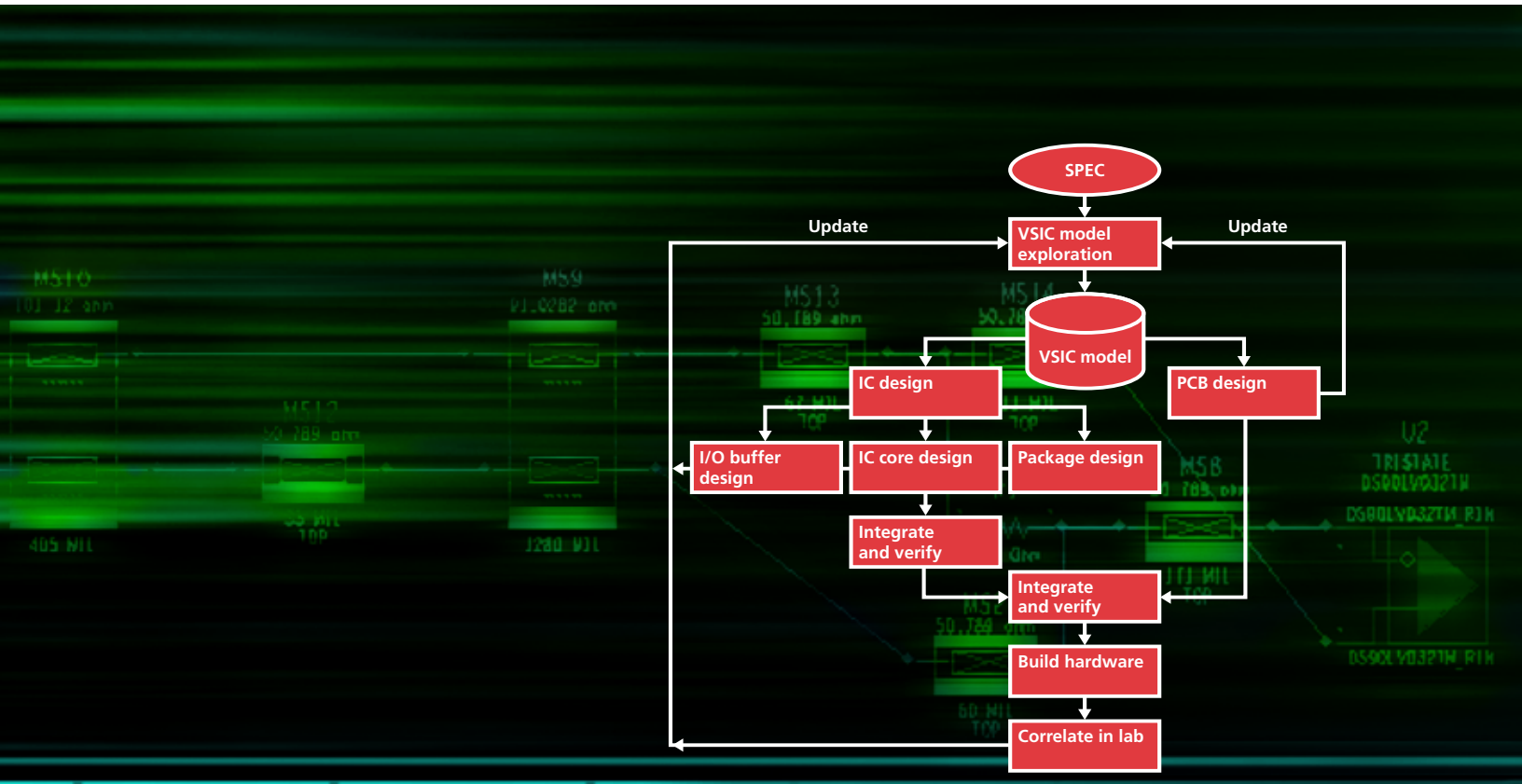
ENABLING COLLABORATION ACROSS DOMAINS

The Cadence Allegro co-design methodology provides for collaboration at all key stages of interconnect design, for example:

- The I/O buffer designer can create buffer models in the context of the VSIC model. Then, as the package and PCB are designed and the model updated with actual design data, the I/O designer can validate the buffer models against actual package and board implementations
- The IC designer and IC package designer can collaborate via an automated process to ensure the bump pattern the IC designer is creating can actually be implemented on the package
- The PCB designer can work with the IC package designer to optimize package-pin design for routing ease, avoiding costly redesign
- The IC producer can provide the PCB systems designer with a silicon design-in kit—an electronic blueprint for the implementation of silicon in a system—cutting the time required to design-in complex semiconductor devices
- Several PCB designers can collaborate on a PCB layout through partitioning technology, enabling major reductions in layout design time

NEW METHODOLOGY REQUIRES NEW TECHNOLOGY

The new co-design methodology requires a new technology platform—one that enables collaboration from the beginning to the end of the design cycle. The methodology must address both the traditional logical and physical design issues, as well as the increasingly complex challenges of timing, power, and signal integrity.



A VSIC model drives a true co-design methodology

THE ALLEGRO SYSTEM INTERCONNECT DESIGN PLATFORM

The Cadence Allegro platform is an integrated solution created to deliver the productivity and economic benefits of the co-design methodology. Built on a common interconnect database and a shared constraint management system, it allows collaboration across design domains.

The Allegro interconnect database enables the creation of a VSIC model, eliminating the need for data translations, reducing errors, and ensuring data integrity. The intelligent, hierarchical Allegro constraint management system captures design intent in the form of constraints and manages them throughout the entire design process, making certain that original design intent is realized.

ACCURATE MODELS INTEGRAL TO INTERCONNECT DESIGN SUCCESS

In order to create accurate models when faced with shrinking design cycles, the Allegro Package and PCB SI tools facilitate the production of both I/O and interconnect models. For I/O models, Allegro simulates with both transistor-level (SPICE) and behavioral models (both IBIS and advanced Allegro DML formats). Importantly, Allegro SI enables IC and systems companies to quickly create behavioral models from SPICE models. These models are Allegro SI-ready, eliminating iterations and saving weeks of work. Interconnect models can be created in either a virtual form during design exploration or from automatic extraction from actual physical designs.

CONSISTENT ADVANCED ANALYSIS

Allegro SI effectively deals with the problems of timing, power, and signal quality across the design chain. Through this robust engine, each designer can perform analysis of their piece of the interconnect to ensure consistent results. Analysis capabilities take into account loss, crosstalk, reflections, and simultaneous switching noise while sweeping a multitude of variables. Reporting capabilities include waveforms and eye diagrams. All of these features add up to improved system performance and reduced prototypes.

SILICON DESIGN-IN KITS SPEED PCB DESIGN

Currently, implementing new silicon devices in a PCB system can be a time-consuming, difficult process. Allegro technology resolves these issues by providing IC companies with the ability to create silicon design-in kits. Electronic blueprints for the implementation of silicon devices in a system, design-in kits can be delivered when — or even before — new silicon is available.

Designed to be plug-and-play compatible, a good design-in kit can drive the entire design process from simulation and exploration to floorplanning, routing, and verification — rapidly accelerating the time needed to simulate and design-in complex devices. Both teams reap the benefits: IC producers profit from increased time to volume for new devices while systems companies get products to market much faster.

ACCELERATED LOGIC AND PHYSICAL DESIGN

Embedded in Allegro Package Designer — the robust IC packaging design environment—is first-of-its-kind technology that allows an IC designer to collaborate with a package designer during the IC bump pattern design phase. Collaboration at this stage enables optimization of the IC bump pattern; reduction in the package cost; elimination of IC re-distribution layer mask and package re-spins; and, possible re-use of a standard package.

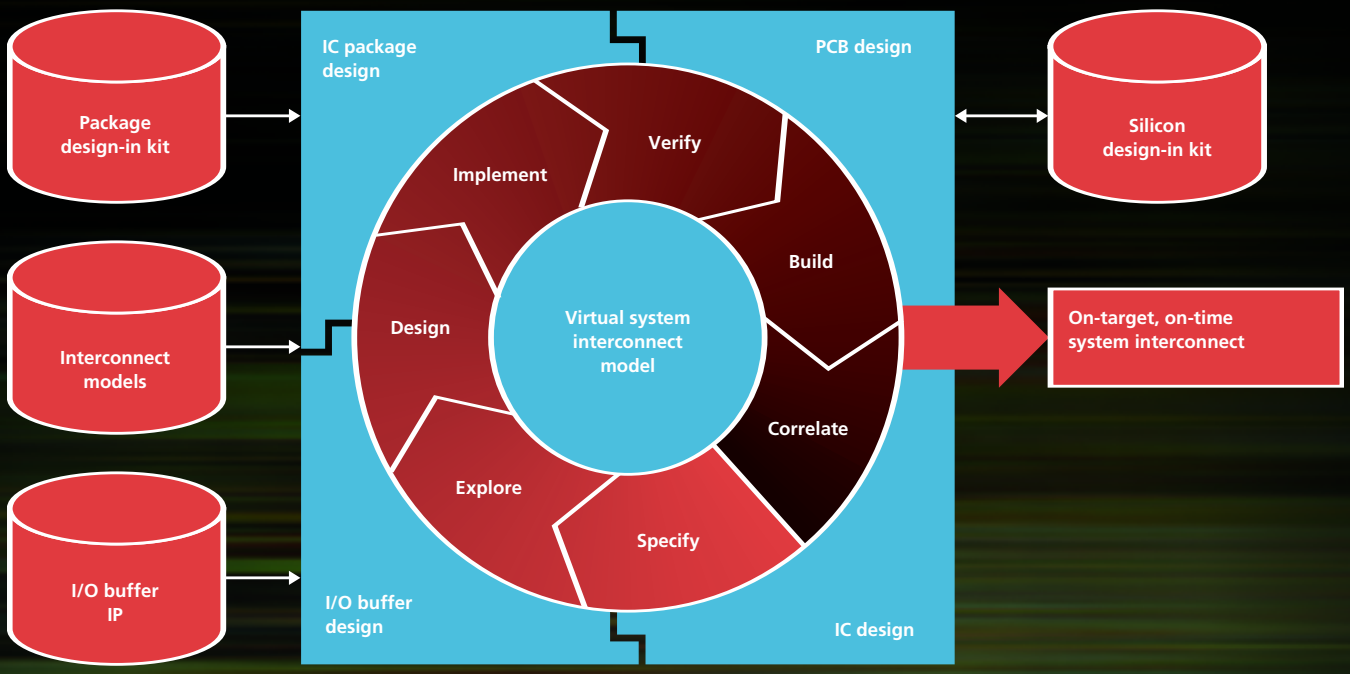
To facilitate logic design in the PCB domain, Allegro Design Editor provides the industry's first multi-style design creation environment. In addition to the traditional schematic-based design approach, it allows designs to be captured using HDL (Verilog) or customizable spreadsheets. Allegro design entry and the physical design of the system interconnect is fully integrated with the constraint management system. The physical design of the system interconnect is also integrated with the constraint management system. Powerful, flexible routing technology makes easy work of routing the highly constrained differential pairs and multilayer boards prevalent in high-speed design.

POST LAYOUT VERIFICATION

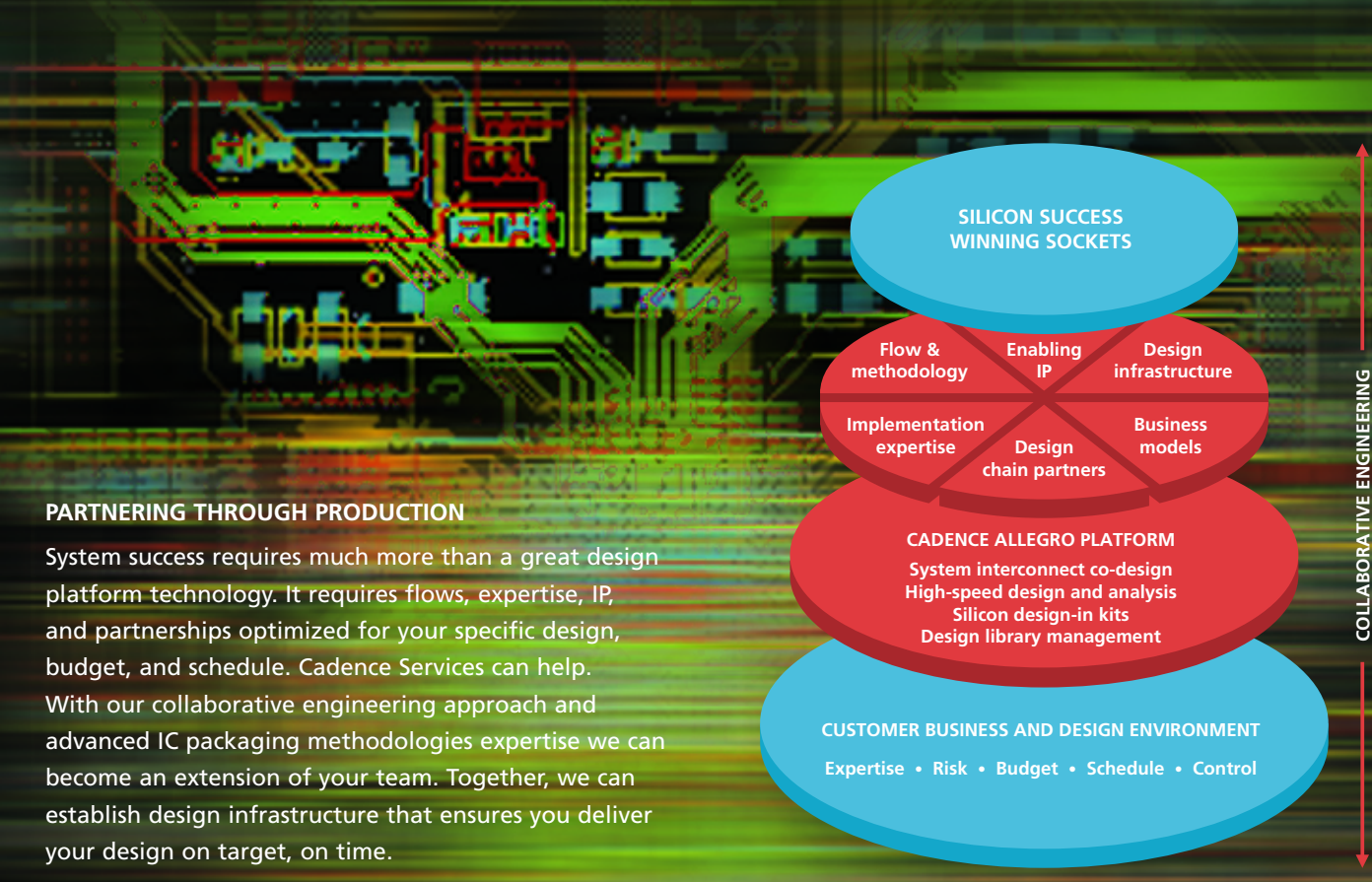
Verification is performed after the system interconnect has been implemented and before actual hardware is built. To ensure consistency, Allegro methodology promotes the use of the same models, analysis, and simulation engines that were used earlier in the flow. Extraction of interconnect models is automated and analysis capabilities take into account actual electrical properties resulting from the implementation of routing and real-world manufacturing tolerances.

ALLEGRO: ON TARGET, ON TIME

The Cadence Allegro system interconnect design platform provides an integrated solution for fast and accurate design of high-speed system interconnects. The Allegro 600 series products and solutions are optimized for teams tasked with designing the gigahertz-speed interconnect of IC packages and PCBs. The Allegro 200 series products and solutions are tailored for PCB designers who need a powerful constraint-driven design solution that is both functional and scalable. The Allegro co-design methodology is supported by Cadence Encounter™ and Virtuoso® platforms, enabling effective design chain collaboration. Using Cadence Allegro system interconnect design platform products, engineers can deliver systems that are on target, on time. For more information about the Allegro platform, log on to **www.cadence.com/allegro**.



An integrated technology platform supports the VSIC model, IP availability, and silicon design-in technology



PARTNERING THROUGH PRODUCTION

System success requires much more than a great design platform technology. It requires flows, expertise, IP, and partnerships optimized for your specific design, budget, and schedule. Cadence Services can help. With our collaborative engineering approach and advanced IC packaging methodologies expertise we can become an extension of your team. Together, we can establish design infrastructure that ensures you deliver your design on target, on time.

Cadence Design Systems, Inc.

Corporate Headquarters
2655 Seely Avenue
San Jose, CA 95134
800.746.6223
408.943.1234
www.cadence.com

© 2005 Cadence Design Systems, Inc. All rights reserved. Cadence, the Cadence logo, Allegro, and Virtuoso are registered trademarks, and Encounter is a trademark of Cadence Design Systems, Inc. All others are properties of their respective holders.

5256B 06/05