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Automated Parasitic Backannotation and Testbench Generation for Verification of RF-SiP Designs

Taranjit Kukal, Cadence Design Systems
Thomas Brandtner, Infineon Technologies Austria AG

Session 8.1

Agenda

- Introduction to RFSiP
- Complexity in RFSiP simulations
- Traditional RFSiP simulation flow at Infineon
- Using RFSiP for accelerating simulations at various stages of design
- Conclusions

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- **Introduction to RFSiP**
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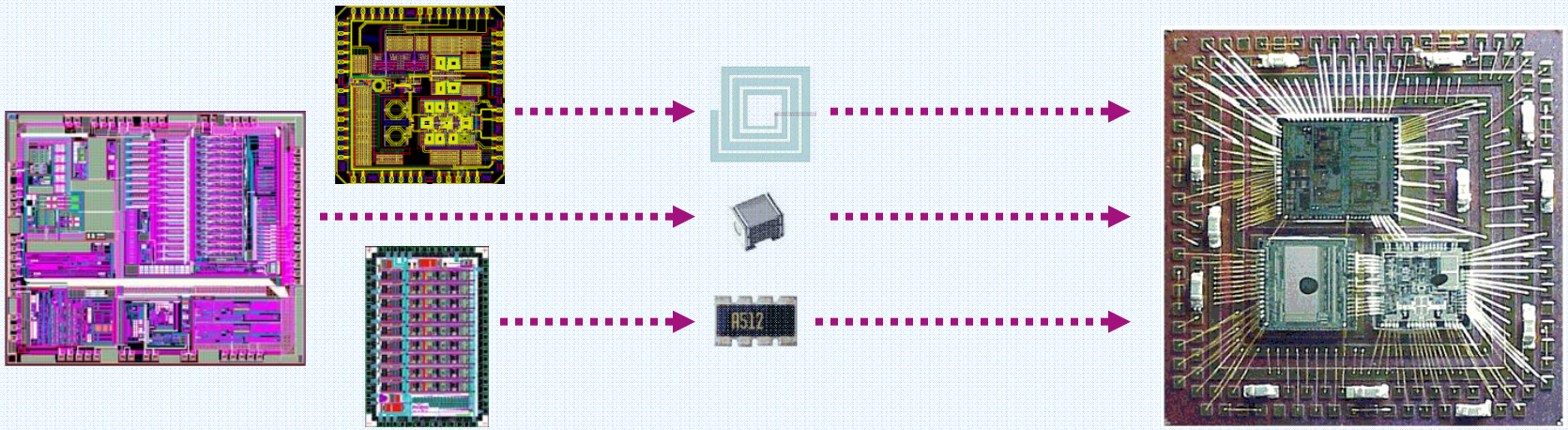
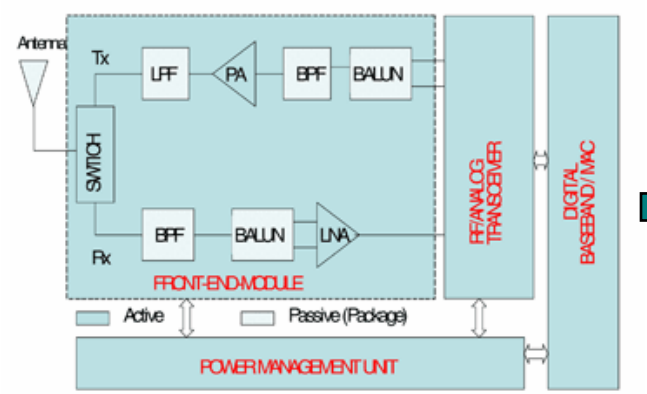
Introduction to RFSiP

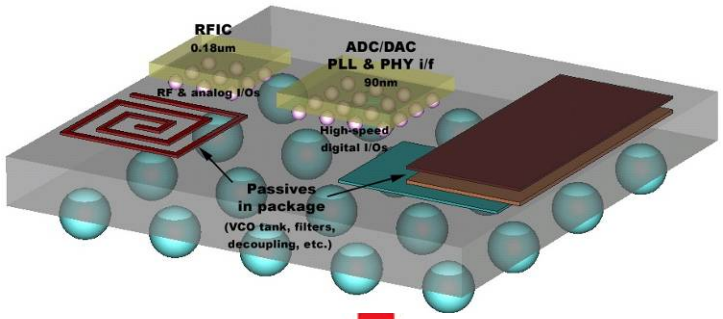
A Complete System or Sub-System in a Single Package

Integration of Multiple IC's (bare die) and Discrete Devices (SMD & Embedded) into One Package rather than One IC (SoC)

Bare Die → Discretes → Single Package







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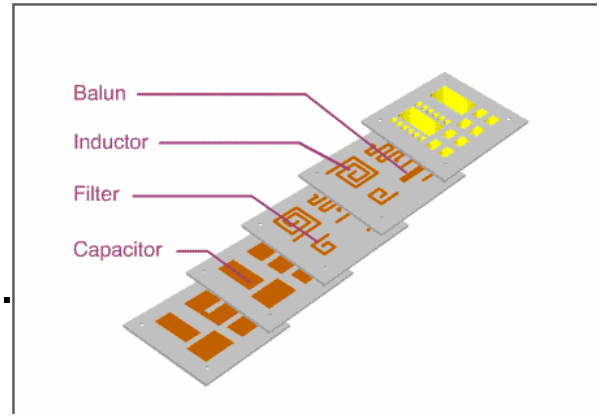
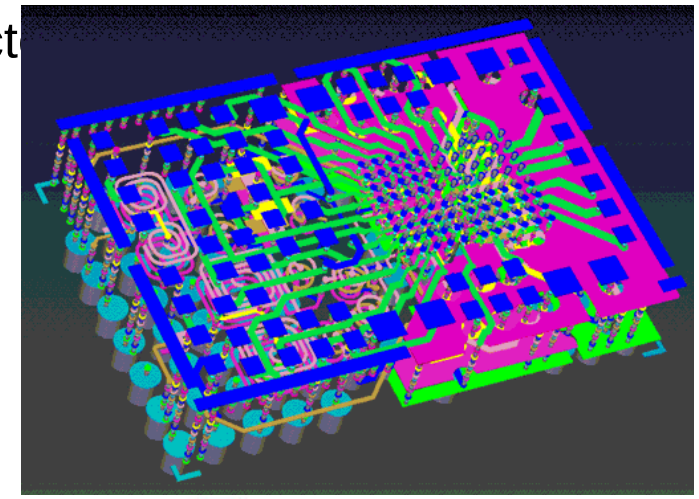
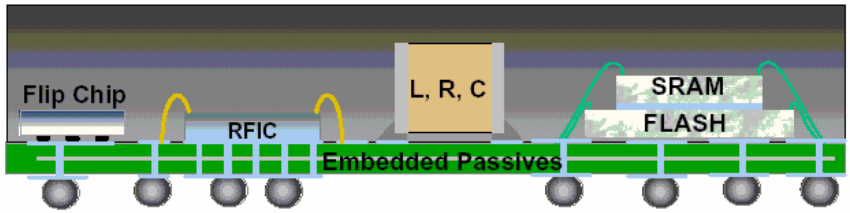
Introduction to RFSiP
- Why SiP for RF Design?

- RF IC's Typically Take 3-5 Mfr. Passes.
  - Mask Sets Cost About 3-5 Million Dollars
  - 6 Month Impact to Schedule
- LTCC (Low Temp. Co-fired Ceramic) Modules.
  - Total Cost Less Than 500K for 3-5 Passes.
  - 6 Week Impact to Schedule
- Mixed Technology Support.
  - Not Limited by Homogeneous Semiconduct GaAs, SiGe all on One Substrate
  - Flexible Design Partitioning
  - Embedded passives – metal structures







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- **Complexity in RFSiP simulations**
- Traditional RFSiP simulation flow at Infineon
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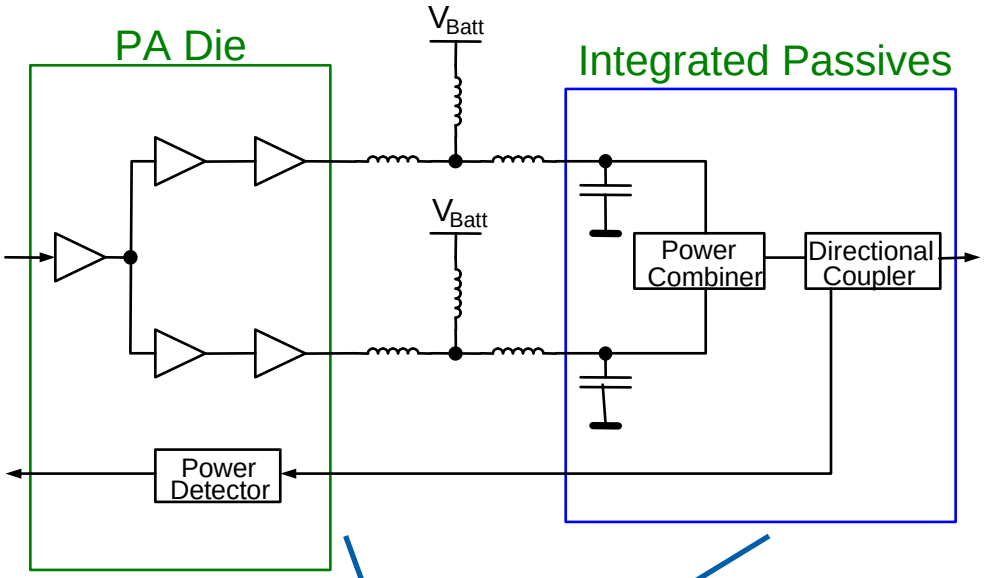
(RF-)SiP Simulations

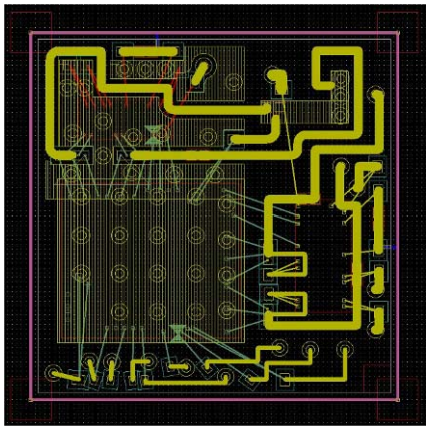
Complexity and Traditional Approaches

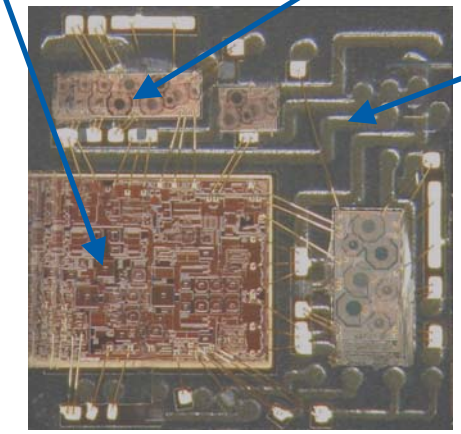
Thomas Brandtner
Infineon Technologies Austria AG

Never stop thinking

RF-SiP Example 1
Power Amplifier with Matching Network



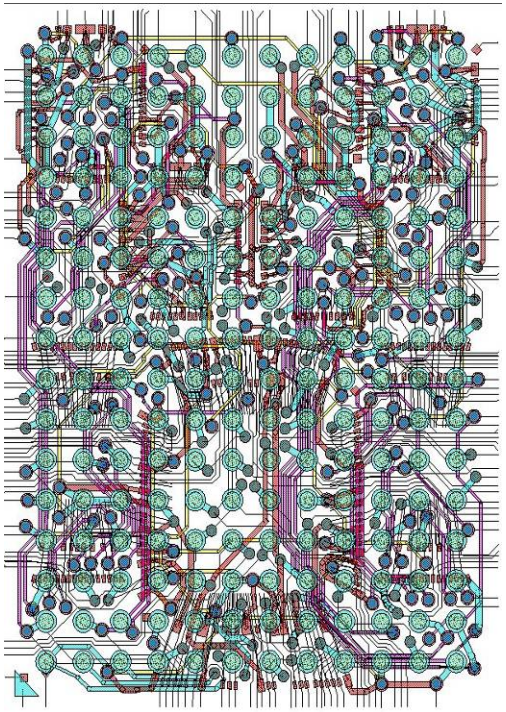


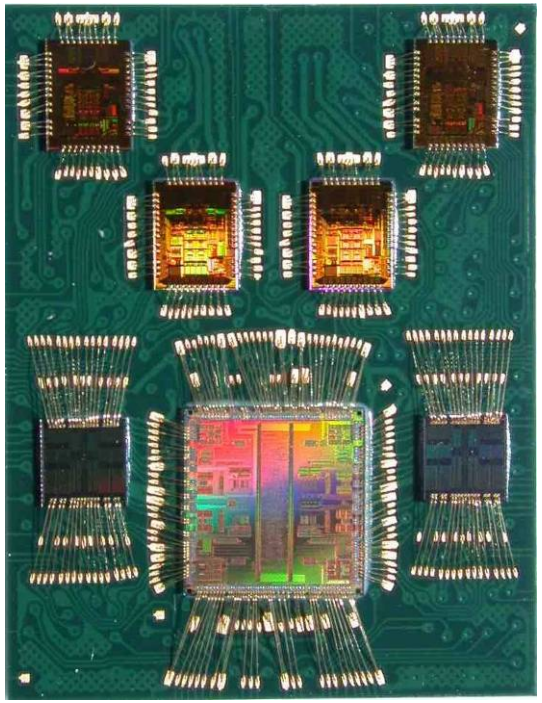


Embedded Passives

- Main SiP simulation challenge:
  „Codesign“ of PA together with the matching network

SiP Example 2
Wireline Transceiver





- Main SiP simulation challenge:
  Isolation between digital output signals and sensitive differential analog input signals up to 10 MHz
- SiP simulation flow required for low and high frequencies!

Complexity in (RF-)SiP Simulations

It‘s more than just „common“ (RF-)IC simulation:

- The design is multitude of die(s) and package (and PCB)
- Multiple process technologies
- 3D package interconnects
- Passive integration

Complexity in (RF-)SiP Simulations
The design is multitude of die(s) and package

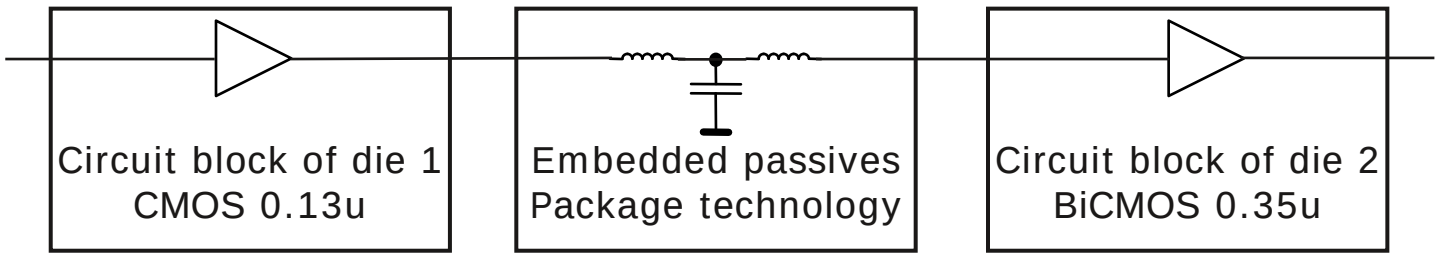
- Different design teams for the different dies and the package
  - at different sites
  - in different design environments
    (digital vs analog, Unix vs Windows)

- Simple and efficient data exchange is crucial for a smooth cooperation between the teams
- Models at various level of abstractions
  Simulator needs to have ability to handle HDL, S-params, transmission lines and transistor level models
- Non-availability of models for all the devices

- Complete design simulation fails to converge
- It takes too long to simulate the complete design.
- Debugging and tuning a portion of design requires partial design simulations
  Simulation of the “critical parts”

Complexity in (RF-)SiP Simulations
Multiple process technologies

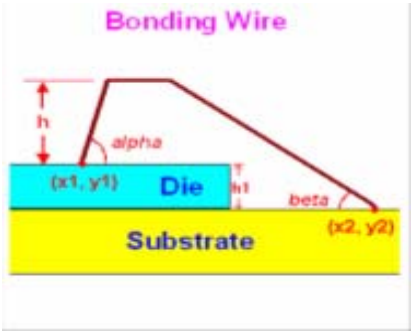
- Different process nodes for different die(s)
  - CMOS of different features sizes
  - BiCMOS or bipolar for analog front-end (LNA, Mixer, PA)
  - Dies with passives structures (C, L, transformer, ...)
- Simulation environment has to support different technologies for different blocks in one netlist
- Name space collisions in model files, e.g.
  - BSIM models of the same name
  - Parameters of the same name

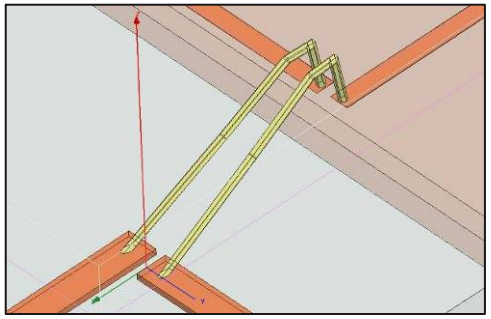


Complexity in (RF-)SiP Simulations
3D package interconnects (1)

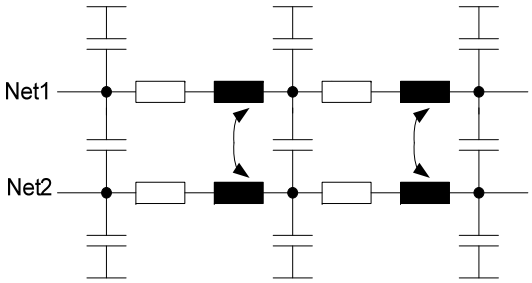
- SiP layout traces
- Wirebond or flipchip connections
- Vias (through power planes)
- Power planes (resonance modes)

- Simple 2.5D RC parasitic extraction is not sufficient any longer
  - 3D modeling of package interconnects become important (wirebond loop shape, …)



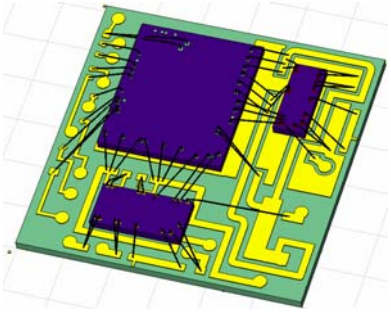


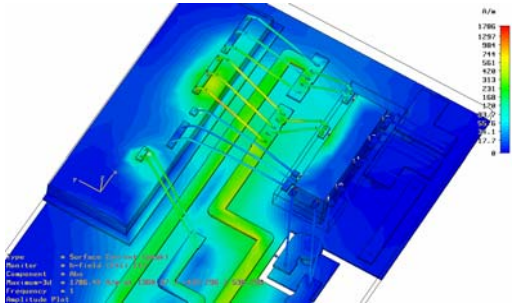
  - 3D quasi-static solvers for lower frequency issues → lumped RLCK models



Complexity in (RF-)SiP Simulations
3D package interconnects (2)

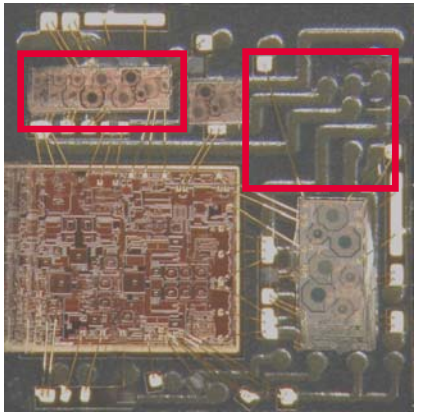
- Simple 2.5D RC parasitic extraction is not sufficient any longer
  - In RF-SiP: Extraction of transmission line effects with full-wave EM solvers for interconnects as well as embedded passives
    → S-parameter models
    → broadband behavioural models in SPICE for increased transient simulation speed





  - Large range of feature sizes (nm, um in dies; mm in packages; cm on PCB)
  - Extraction across different domains (wafer-level packaging: coupling from package interconnect to die structures)

Complexity in RF-SiP Simulations
Passive Integration



- RF SiP designs extensively use passive integration
  - to miniaturize systems and reduce costs.
  - Performance matching, tuning, filtering, and biasing.

- Two passive integration techniques that are commonly used in RF SiP designs are
  - Integrated passive devices
    - thin-film solutions of resistor and capacitor arrays
    - dies of special process technology with passives structures only
  - Embedded passives
    - directly integrated in the package substrate
    - analyzed carefully for high-order effects, such as dispersion and radiation (not only a simple RLCK parasitic extraction!)

- Exploration of design space:
  - capability to synthesize passives
  - generate models with various levels of accuracy.

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- **Traditional (RF-)SiP simulation flow**
- Using RFSiP for accelerating simulations at various stages of design
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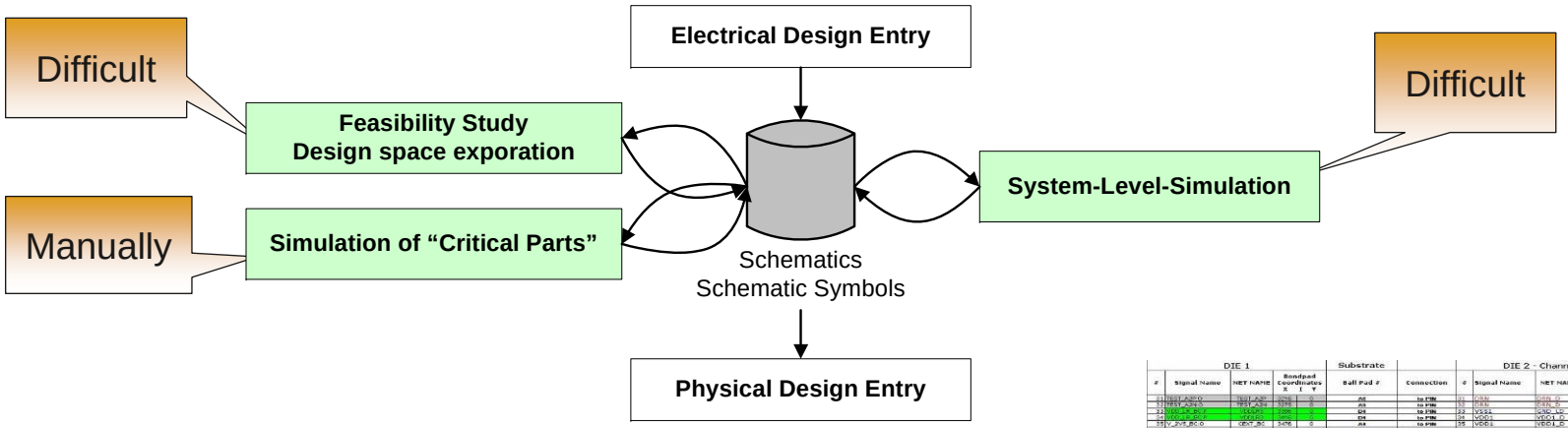
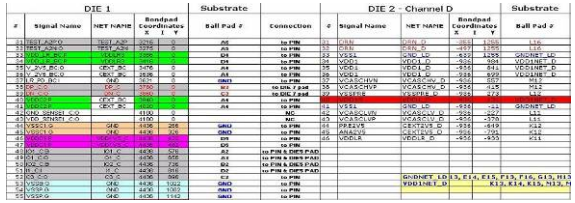
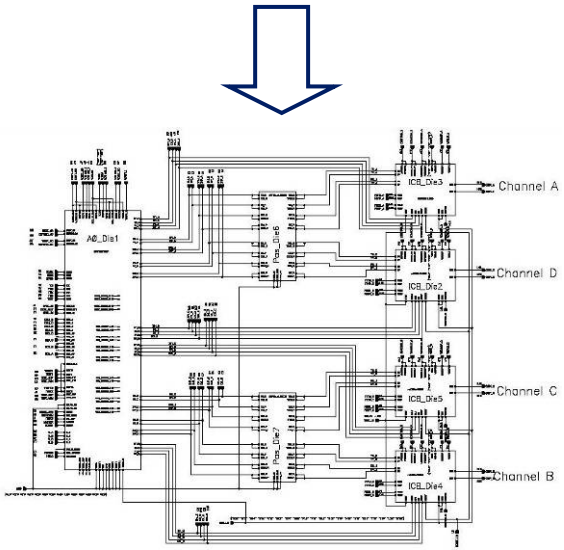
Traditional (RF-)SiP Design Flow
Electrical Design Entry and Simulation



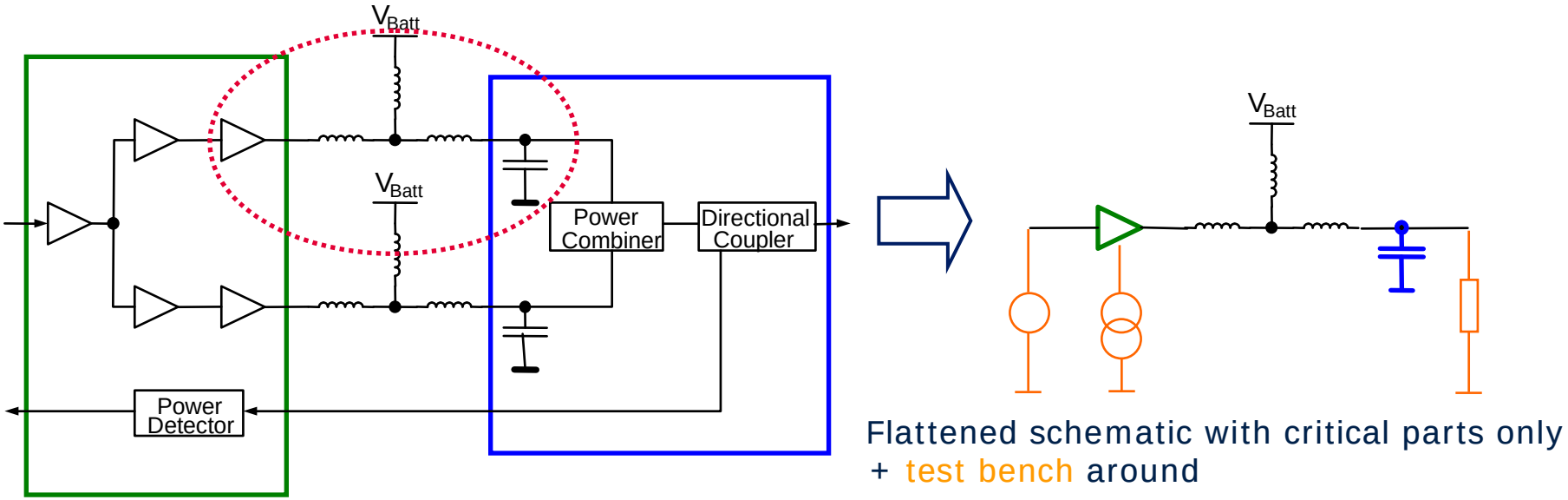




- Electrical design entry:
  Old-fashioned Excel „netlists“ replaced by schematic entry
  - Nice graphical overview
  - Automated link to system-level simulation (Verilog, VHDL netlists); but still difficult due to simulation complexity

- In parallel, introduction of table-based entry with SCM for „digital“ oriented designers

Traditional (RF-)SiP Design Flow
Simulation of Critical Parts

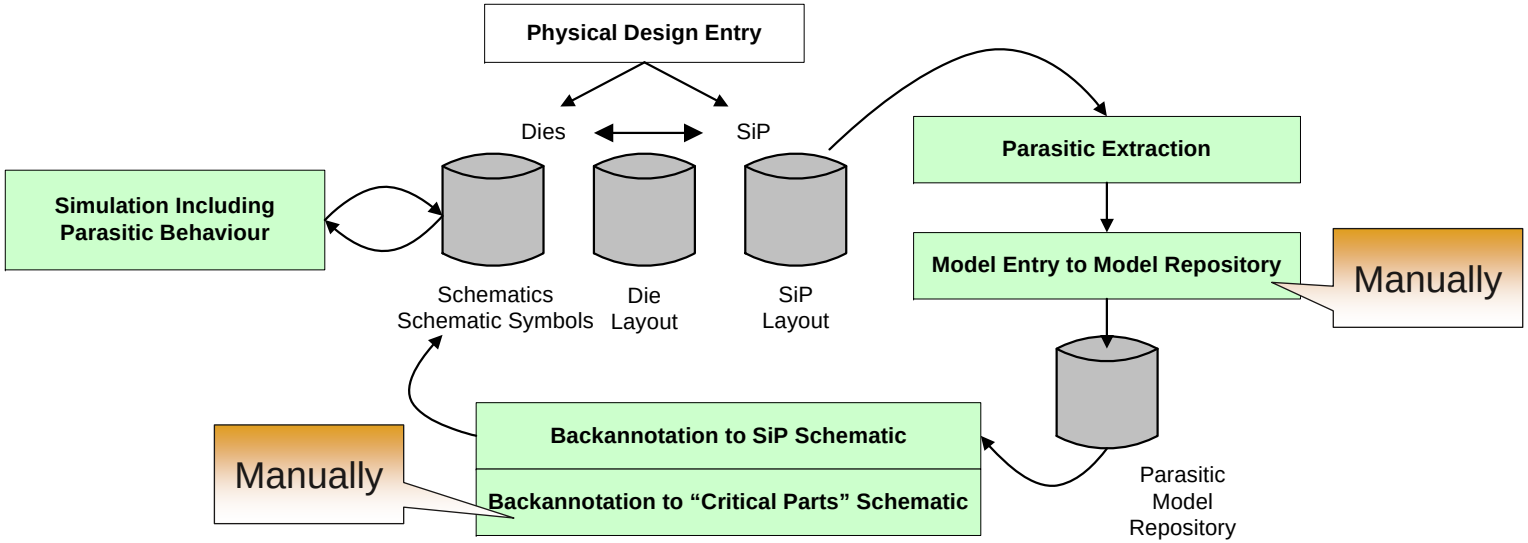


Flattened schematic with critical parts only
+ test bench around

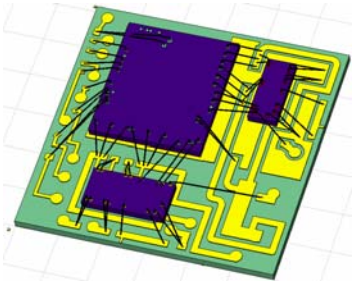
- Copy the required blocks or components from the master design to new test design.
- The blocks or components are manually connected in the new test design.
- Manually rename models across the different technology nodes to enable multi-technology simulation
- Add test-bench components (voltage and current sources, load resistors, ...)

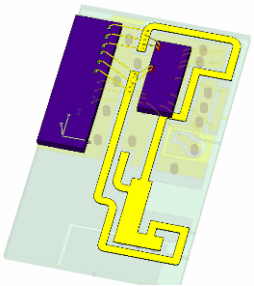
- Hope that connectivity in new test design still match with the „real world“ in the master design.

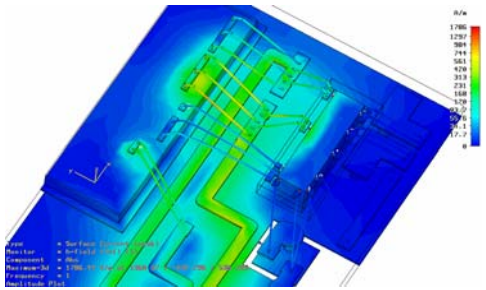
Traditional (RF-)SiP Design Flow
Manual Extraction and Insertion of Parasitics

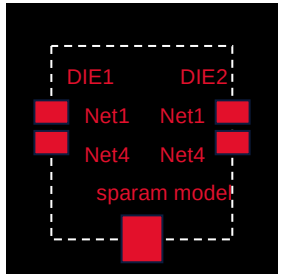


- Model extraction in a 3rd party full-wave solver (HFSS, Microwave Studio):
  - Take only parts of SiP layout to reduce complexity
  - Run extraction, hand over S-parameter Touchstone file to circuit designer
- Create schematic symbol for S-parameter model manually
- "Manual backannotation" of test design:
  - Rip up nets
  - Insert new symbols which represent parasitic models

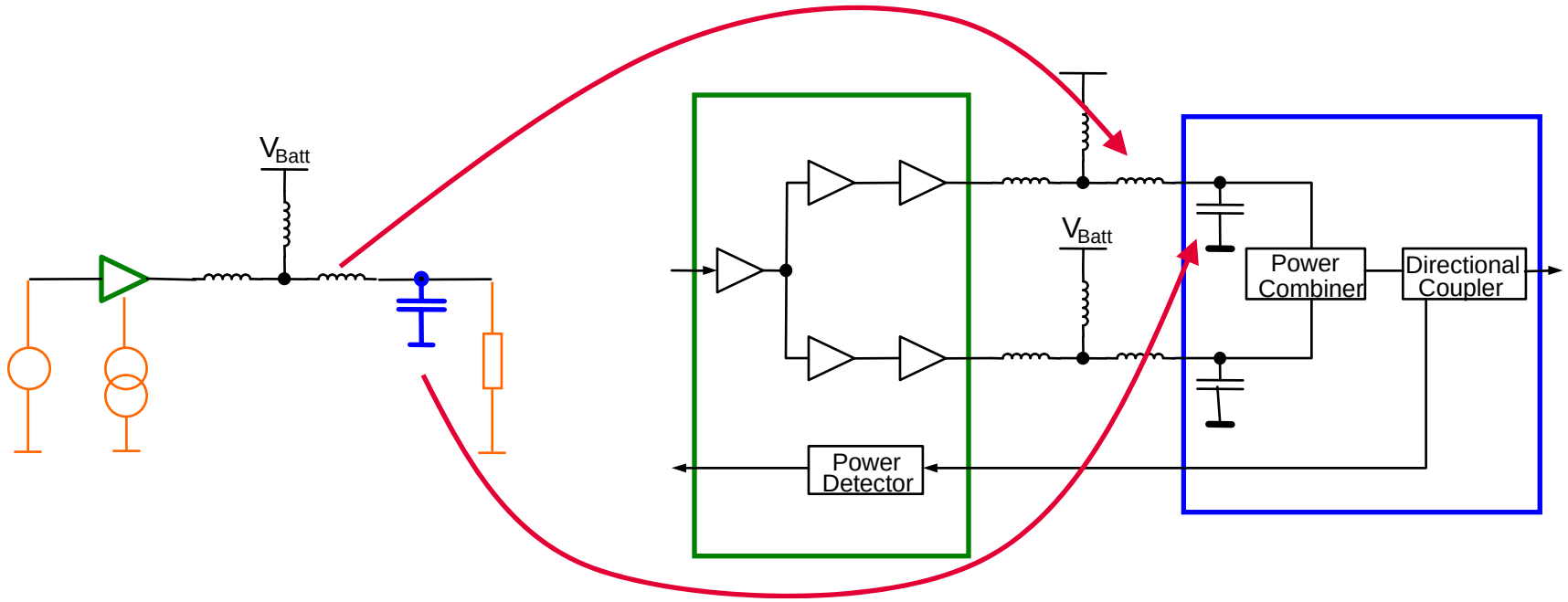








Traditional (RF-)SiP Design Flow
Updating the Master Design



- Simulate the test-bench design and tune the design parameters for optimal results.
- Manual change in master design to reflect the updated parameters
  - Instance values (R/L/C) of SMD or die components
  - Physical parameters of embedded passives
  - Constraints on nets for length of traces
- Export the master design to SiP Layout

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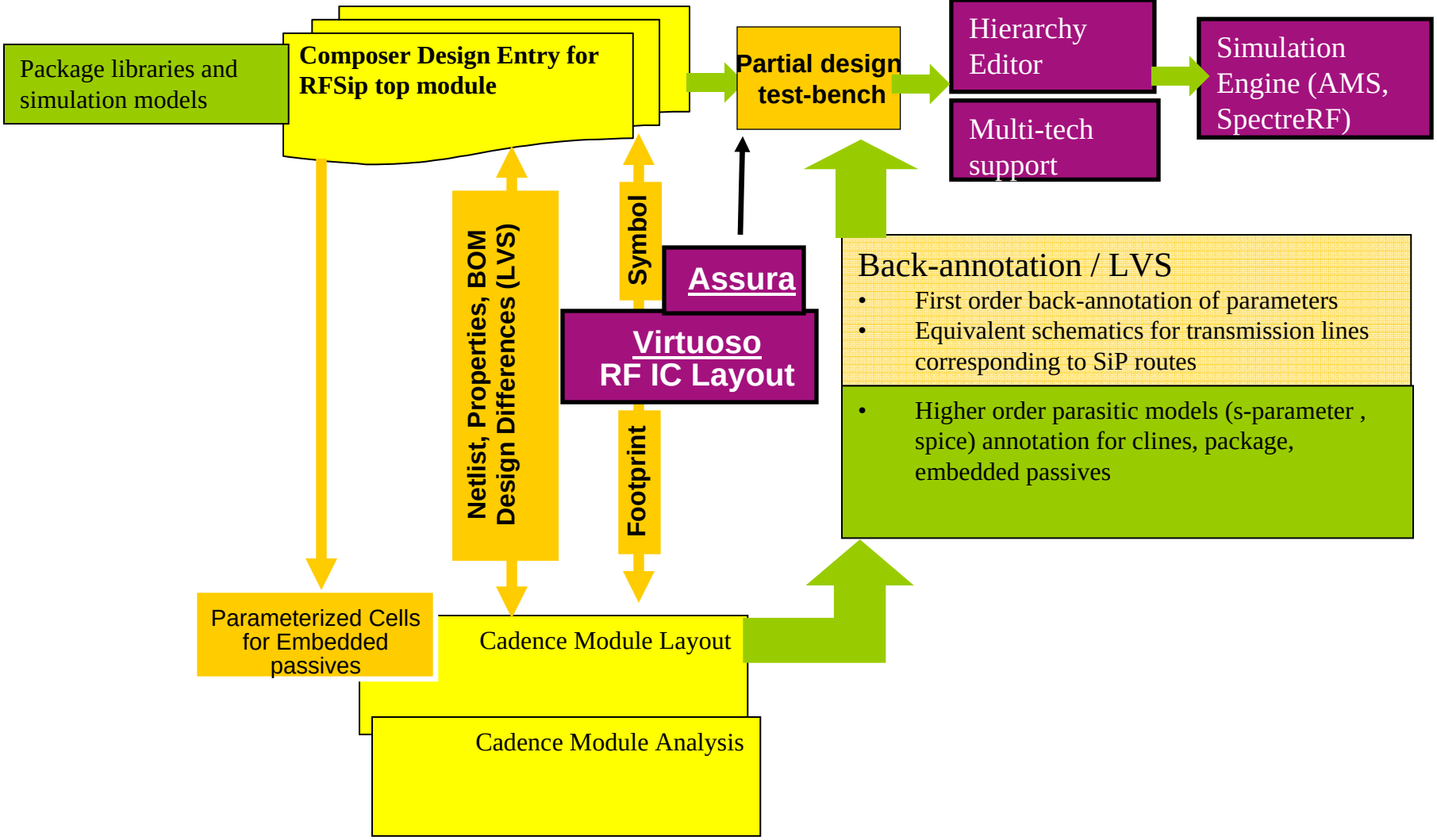
Using RFSiP for accelerating simulations at various stages of design

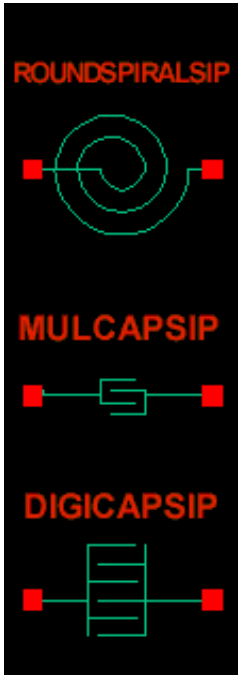
Taranjit Kukal, Cadence Design Systems

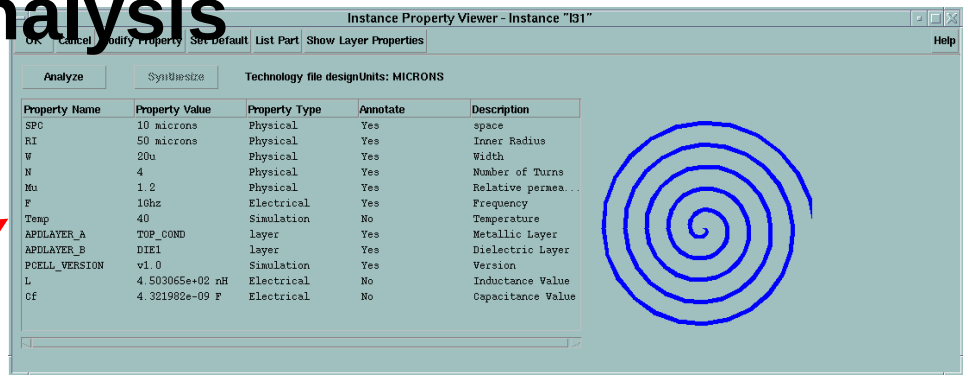
RFSiP 15.7
RFSiP 16.0

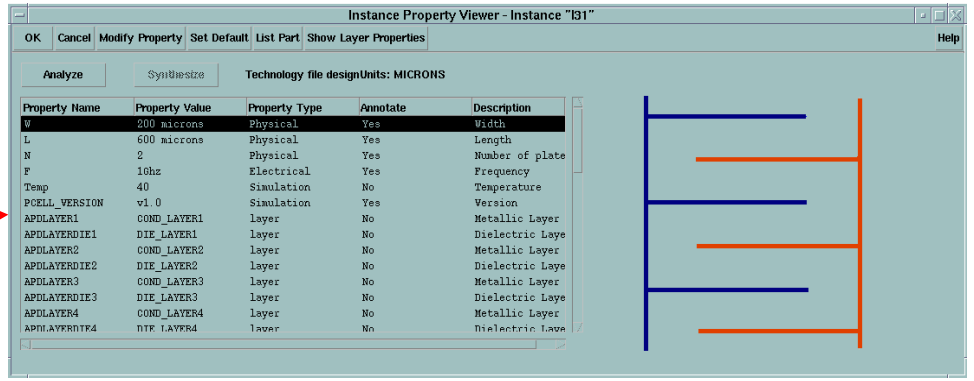


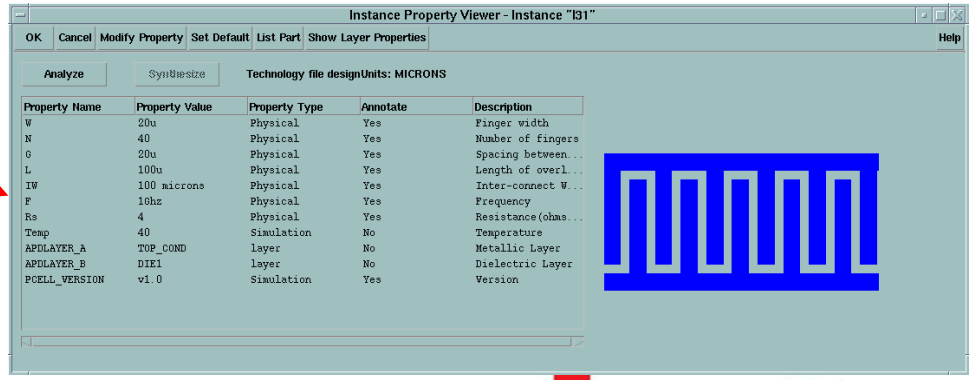
Using Cadence RFSiP Solution - Passive Structure analysis

Composer Symbol Views

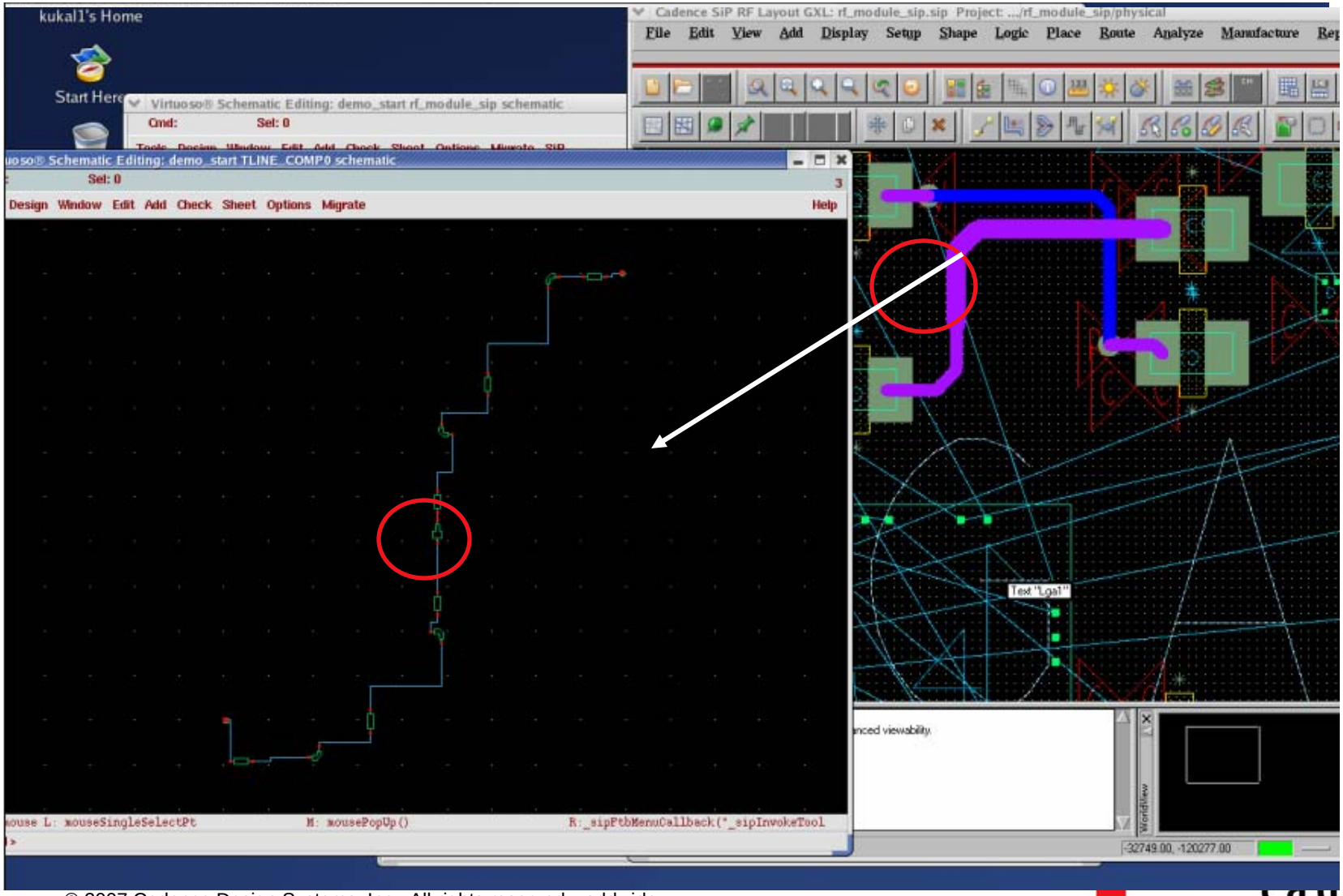






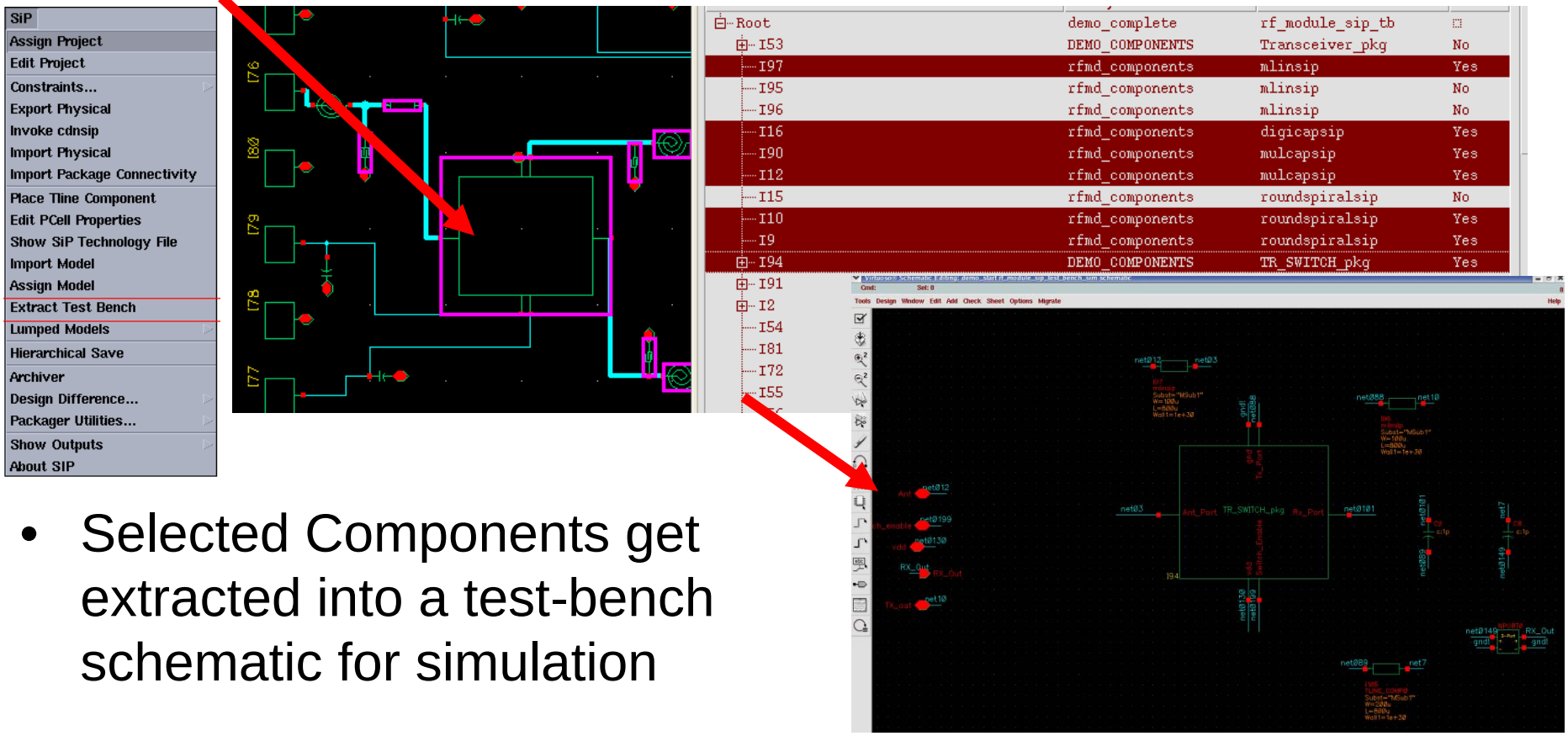


Using Cadence RFSiP Solution
- 1st order annotation through tline abutment



Using Cadence RFSiP Solution
- Critical portion of design extracted automatically

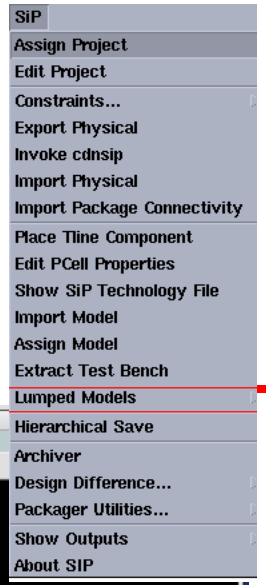
- Components selected by user for critical path simulation

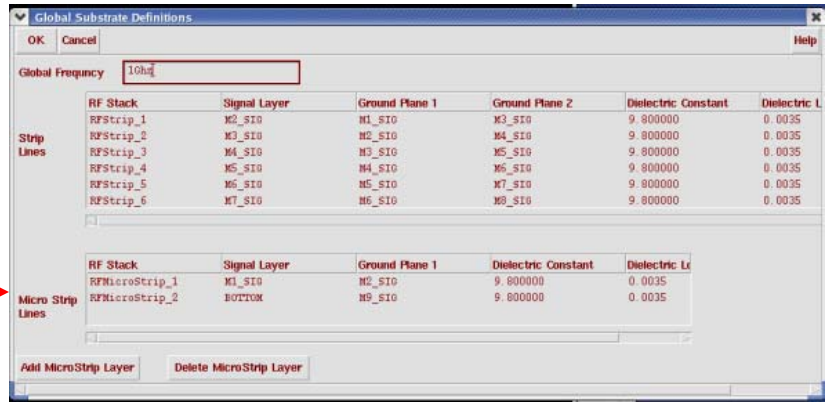


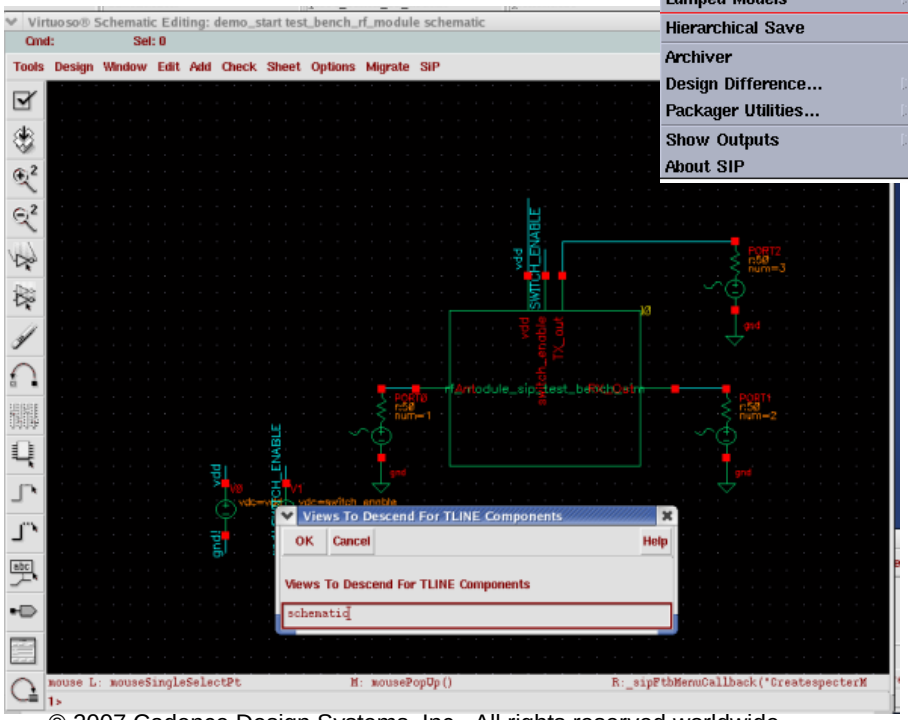
- Selected Components get extracted into a test-bench schematic for simulation

Using Cadence RFSiP Solution
- Simulating Design for trials and tuning

- Setup SiP Substrate parameters for simulations



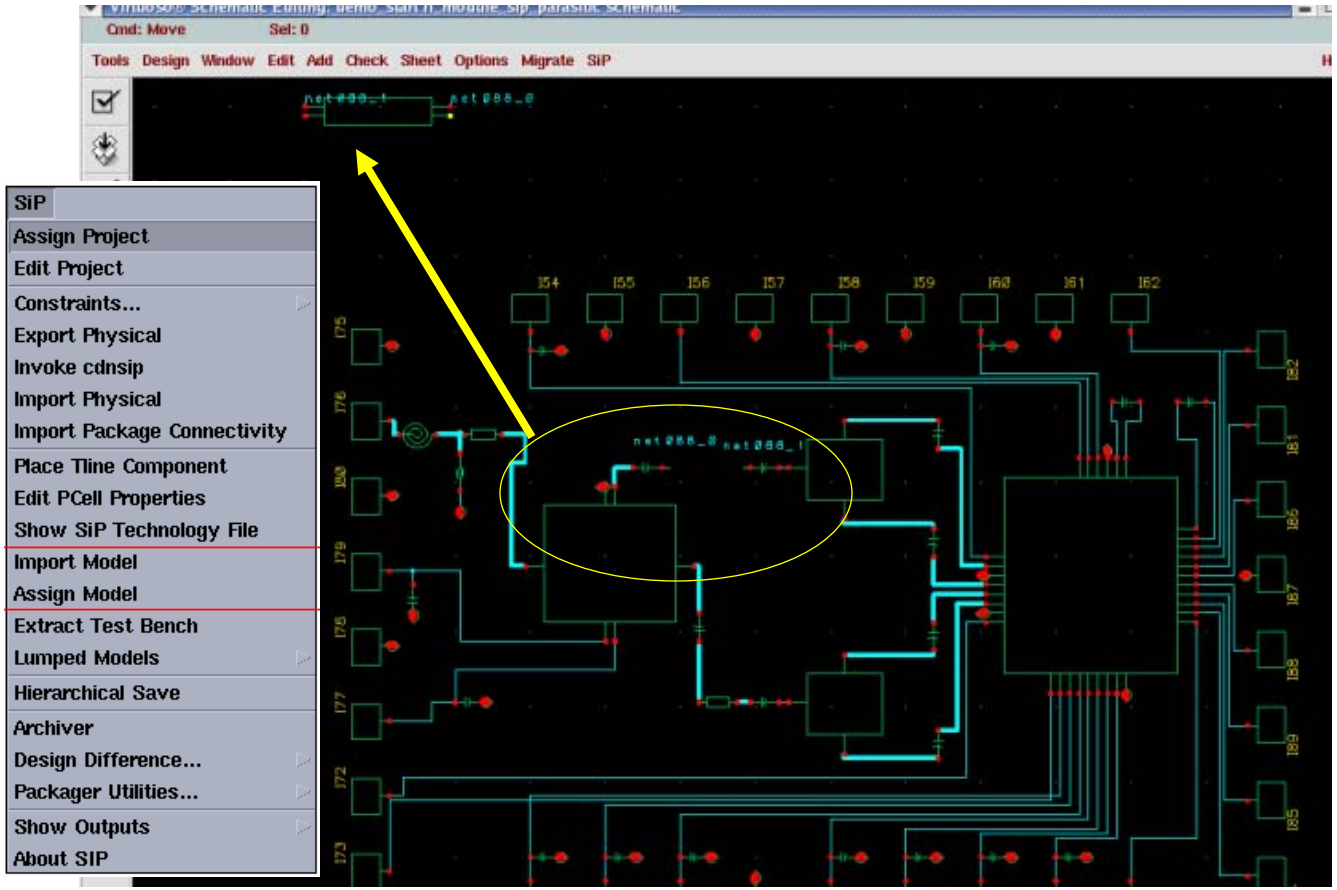




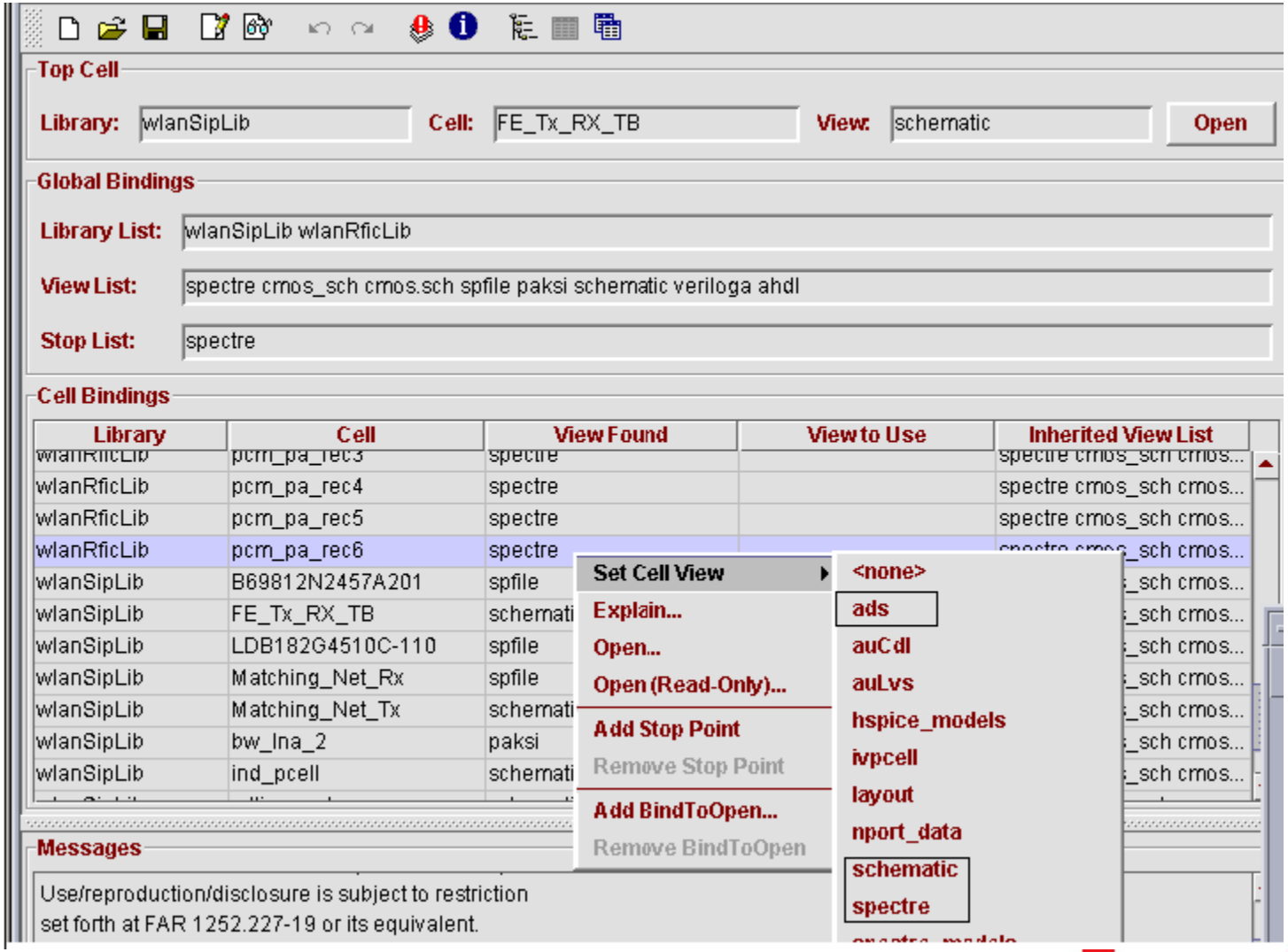
- Create lumped models for tlines and embedded passives
- Hook up stimuli
- Simulate with SpectreRF

Using Cadence RFSiP Solution
- Automatic Parasitic annotation to test-benches

- Import Model
  - Spice
  - S-parameter
- Assign Model
  - Single net
  - Coupled Nets
- Net(s) abutted and model inserted automatically



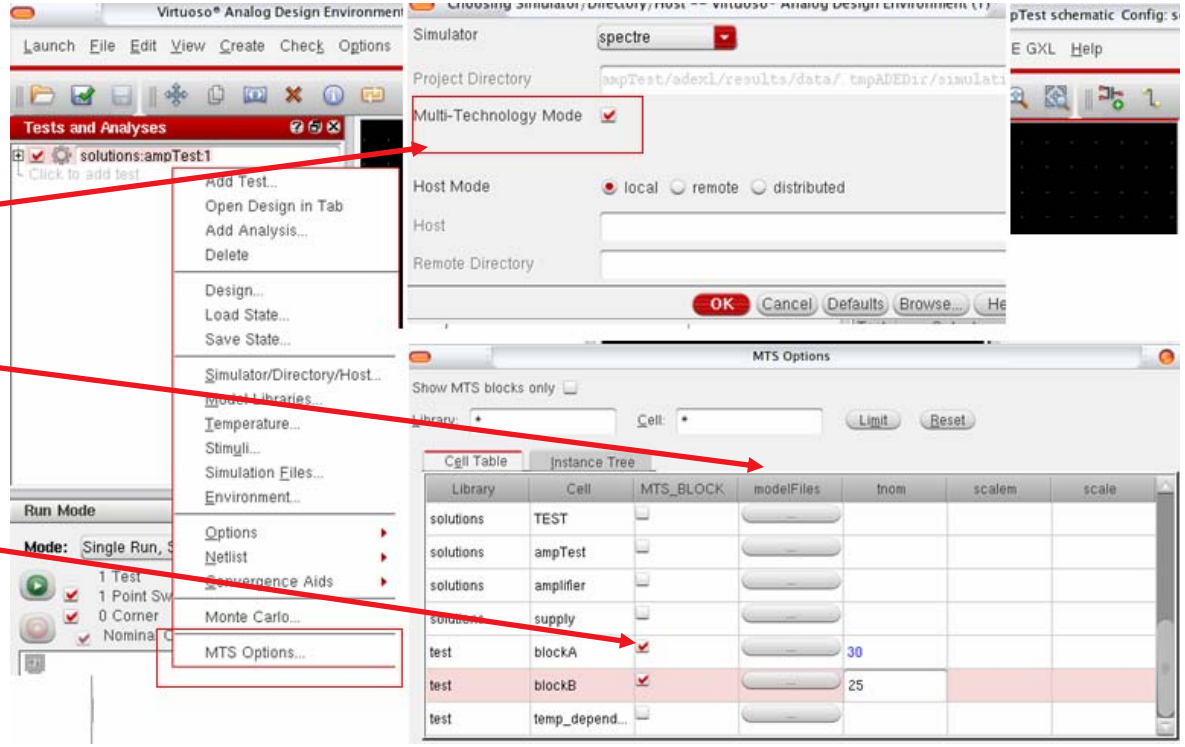
Using Cadence RFSiP Solution
- Verifying design post-layout: Xtor, HDL, tlines, s-param



Using Cadence RFSiP Solution - Simulating multi technology DIE(s)

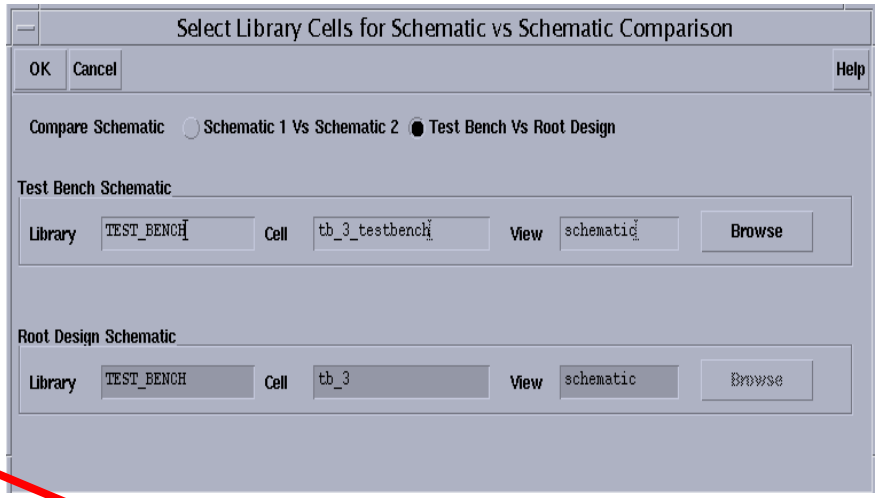
DIE(s) with different technologies can be simulated without the need of changing model names

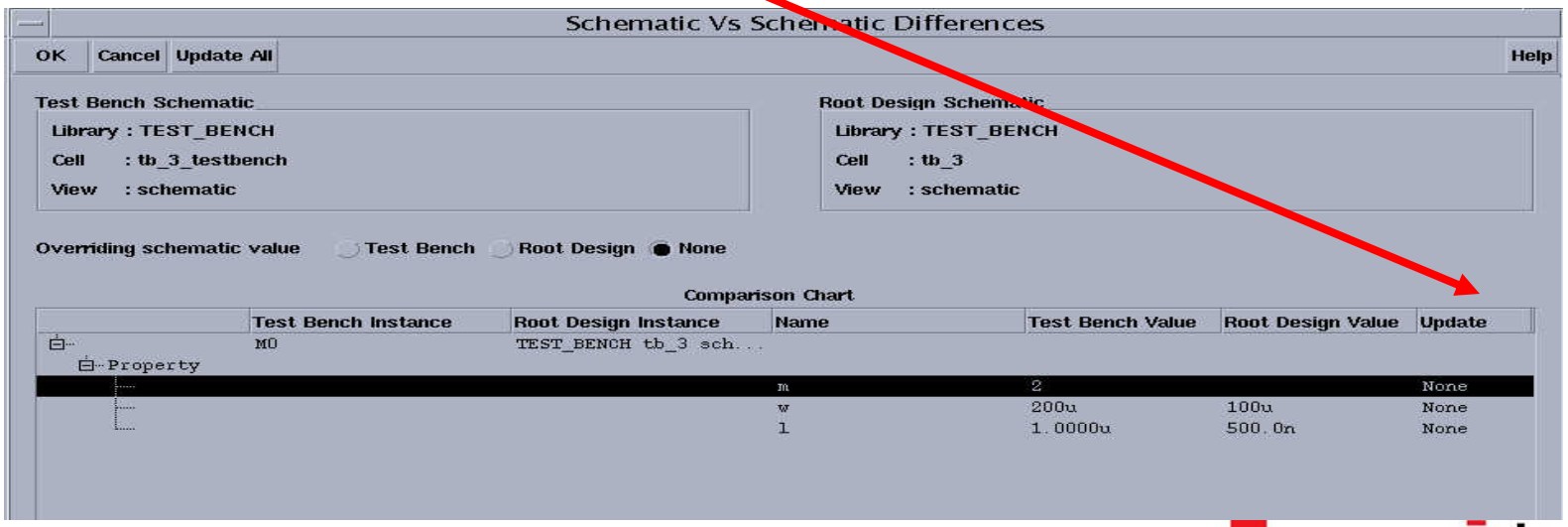
- Ability to mark blocks as MTS blocks
- Ability to set model files on a per block basis
- Ability to set MTS options (simulator specific) on a per block basis
- Works with Spectre, Ultrasim and AMS simulators



Using Cadence RFSiP Solution
- Updating Master design from testbench

- Extracted Schematic can be compared against Master Schematic
- Either schematic can be updated with changes





Using Cadence RFSiP Solution - Summary

- The Cadence RF SiP flow eliminates the need for:
  - Capturing designs twice for purposes of simulation and SiP implementation
  - Creating separate testbench designs for analysis and simulations, followed by manual sync-ups with the master design
  - Manual insertion of parasitic models (obtained from third-party sources) into the testbench design
  - Manual renaming of models for different dies that are on different technology nodes
  - Explicit export of layout structures to third-party solvers for extraction

Using Cadence RFSiP Solution - Summary

- The Cadence RF SiP flow promotes:
  - Single front-end driven simulation and implementation covering both
    - IC layout
    - SiP layout
  - Easy analysis of Embedded passives with physical parameters
  - Pre-layout simulations with 1st order simulations that are fast and allow rapid exploration
  - Post-layout verification with multitude of DIE technologies and package parasitics
  - Use of integrated solvers for 3-D structures and RF Shapes

Agenda

- Introduction to RFSiP
- Complexity in RFSiP simulations
- Traditional approach used at IFX for simulation of RFSiP
- Using RFSiP for accelerating simulations at various stages of design
- **Conclusions**

Conclusion

- RFSiP 15.7 design flow used at Infineon for productive designs.
  The following features are mainly used:
  - Schematic entry
  - Automated link between Composer and Allegro CDNSIP

  Productivity gain of 2-3 man weeks for a RF-SiP design (Example 1) in comparison to old Excel style

- Some RFSiP 16.0 features specified together with Cadence:
  - Parasitic model import
  - Automated model backannotation
  - Automated testbench generation (“critical parts”)

  Expected productivity gain due to faster loops between design and simulation steps and decreased number of manual errors.

- RFSiP 16.0 will be offered for productive designs in Infineon’s next internal chip/package codesign flow release.

- Infineon would like to see “one common” SiP flow solution rather than a split between RFSiP and digital-SiP (SCM, IOP):
  - Support of SCM or Composer for connectivity entry independent of type of top-level die design (analog or digital)
  - One common IO-Planner for both digital and analog designs based on OA database.

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