

# Automated Parasitic Backannotation and Testbench Generation for Verification of RF-SiP Designs

Taranjit Kukal, Cadence Design Systems  
Thomas Brandtner, Infineon Technologies Austria AG

Session 8.1





# Agenda

- Introduction to RFSiP
- Complexity in RFSiP simulations
- Traditional RFSiP simulation flow at Infineon
- Using RFSiP for accelerating simulations at various stages of design
- Conclusions



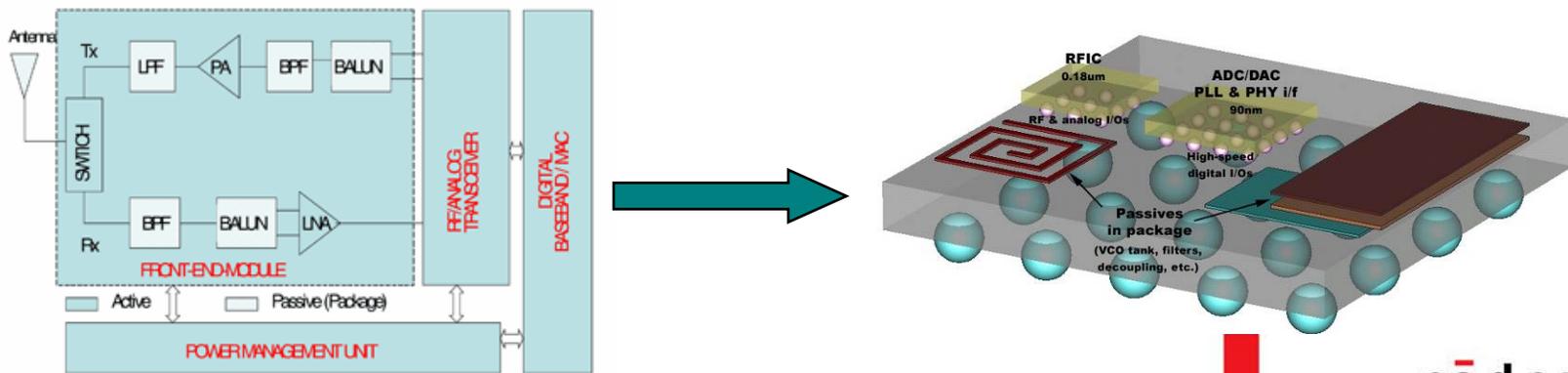
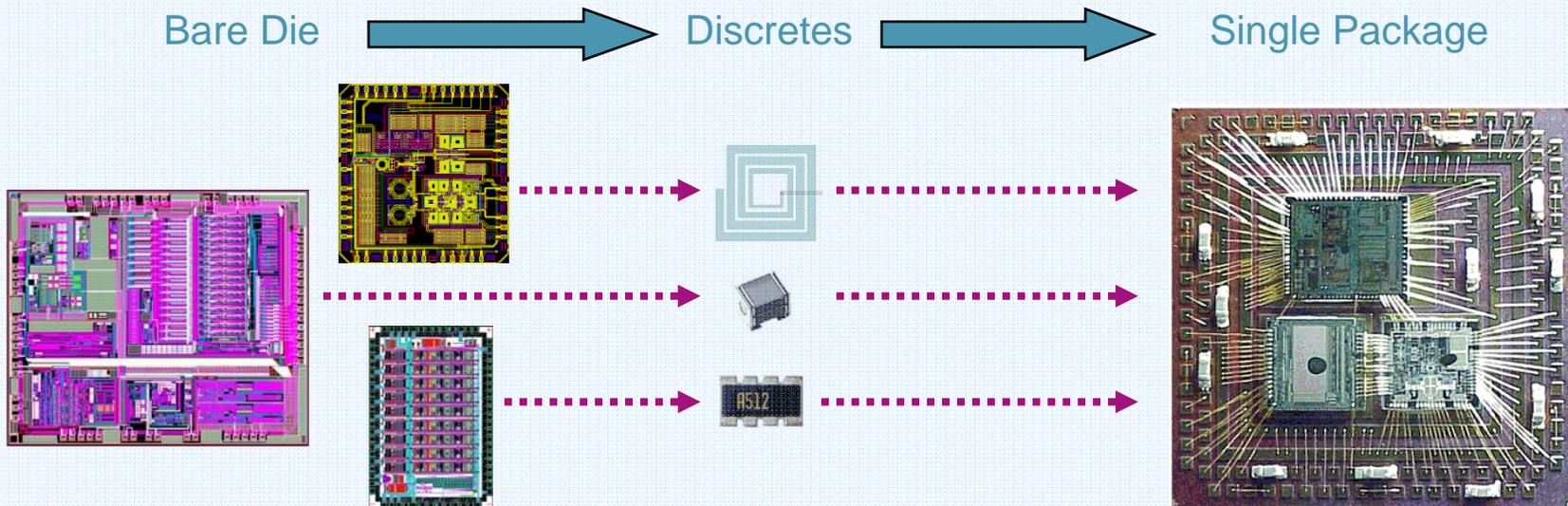
# Agenda

- **Introduction to RFSiP**
- Complexity in RFSiP simulations
- Traditional RFSiP simulation flow at Infineon
- Using RFSiP for accelerating simulations at various stages of design
- Conclusions

# Introduction to RFSiP

## A Complete System or Sub-System in a Single Package

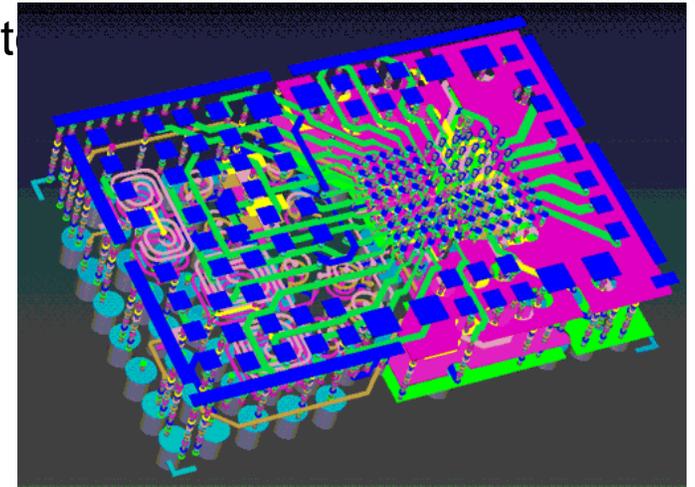
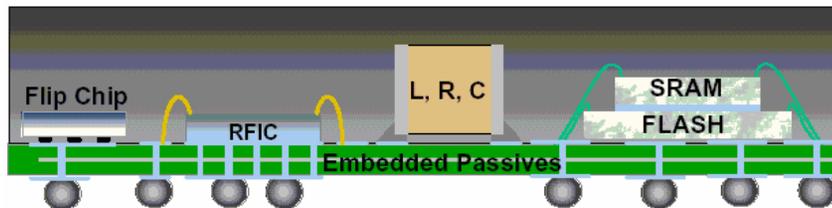
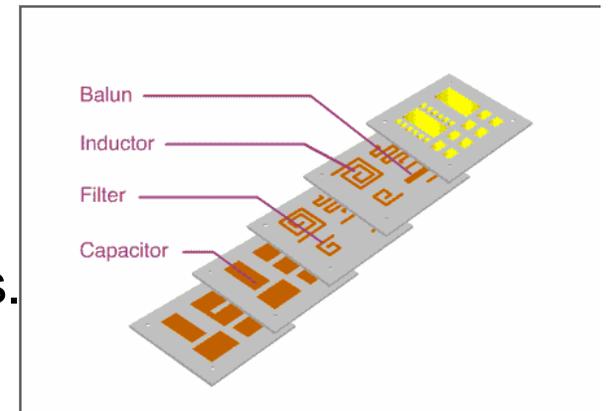
*Integration of Multiple IC's (bare die) and Discrete Devices (SMD & Embedded) into One Package rather than One IC (SoC)*



# Introduction to RFSiP

## - Why SiP for RF Design?

- RF IC's Typically Take 3-5 Mfr. Passes.
  - Mask Sets Cost About 3-5 Million Dollars
  - 6 Month Impact to Schedule
- LTCC (Low Temp. Co-fired Ceramic) Modules.
  - Total Cost Less Than 500K for 3-5 Passes.
  - 6 Week Impact to Schedule
- Mixed Technology Support.
  - Not Limited by Homogeneous Semiconductors  
GaAs, SiGe all on One Substrate
  - Flexible Design Partitioning
  - Embedded passives – metal structures





# Agenda

- Introduction to RFSiP
- **Complexity in RFSiP simulations**
- Traditional RFSiP simulation flow at Infineon
- Using RFSiP for accelerating simulations at various stages of design
- Conclusions

# (RF-)SiP Simulations

## Complexity and Traditional Approaches

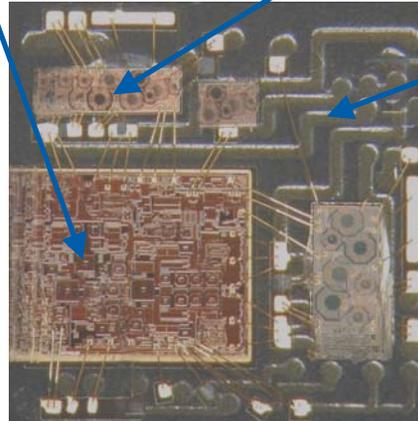
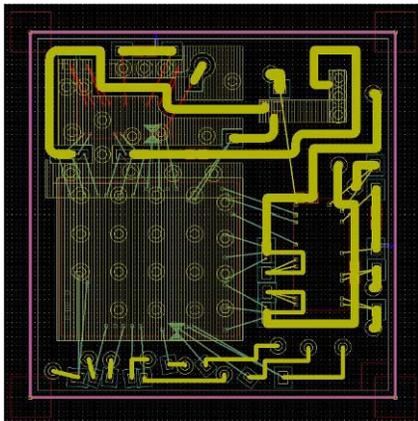
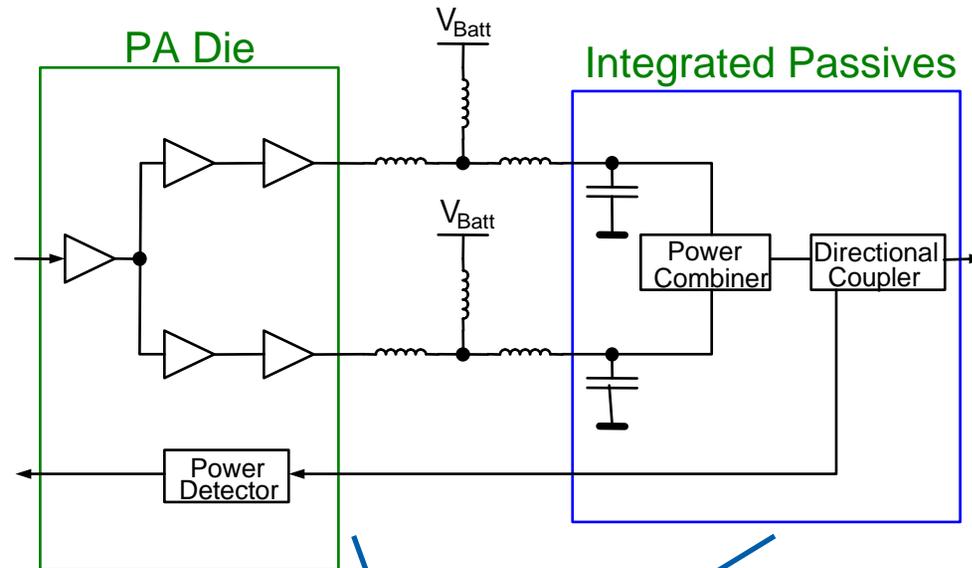
Thomas Brandtner  
Infineon Technologies Austria AG



Never stop thinking

# RF-SiP Example 1

## Power Amplifier with Matching Network

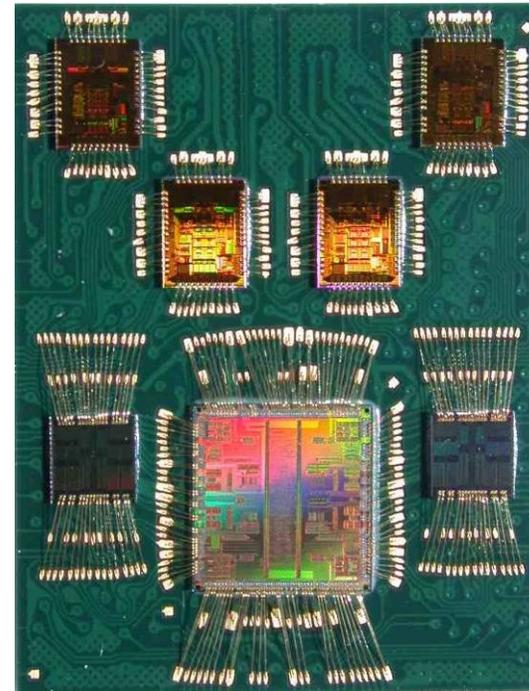
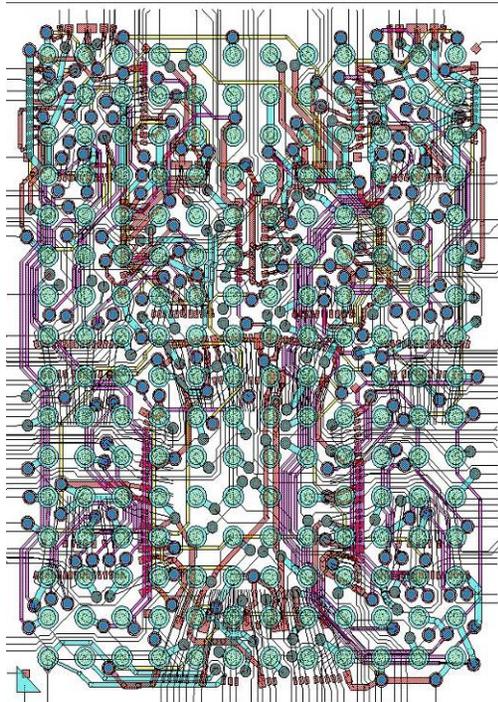


Embedded Passives

- Main SiP simulation challenge:  
„Codesign“ of PA together with the matching network

# SiP Example 2

## Wireline Transceiver



- Main SiP simulation challenge:  
Isolation between digital output signals and sensitive differential analog input signals up to 10 MHz
- SiP simulation flow required for low and high frequencies!

# Complexity in (RF-)SiP Simulations

It's more than just „common“ (RF-)IC simulation:

- The design is multitude of die(s) and package (and PCB)
- Multiple process technologies
- 3D package interconnects
- Passive integration

# Complexity in (RF-)SiP Simulations

## The design is multitude of die(s) and package



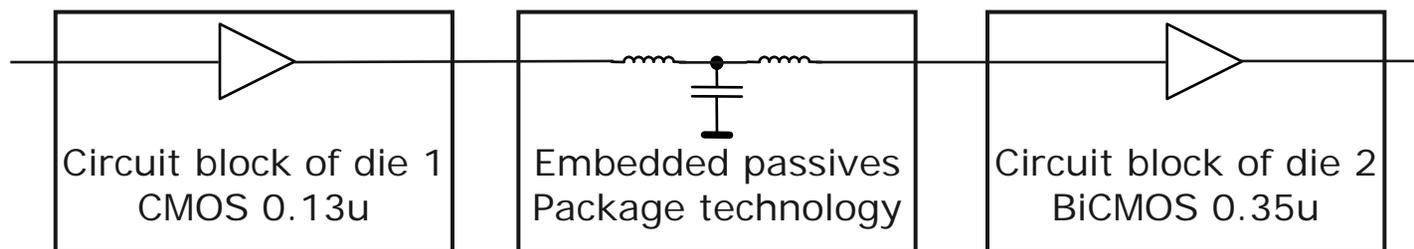
- Different design teams for the different dies and the package
  - at different sites
  - in different design environments  
(digital vs analog, Unix vs Windows)
- Simple and efficient data exchange is crucial for a smooth cooperation between the teams
- Models at various level of abstractions  
Simulator needs to have ability to handle HDL, S-params, transmission lines and transistor level models
- Non-availability of models for all the devices
- Complete design simulation fails to converge
- It takes too long to simulate the complete design.
- Debugging and tuning a portion of design requires partial design simulations  
Simulation of the “critical parts”

# Complexity in (RF-)SiP Simulations

## Multiple process technologies



- Different process nodes for different die(s)
  - CMOS of different features sizes
  - BiCMOS or bipolar for analog front-end (LNA, Mixer, PA)
  - Dies with passives structures (C, L, transformer, ...)
- Simulation environment has to support different technologies for different blocks in one netlist
- Name space collisions in model files, e.g.
  - BSIM models of the same name
  - Parameters of the same name

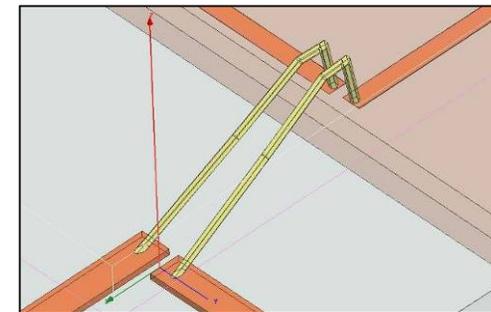
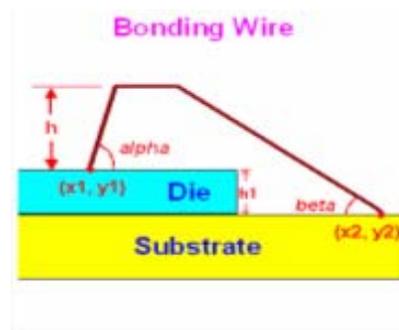


# Complexity in (RF-)SiP Simulations

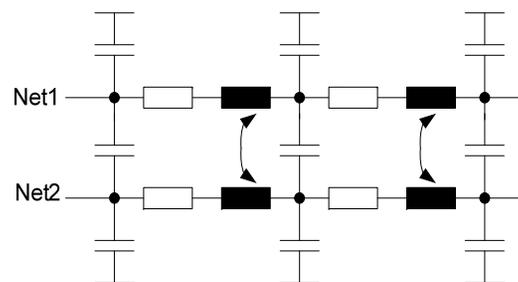
## 3D package interconnects (1)



- SiP layout traces
- Wirebond or flipchip connections
- Vias (through power planes)
- Power planes (resonance modes)
  
- Simple 2.5D RC parasitic extraction is not sufficient any longer
  - 3D modeling of package interconnects become important (wirebond loop shape, ...)



- 3D quasi-static solvers for lower frequency issues
  - lumped RLCK models

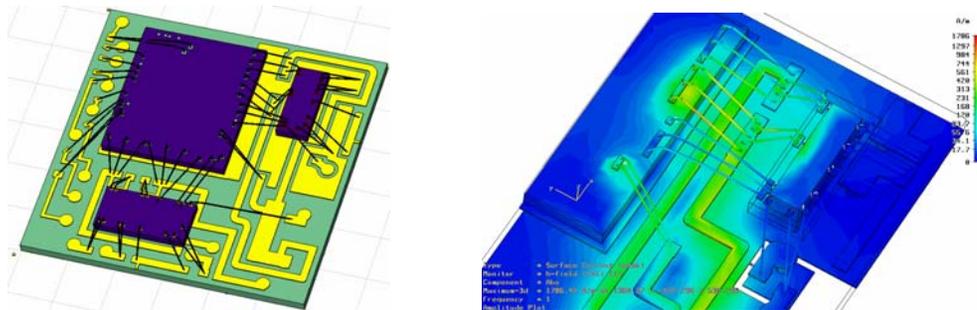


# Complexity in (RF-)SiP Simulations

## 3D package interconnects (2)



- Simple 2.5D RC parasitic extraction is not sufficient any longer
  - In RF-SiP: Extraction of transmission line effects with full-wave EM solvers for interconnects as well as embedded passives
    - S-parameter models
    - broadband behavioural models in SPICE for increased transient simulation speed



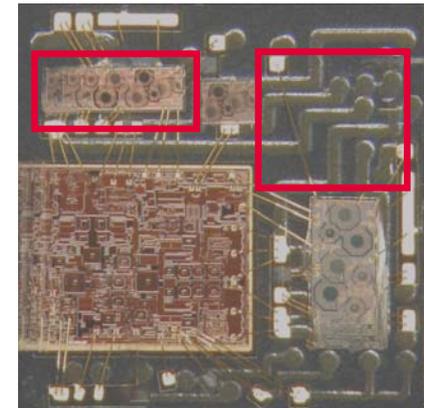
- Large range of feature sizes (nm, um in dies; mm in packages; cm on PCB)
- Extraction across different domains (wafer-level packaging: coupling from package interconnect to die structures)

# Complexity in RF-SiP Simulations

## Passive Integration



- RF SiP designs extensively use passive integration
  - to miniaturize systems and reduce costs.
  - Performance matching, tuning, filtering, and biasing.
  
- Two passive integration techniques that are commonly used in RF SiP designs are
  - Integrated passive devices
    - thin-film solutions of resistor and capacitor arrays
    - dies of special process technology with passives structures only
  - Embedded passives
    - directly integrated in the package substrate
    - analyzed carefully for high-order effects, such as dispersion and radiation (not only a simple RLCK parasitic extraction!)
  
- Exploration of design space:
  - capability to synthesize passives
  - generate models with various levels of accuracy.

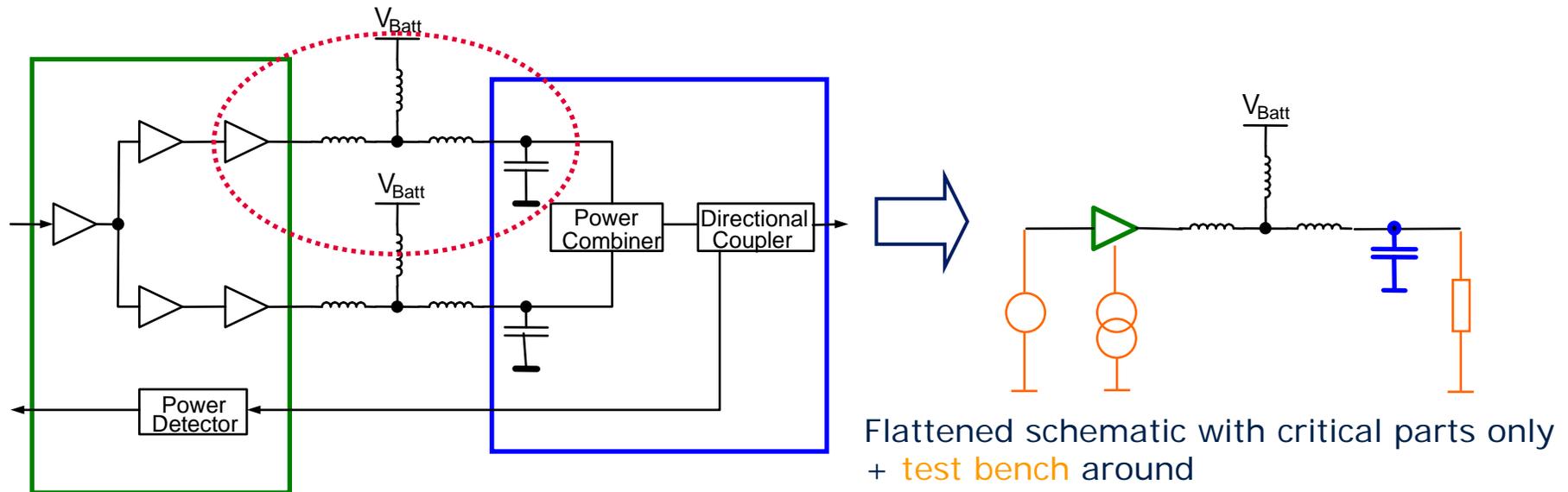


# Agenda

- Introduction to RFSiP
- Complexity in (RF-)SiP simulations
- **Traditional (RF-)SiP simulation flow**
- Using RFSiP for accelerating simulations at various stages of design
- Conclusions



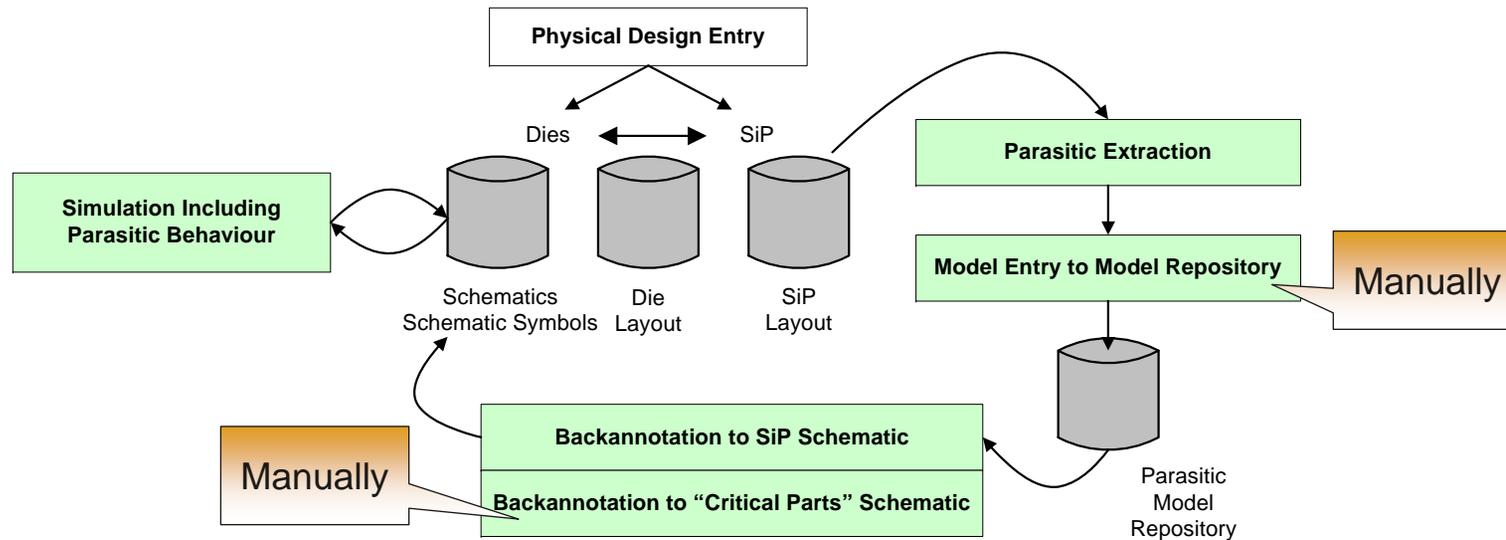
# Traditional (RF-)SiP Design Flow Simulation of Critical Parts



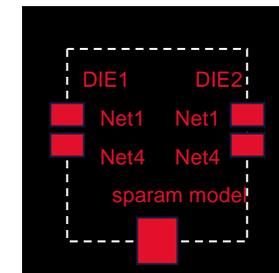
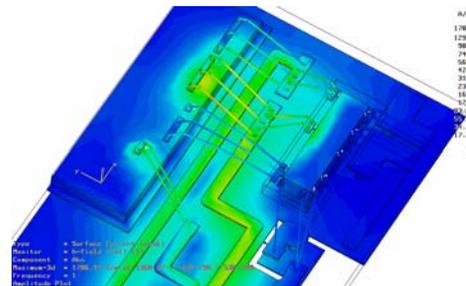
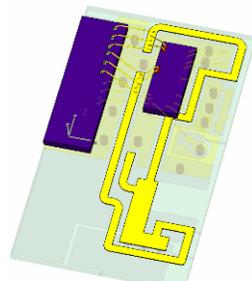
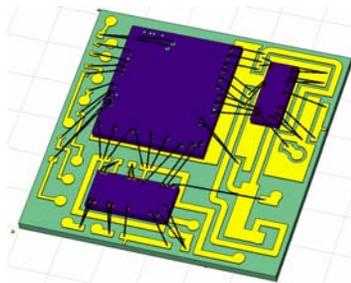
- Copy the required blocks or components from the master design to new test design.
- The blocks or components are manually connected in the new test design.
- Manually rename models across the different technology nodes to enable multi-technology simulation
- Add test-bench components (voltage and current sources, load resistors, ...)
- Hope that connectivity in new test design still match with the „real world“ in the master design.

# Traditional (RF-)SiP Design Flow

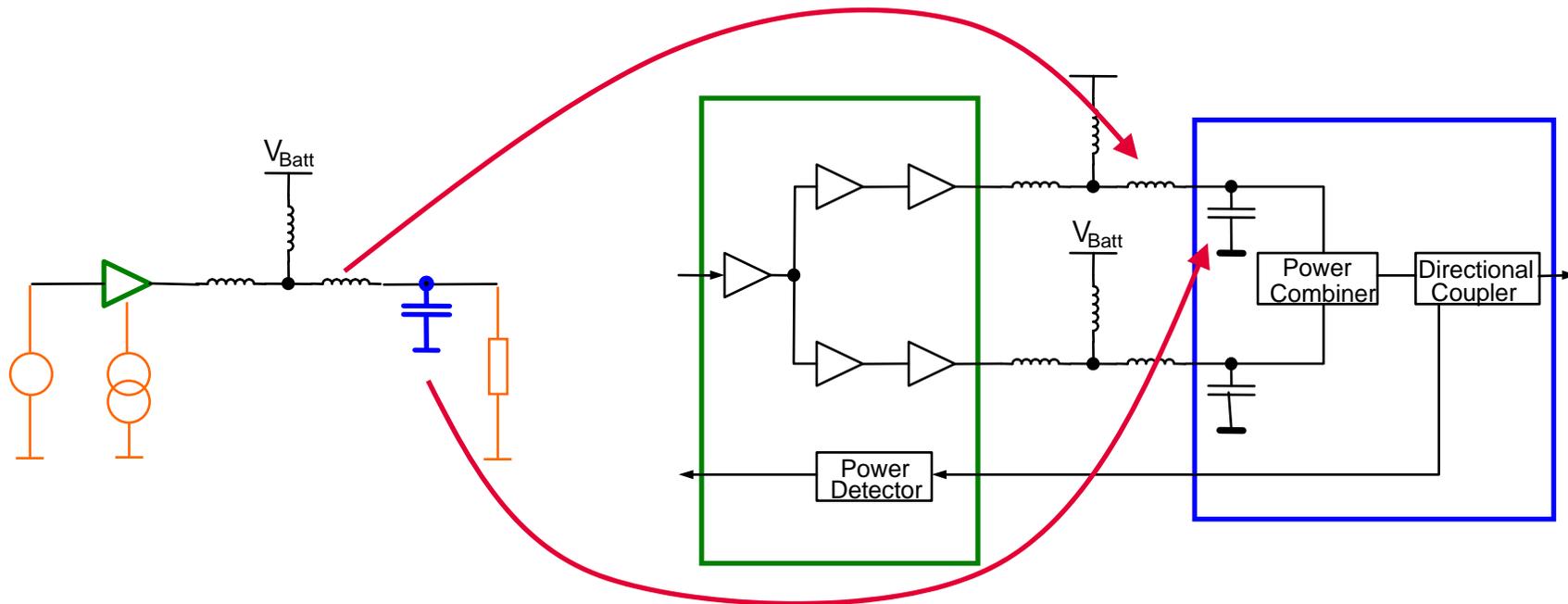
## Manual Extraction and Insertion of Parasitics



- Model extraction in a 3rd party full-wave solver (HFSS, Microwave Studio):
  - Take only parts of SiP layout to reduce complexity
  - Run extraction, hand over S-parameter Touchstone file to circuit designer
- Create schematic symbol for S-parameter model manually
- “Manual backannotation” of test design:
  - Rip up nets
  - Insert new symbols which represent parasitic models



# Traditional (RF-)SiP Design Flow Updating the Master Design



- Simulate the test-bench design and tune the design parameters for optimal results.
- Manual change in master design to reflect the updated parameters
  - Instance values (R/L/C) of SMD or die components
  - Physical parameters of embedded passives
  - Constraints on nets for length of traces
- Export the master design to SiP Layout



# Agenda

- Introduction to RFSiP
- Complexity in RFSiP simulations
- Traditional RFSiP simulation flow at Infineon
- **Using RFSiP for accelerating simulations at various stages of design**
- Conclusions

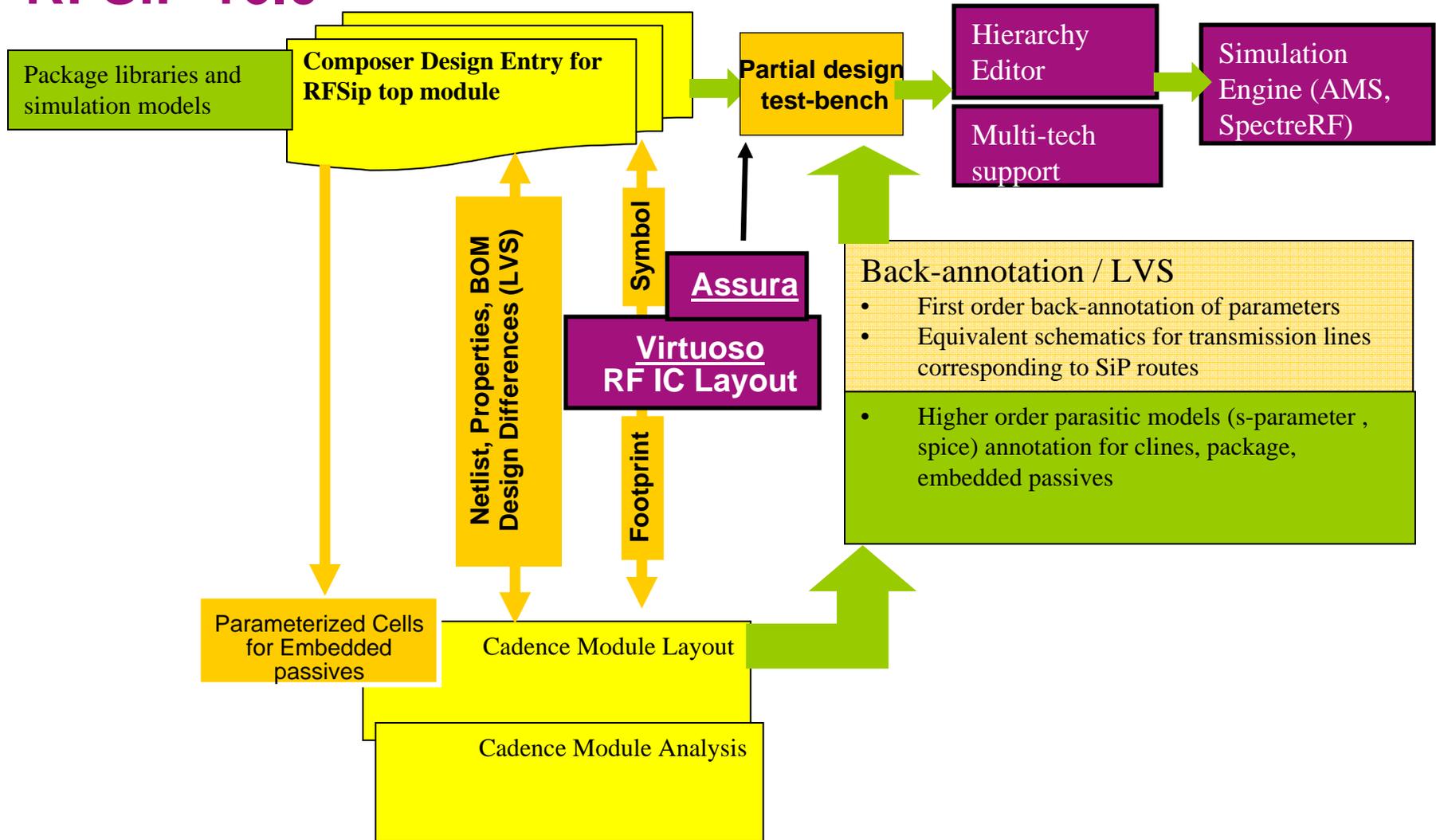
# Using RFSiP for accelerating simulations at various stages of design

Taranjit Kukal, Cadence Design Systems



# RFSiP 15.7

## RFSiP 16.0



# Using Cadence RFSiP Solution - Passive Structure analysis

## Composer Symbol Views



Instance Property Viewer - Instance "I31"

Analyze Synthesize Technology file designUnits: MICRONS

Property Name	Property Value	Property Type	Annotate	Description
SPC	10 microns	Physical	Yes	space
RI	50 microns	Physical	Yes	Inner Radius
W	20u	Physical	Yes	Width
N	4	Physical	Yes	Number of Turns
Mu	1.2	Physical	Yes	Relative permea...
F	1ghz	Electrical	Yes	Frequency
Temp	40	Simulation	No	Temperature
APDLAYER_A	TOP_COND	layer	Yes	Metallic Layer
APDLAYER_B	DIE1	layer	Yes	Dielectric Layer
PCELL_VERSION	v1.0	Simulation	Yes	Version
L	4.503065e+02 nH	Electrical	No	Inductance Value
CF	4.321982e-09 F	Electrical	No	Capacitance Value

Instance Property Viewer - Instance "I31"

Analyze Synthesize Technology file designUnits: MICRONS

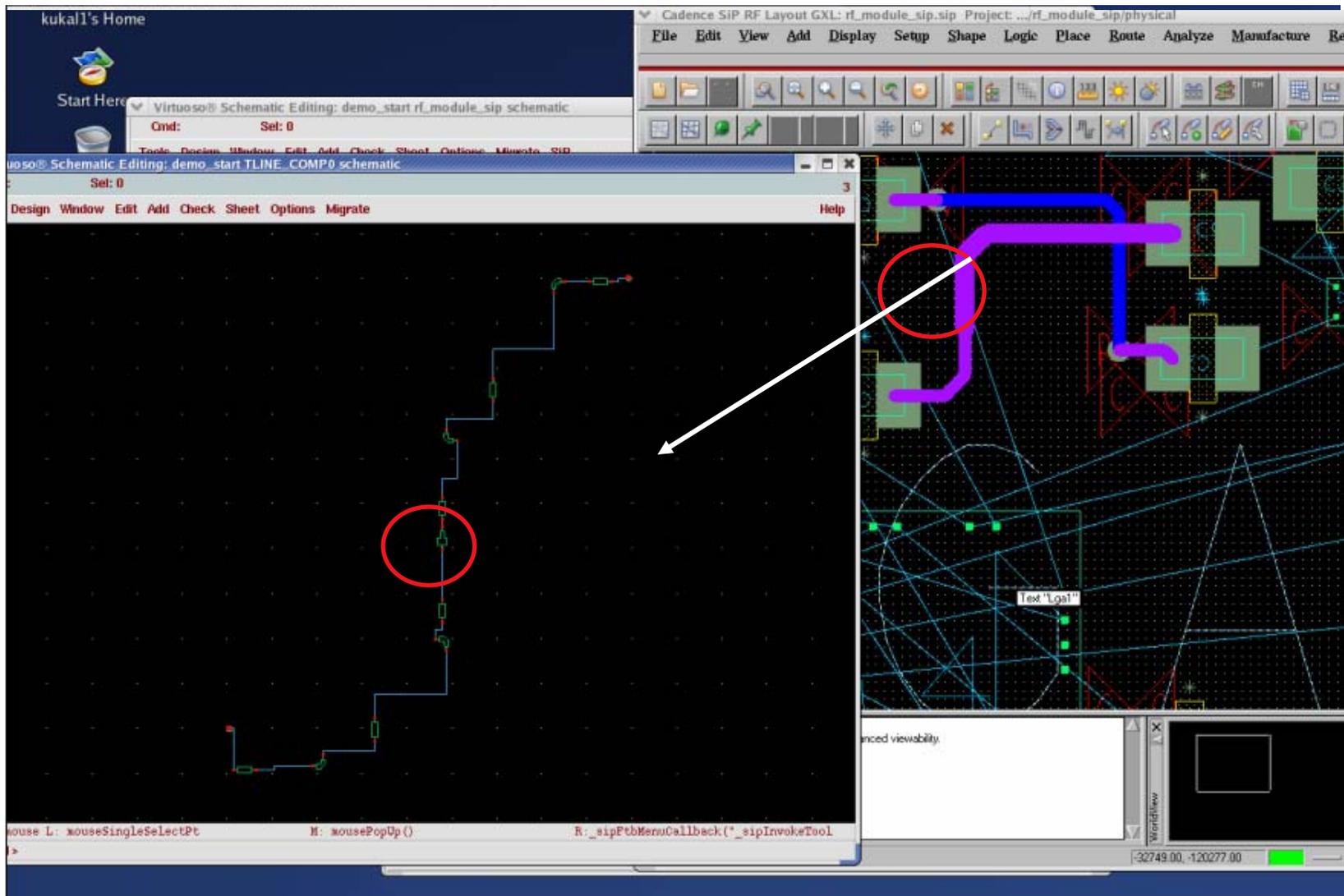
Property Name	Property Value	Property Type	Annotate	Description
W	200 microns	Physical	Yes	Width
L	600 microns	Physical	Yes	Length
N	2	Physical	Yes	Number of plate
F	1ghz	Electrical	Yes	Frequency
Temp	40	Simulation	No	Temperature
PCELL_VERSION	v1.0	Simulation	Yes	Version
APDLAYER1	COND_LAYER1	layer	No	Metallic Layer
APDLAYERDIE1	DIE_LAYER1	layer	No	Dielectric Layer
APDLAYER2	COND_LAYER2	layer	No	Metallic Layer
APDLAYERDIE2	DIE_LAYER2	layer	No	Dielectric Layer
APDLAYER3	COND_LAYER3	layer	No	Metallic Layer
APDLAYERDIE3	DIE_LAYER3	layer	No	Dielectric Layer
APDLAYER4	COND_LAYER4	layer	No	Metallic Layer
APDLAYERDIE4	DIE_LAYER4	layer	No	Dielectric Layer

Instance Property Viewer - Instance "I31"

Analyze Synthesize Technology file designUnits: MICRONS

Property Name	Property Value	Property Type	Annotate	Description
W	20u	Physical	Yes	Finger width
N	40	Physical	Yes	Number of fingers
G	20u	Physical	Yes	Spacing between...
L	100u	Physical	Yes	Length of overl...
IW	100 microns	Physical	Yes	Inter-connect W...
F	1ghz	Physical	Yes	Frequency
Rs	4	Physical	Yes	Resistance (ohms...
Temp	40	Simulation	No	Temperature
APDLAYER_A	TOP_COND	layer	No	Metallic Layer
APDLAYER_B	DIE1	layer	No	Dielectric Layer
PCELL_VERSION	v1.0	Simulation	Yes	Version

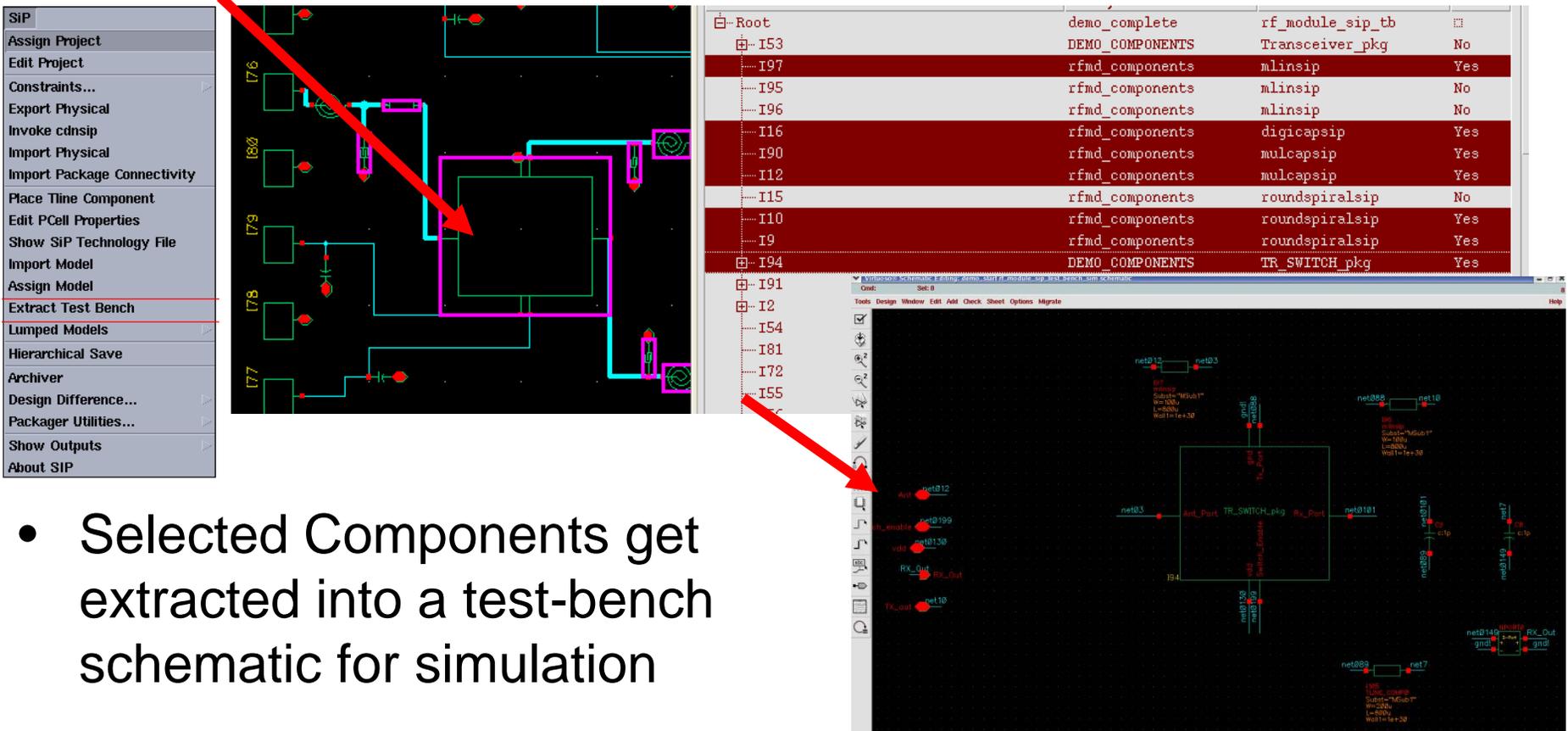
# Using Cadence RFSiP Solution - 1st order annotation through tline abutment



# Using Cadence RFSiP Solution

## - Critical portion of design extracted automatically

- Components selected by user for critical path simulation



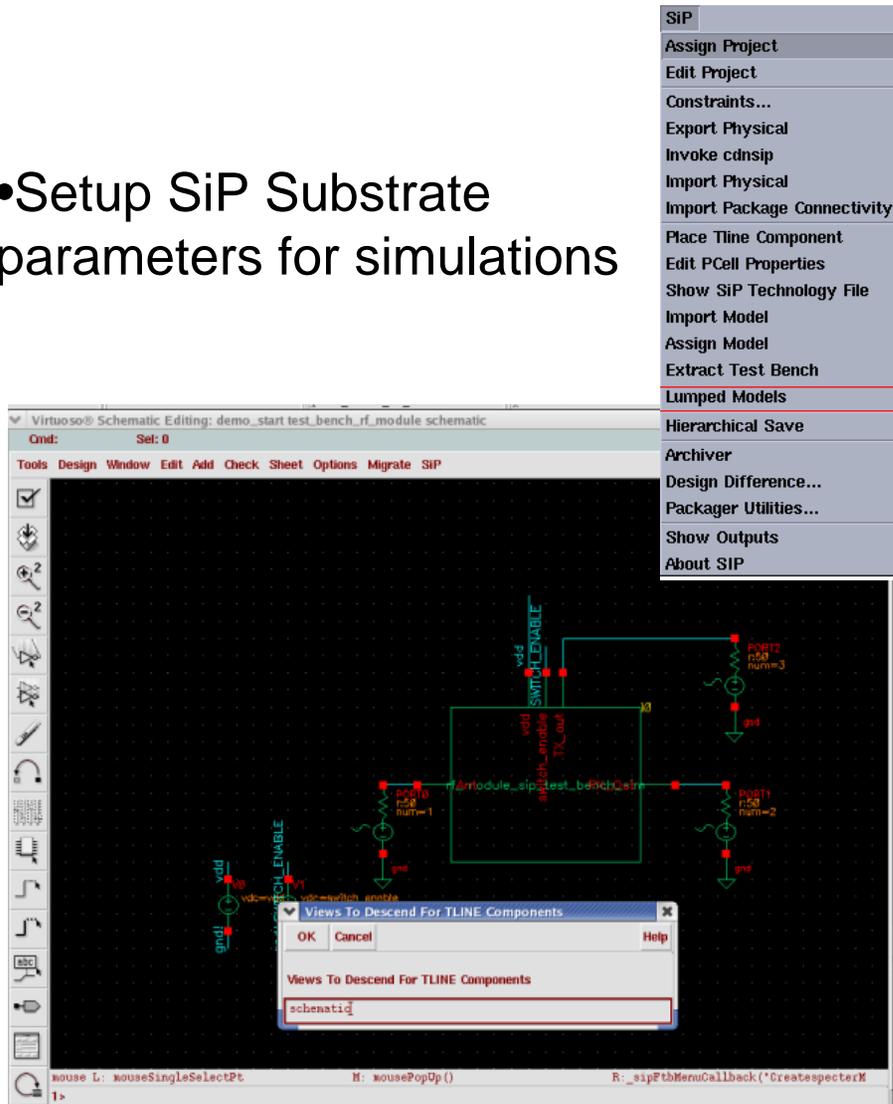
The image displays a multi-panel interface from the Cadence RFSiP solution. On the left is a menu with options like 'Assign Project', 'Edit Project', and 'Extract Test Bench'. The top-left panel shows a circuit schematic with a red arrow pointing to a specific component. The top-right panel is a table listing components and their properties. The bottom-right panel shows a test-bench schematic with a red arrow pointing to it from the table.

Component ID	Component Name	Component Type	Component Value
Root	demo_complete	rf_module_sip_tb	
I53	DEMO_COMPONENTS	Transceiver_pkg	No
I97	rfmd_components	mlnsip	Yes
I95	rfmd_components	mlnsip	No
I96	rfmd_components	mlnsip	No
I16	rfmd_components	digicapsip	Yes
I90	rfmd_components	mulcapsip	Yes
I12	rfmd_components	mulcapsip	Yes
I15	rfmd_components	roundspiralsip	No
I10	rfmd_components	roundspiralsip	Yes
I9	rfmd_components	roundspiralsip	Yes
I94	DEMO_COMPONENTS	TR_SWITCH_pkg	Yes

- Selected Components get extracted into a test-bench schematic for simulation

# Using Cadence RFSiP Solution - Simulating Design for trials and tuning

- Setup SiP Substrate parameters for simulations



Global Substrate Definitions

Global Frequency: 10GHz

Strip Lines	RF Stack	Signal Layer	Ground Plane 1	Ground Plane 2	Dielectric Constant	Dielectric Loss
	RFStrip_1	M2_S10	M1_S10	M3_S10	9.800000	0.0035
	RFStrip_2	M3_S10	M2_S10	M4_S10	9.800000	0.0035
	RFStrip_3	M4_S10	M3_S10	M5_S10	9.800000	0.0035
	RFStrip_4	M5_S10	M4_S10	M6_S10	9.800000	0.0035
	RFStrip_5	M6_S10	M5_S10	M7_S10	9.800000	0.0035
	RFStrip_6	M7_S10	M6_S10	M8_S10	9.800000	0.0035

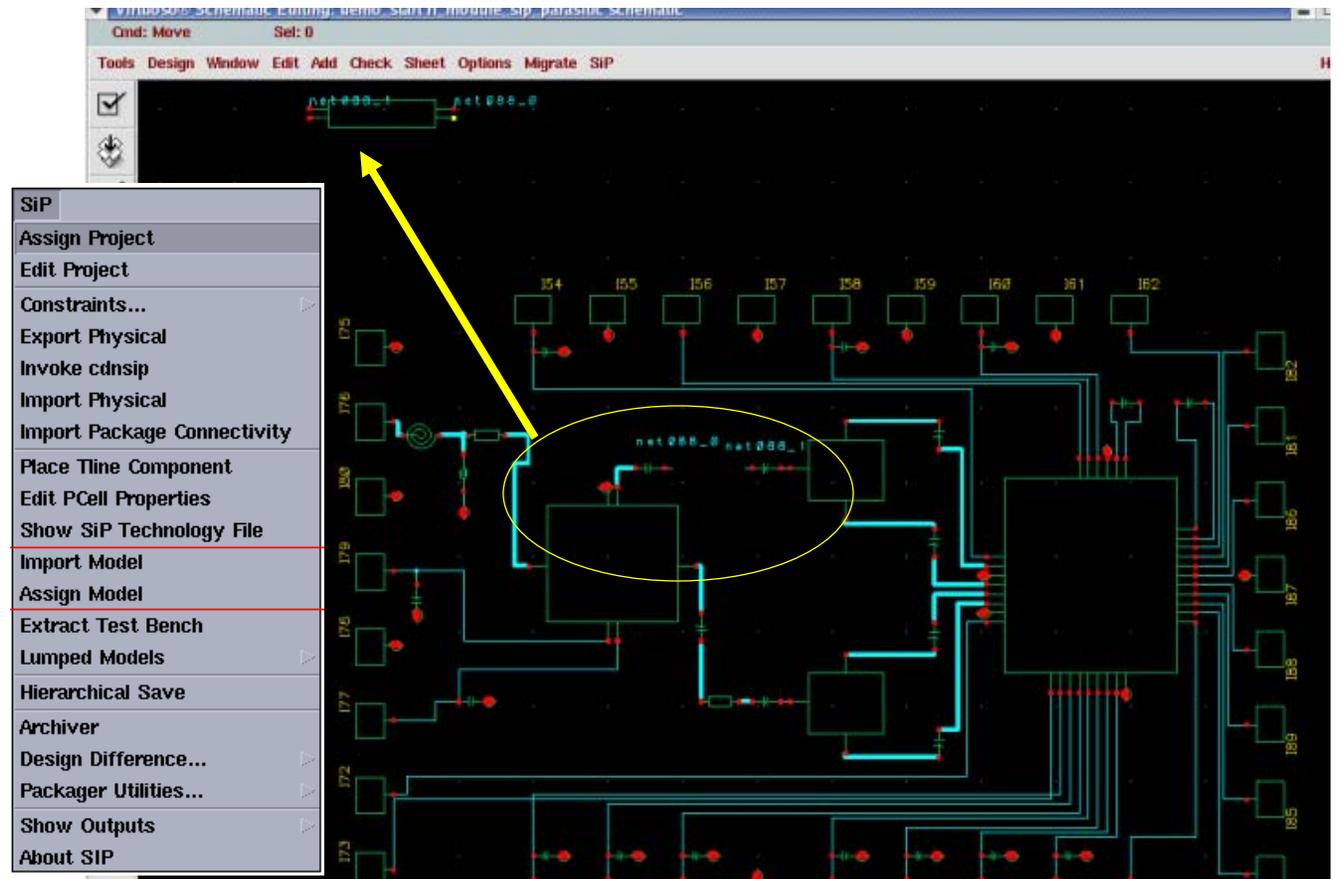
Micro Strip Lines	RF Stack	Signal Layer	Ground Plane 1	Dielectric Constant	Dielectric Loss
	RFMicroStrip_1	M1_S10	M2_S10	9.800000	0.0035
	RFMicroStrip_2	BOTTOM	M9_S10	9.800000	0.0035

Add MicroStrip Layer    Delete MicroStrip Layer

- Create lumped models for tlines and embedded passives
- Hook up stimuli
- Simulate with SpectreRF

# Using Cadence RFSiP Solution - Automatic Parasitic annotation to test-benches

- Import Model
  - Spice
  - S-parameter
- Assign Model
  - Single net
  - Coupled Nets
- Net(s) abutted and model inserted automatically



# Using Cadence RFSiP Solution

## - Verifying design post-layout: Xtor, HDL, tlines, s-param

The screenshot displays the Cadence RFSiP Solution interface. At the top, the 'Top Cell' section shows the current configuration: Library: wlanSipLib, Cell: FE\_Tx\_RX\_TB, View: schematic, with an 'Open' button. Below this are sections for 'Global Bindings' and 'Cell Bindings'.

**Global Bindings:**

- Library List: wlanSipLib wlanRficLib
- View List: spectre cmos\_sch cmos.sch spfile paksi schematic veriloga ahdl
- Stop List: spectre

**Cell Bindings Table:**

Library	Cell	View Found	View to Use	Inherited View List
wlanRficLib	pcm_pa_rec3	spectre		spectre cmos_sch cmos...
wlanRficLib	pcm_pa_rec4	spectre		spectre cmos_sch cmos...
wlanRficLib	pcm_pa_rec5	spectre		spectre cmos_sch cmos...
wlanRficLib	pcm_pa_rec6	spectre		spectre cmos_sch cmos...
wlanSipLib	B69812N2457A201	spfile		_sch cmos...
wlanSipLib	FE_Tx_RX_TB	schemati		_sch cmos...
wlanSipLib	LDB182G4510C-110	spfile		_sch cmos...
wlanSipLib	Matching_Net_Rx	spfile		_sch cmos...
wlanSipLib	Matching_Net_Tx	schemati		_sch cmos...
wlanSipLib	bw_lna_2	paksi		_sch cmos...
wlanSipLib	ind_pcell	schemati		_sch cmos...

A context menu is open over the 'FE\_Tx\_RX\_TB' row, showing options: 'Set Cell View' (selected), 'Explain...', 'Open...', 'Open (Read-Only)...', 'Add Stop Point', 'Remove Stop Point', 'Add BindToOpen...', and 'Remove BindToOpen...'. The 'Set Cell View' sub-menu is also open, listing available views: '<none>', 'ads', 'auCdl', 'auLvs', 'hspice\_models', 'ivpcell', 'layout', 'nport\_data', 'schematic', and 'spectre'.

**Messages:**

Use/reproduction/disclosure is subject to restriction set forth at FAR 1252.227-19 or its equivalent.

# Using Cadence RFSiP Solution - Simulating multi technology DIE(s)

DIE(s) with different technologies can be simulated without the need of changing model names

- Ability to mark blocks as MTS blocks
- Ability to set model files on a per block basis
- Ability to set MTS options (simulator specific) on a per block basis
- Works with Spectre, Ultrasim and AMS simulators

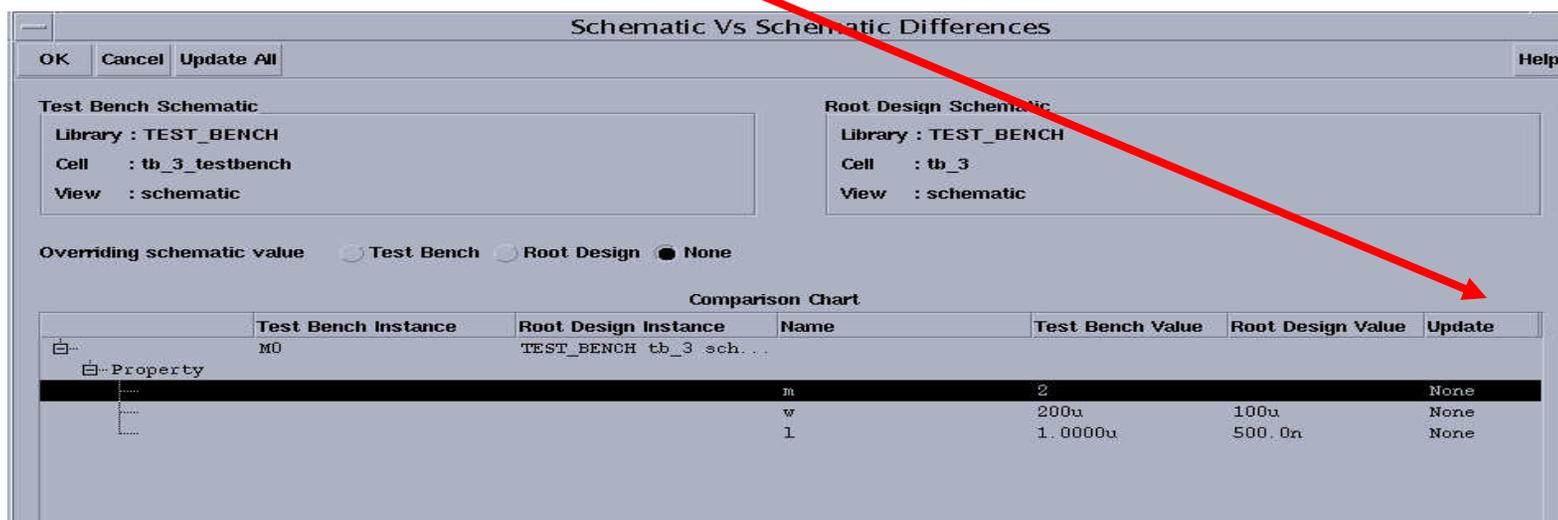
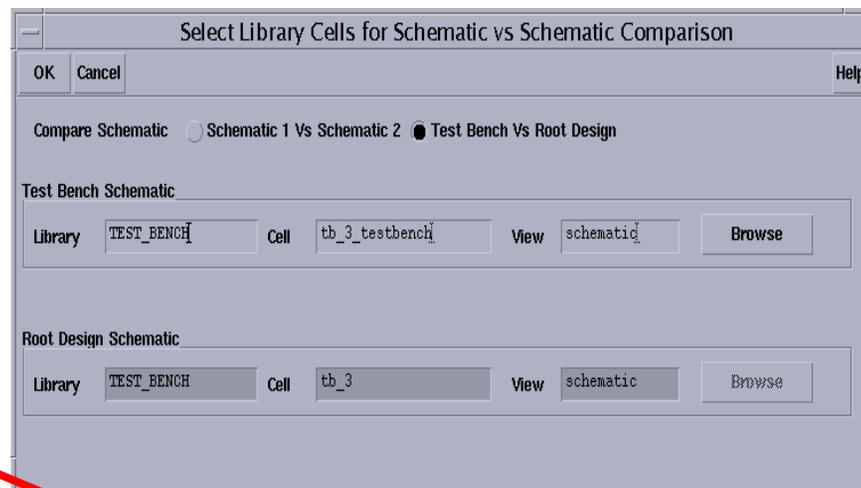
The image displays three overlapping screenshots from the Cadence Virtuoso Analog Design Environment. The top-left screenshot shows the 'Tests and Analyses' window with a context menu open, highlighting 'MTS Options...'. The top-right screenshot shows the 'Multi-Technology Mode' dialog box with the 'Multi-Technology Mode' checkbox checked. The bottom screenshot shows the 'MTS Options' dialog box with the 'Cell Table' tab selected, displaying a table of MTS blocks.

Library	Cell	MTS_BLOCK	modelFiles	tnom	scalem	scale
solutions	TEST	<input type="checkbox"/>				
solutions	ampTest	<input type="checkbox"/>				
solutions	amplifier	<input type="checkbox"/>				
solutions	supply	<input type="checkbox"/>				
test	blockA	<input checked="" type="checkbox"/>		30		
test	blockB	<input checked="" type="checkbox"/>		25		
test	temp_depend...	<input type="checkbox"/>				

# Using Cadence RFSiP Solution

## - Updating Master design from testbench

- Extracted Schematic can be compared against Master Schematic
- Either schematic can be updated with changes





# Using Cadence RFSiP Solution

## - Summary

- The Cadence RF SiP flow eliminates the need for:
  - Capturing designs twice for purposes of simulation and SiP implementation
  - Creating separate testbench designs for analysis and simulations, followed by manual sync-ups with the master design
  - Manual insertion of parasitic models (obtained from third-party sources) into the testbench design
  - Manual renaming of models for different dies that are on different technology nodes
  - Explicit export of layout structures to third-party solvers for extraction



# Using Cadence RFSiP Solution - Summary

- The Cadence RF SiP flow promotes:
  - Single front-end driven simulation and implementation covering both
    - IC layout
    - SiP layout
  - Easy analysis of Embedded passives with physical parameters
  - Pre-layout simulations with 1<sup>st</sup> order simulations that are fast and allow rapid exploration
  - Post-layout verification with multitude of DIE technologies and package parasitics
  - Use of integrated solvers for 3-D structures and RF Shapes



# Agenda

- Introduction to RFSiP
- Complexity in RFSiP simulations
- Traditional approach used at IFX for simulation of RFSiP
- Using RFSiP for accelerating simulations at various stages of design
- **Conclusions**

# Conclusion

- RFSiP 15.7 design flow used at Infineon for productive designs.  
The following features are mainly used:
  - Schematic entry
  - Automated link between Composer and Allegro CDNSiPProductivity gain of 2-3 man weeks for a RF-SiP design (Example 1) in comparison to old Excel style
  
- Some RFSiP 16.0 features specified together with Cadence:
  - Parasitic model import
  - Automated model backannotation
  - Automated testbench generation (“critical parts”)Expected productivity gain due to faster loops between design and simulation steps and decreased number of manual errors.
  
- RFSiP 16.0 will be offered for productive designs in Infineon’s next internal chip/package codesign flow release.
  
- Infineon would like to see “one common” SiP flow solution rather than a split between RFSiP and digital-SiP (SCM, IOP):
  - Support of SCM or Composer for connectivity entry independent of type of top-level die design (analog or digital)
  - One common IO-Planner for both digital and analog designs based on OA database.



cadence designer network

A cluster of overlapping speech bubbles in various colors (orange, green, yellow, blue) is positioned behind the main title text.

# CONNECT: IDEAS

**CDNLive! 2007 Silicon Valley**