CDNLive, Munich, 2007

Experience with using Cadence SPB 15.7 tools for advanced SiP designs

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May 15, 2007

Plan:

1- Introduction: what is a SIP within NXP?

2- NXP needs for SIP design

3- Our experience with Cadence SPB 15.7

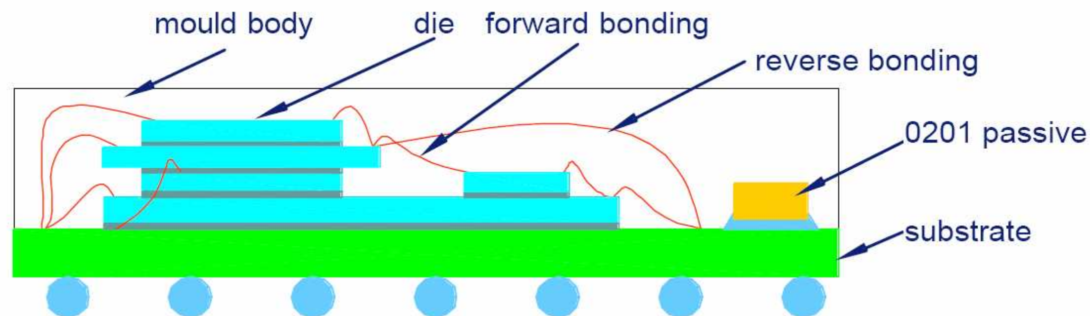
4- Summary

5- Conclusions

1- Introduction: what is a SIP within NXP?

Any package containing multiple die, passive components or both

Includes MCM, RF module, stacked die, SoP, PoP, …



Relevance of SiP within NXP semiconductors:

- SiP volume has been largely increasing over past years
- Many application areas and BL's involved
- Impact on design technology is huge

1- Introduction: Current SIP design flow need improvements

Motivation for development of NXP SIP DE:

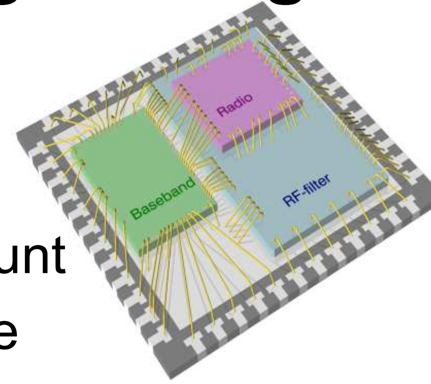
- **No standard way of working and/or design tools**
- **No SiP centered design methodology**
- **Package and IC design are different worlds**

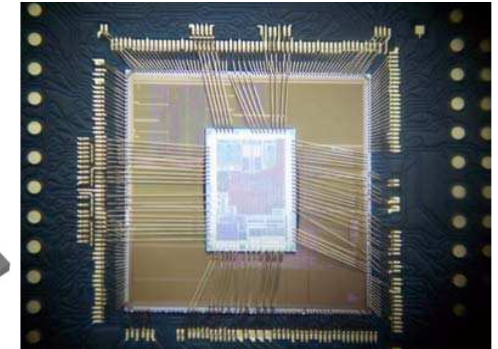
- **Current SIP design methodology and flow need to be improved**

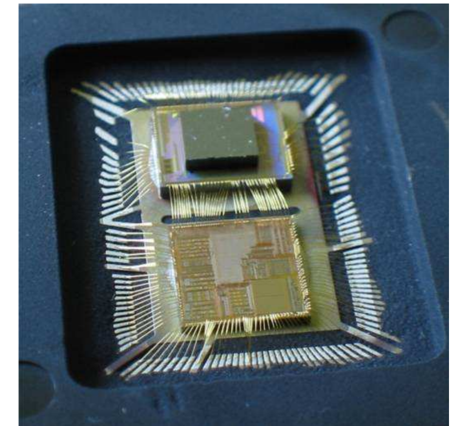
1- Introduction: SiP DE target designs

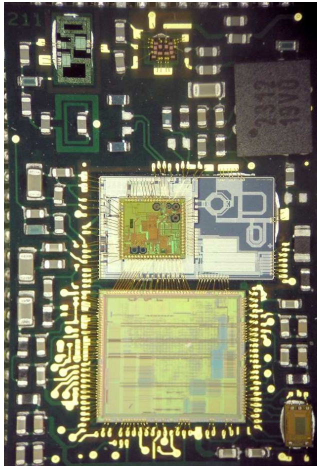
Complex system SiP's:

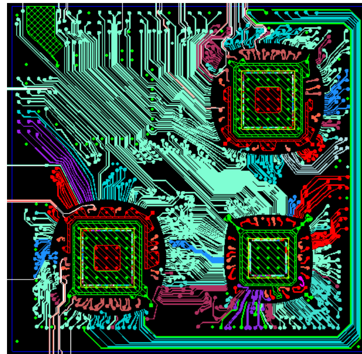
- Laminate substrates
- Integrating parts/IC's with high IO count
- High-complexity interconnect scheme
- Requiring IC-package co-design
- Requiring careful interconnect analysis

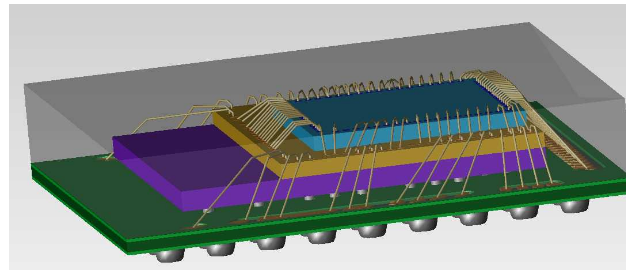


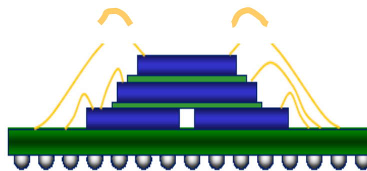


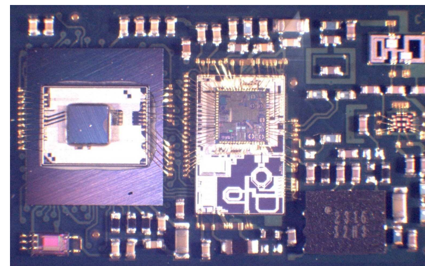


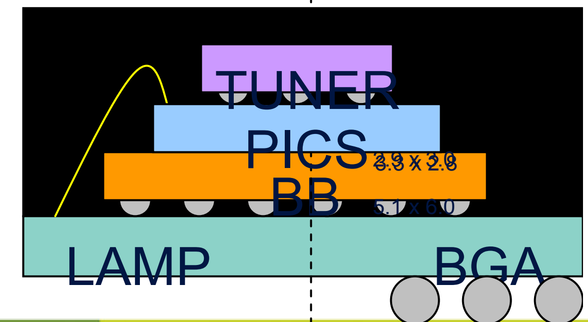












2- NXP needs for SIP design: generic task overview

IC package co-design

Create and import BMs for IC parts

Packaging and Assembly Design Kit implementation

IC part import

Schematic/logic capture

Layout design

Physical layout verification

Export manufacturing data

Baseline SiP DE

SiP circuit simulation and electrical verification

Interconnect model extraction

SiP electrical analysis & verification

Point tool analysis:
- Thermal
- Mechanical
- Reliability

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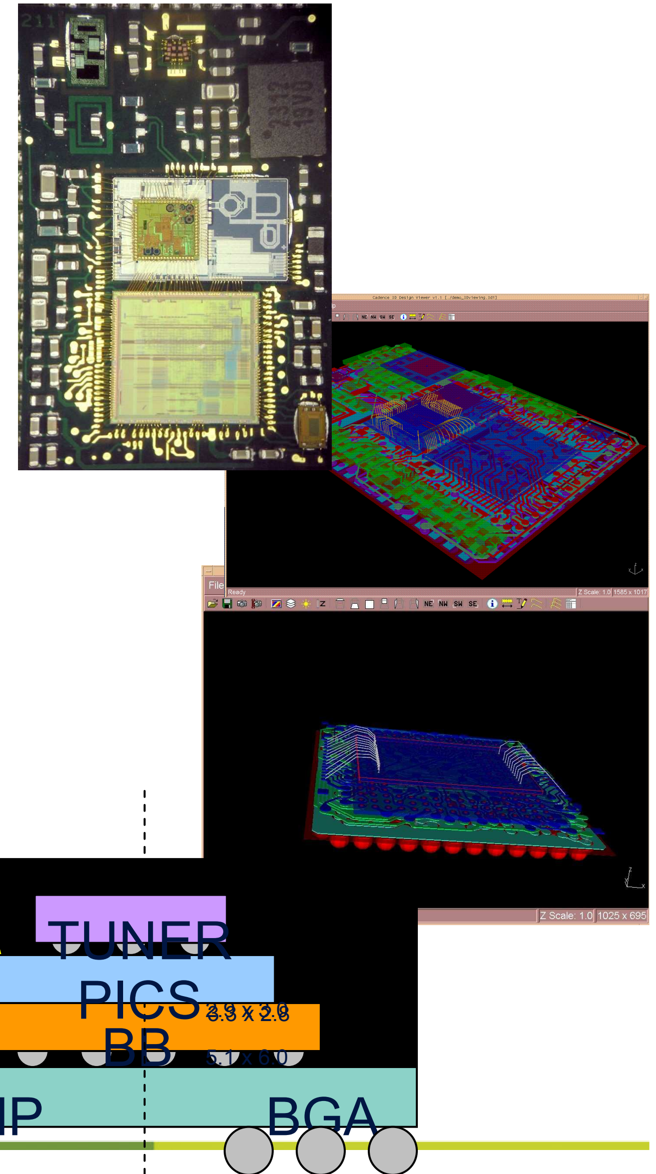
On-going

2- NXP needs for SIP design:

Cadence SPB 15.7 functionalities were tested by creating a complete design databases of:

- SIP1
  - Complex system module: 50 SMDs and 6 dies (BiCMOS, passive silicon technology, CMOS, etc..), on a 4 layers BGA laminate.
  - Wirebonded ICs only
- SIP2
  - 3 dies (CMOS, passive silicon technology, BiCMOS) stacked on a 4 layers LGA laminate
  - Flip-chipped and Wirebonded DIEs
  - IC-package co-design
- SIP products which requires:
  - **IC-package co-design,**
  - **RF and Digital ICs**,



3- Features offered by Cadence SPB tools

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3- Features offered by Cadence SPB tools

Packaging and Assembly Design Kit implementation

Technology related information delivered into a single repository with:
- laminate stack information,
- LGA/BGA physical symbols,
- SMD footprints,
- Vias, bondfingers
- Substrate DRs
- Most of the assembly DRs

Easy import

Physical design (CDNSIP tool)

Cadence SPB is meeting most of our needs

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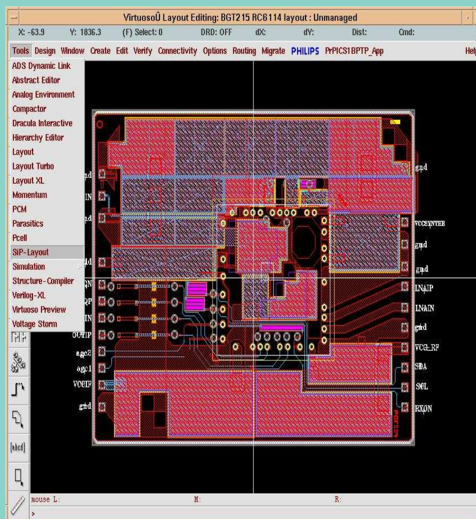
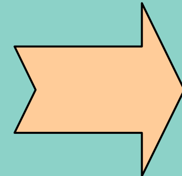
3- Features offered by Cadence SPB tools

IC part Import

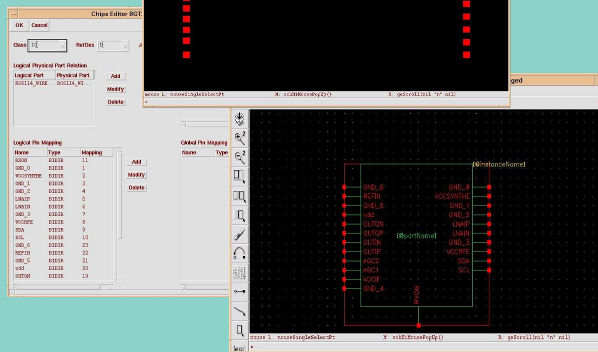
Import the IC views for physical design through 3 different ways:
- Virtuoso IC database
- LEF/DEF files and OA database
- ASCII file



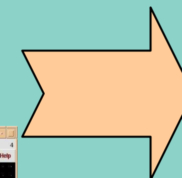


chips view

footprint



symbol



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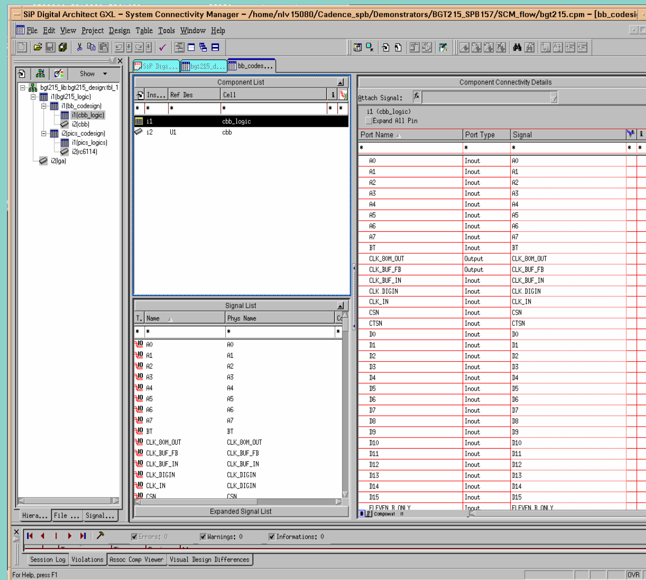
3- Features offered by Cadence SPB tools

Schematic or logic capture

Digital or RF ?

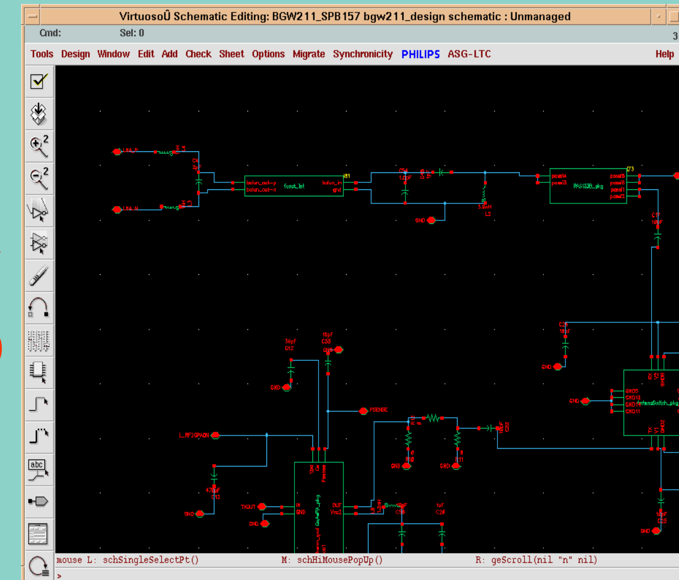
Allow to build up:
- The database of the components
- Make the connectivity



SCM

OR

AND



Virtuoso Composer

NXP expects 1 single flow

3- Features offered by Cadence SPB tools

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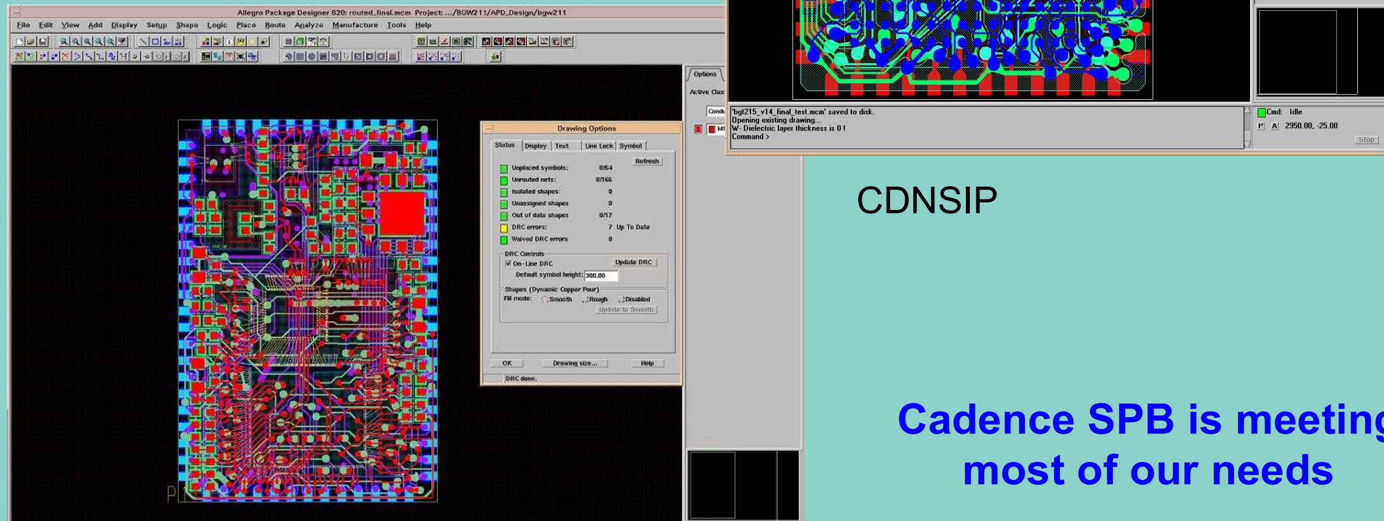
3- Features offered by Cadence SPB tools

Layout design

Advanced functionalities for physical design:
- Component placement / floorplan
- DIE stack settings
- Routing on laminate substrate
- Wirebonding …



CDNSIP

Cadence SPB is meeting most of our needs

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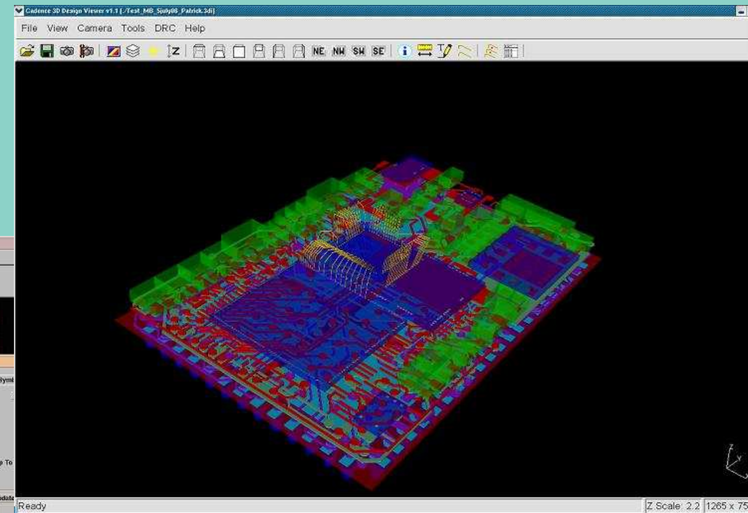
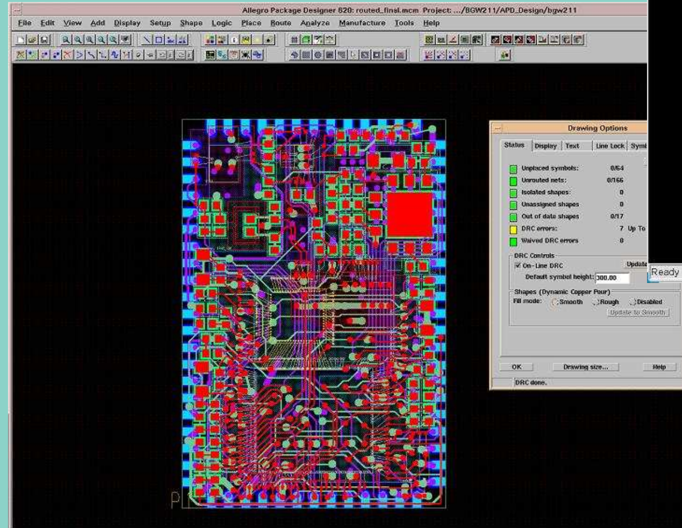
3- Features offered by Cadence SPB tools

Physical layout verification

Physical design verification:
- 3D assembly DRC
- 2D assembly and laminate DRC
- 3D viewer

Fully routed design with 2D and 3D DR checks in CDNSIP





Cadence SPB is meeting most of our needs

NXP expects a single DR database (2D+3D, substrate + assembly)

3- Features offered by Cadence SPB tools

IC package co-design

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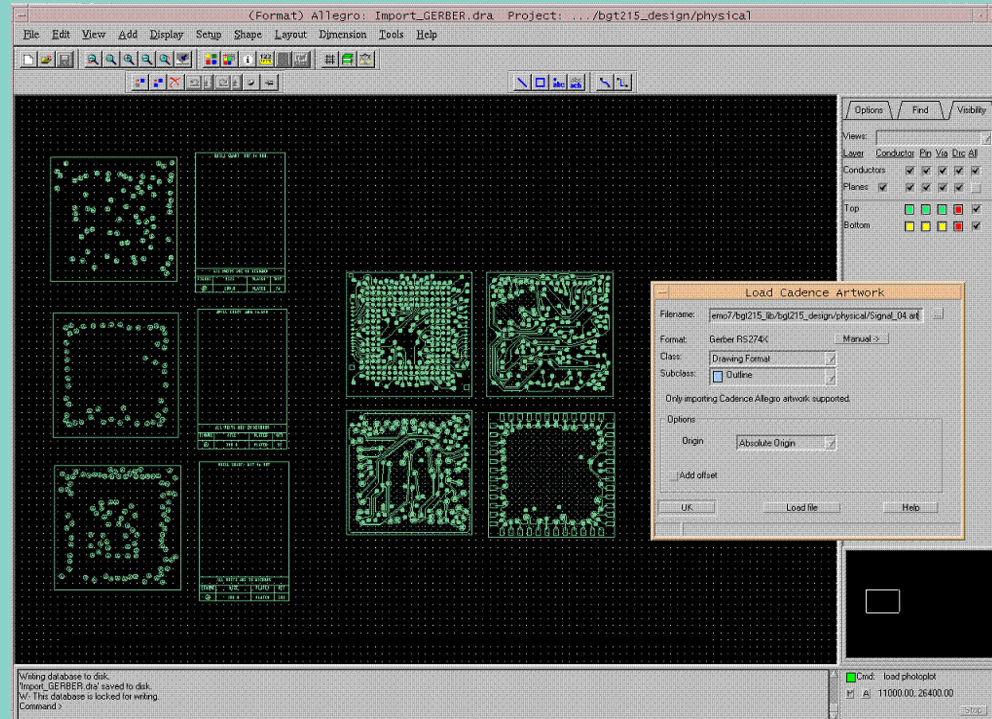
3- Features offered by Cadence SPB tools

Export manufacturing data

Different format and possibilities to export data for manufacturing:
- DxF, gerber, gds2…
- Drill file, bill of materials
- Customized Report, …



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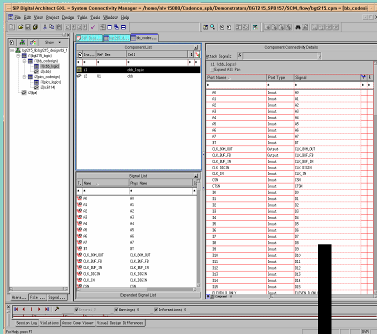
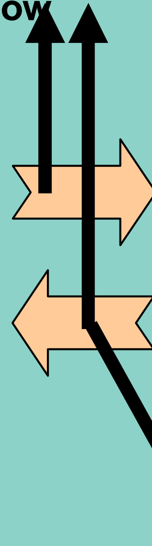
3- Features offered by Cadence SPB tools

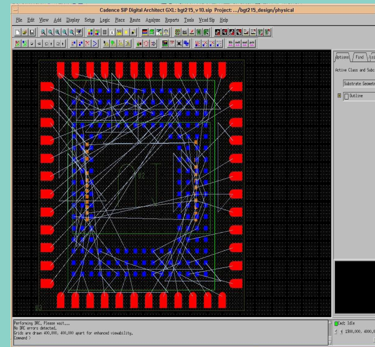
IC package co-design (1)

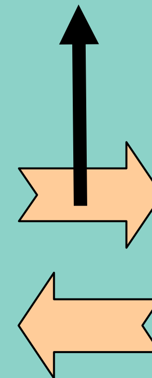
- Swapping bumps is causing troubles in the flow

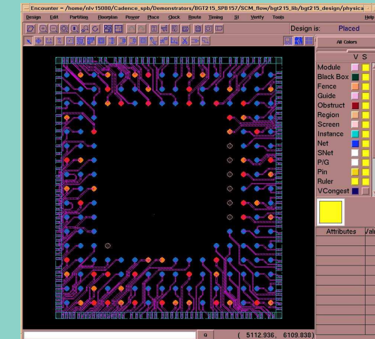
- Not fully automated links: IO file has to be manually edited











SCM

CDNSIP

Encounter I/O planner

- The front end tool can't edit the IC connectivity
- Power / ground PINS are not correctly handled by the flow

- Synchronization issue when adding deleting/pins in CDNSIP

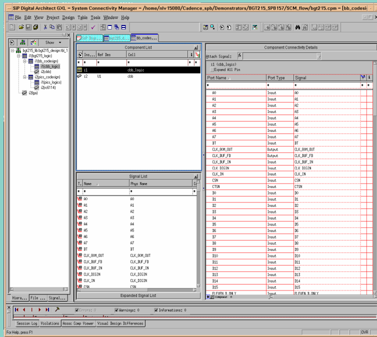
IC-package co-design not mature yet: Too many braking points in the flow

3- Features offered by Cadence SPB tools

IC package co-design (2)

- With the latest technologies, Digital IC design becomes more complicated.

- We see limitations in First Encounter, specially with respect to IO ring creation.



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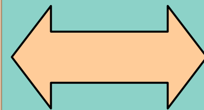
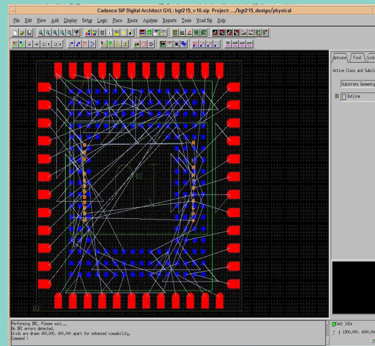
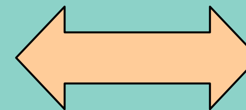
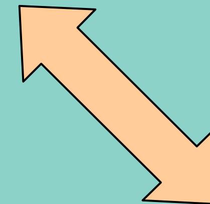


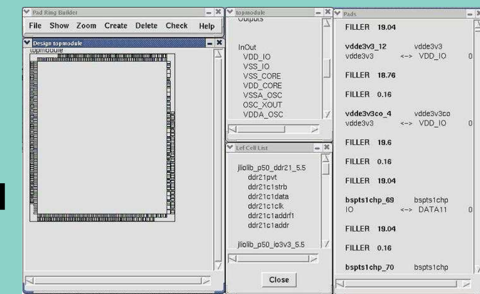


CDNSIP



Encounter I/O planner





In-house tool

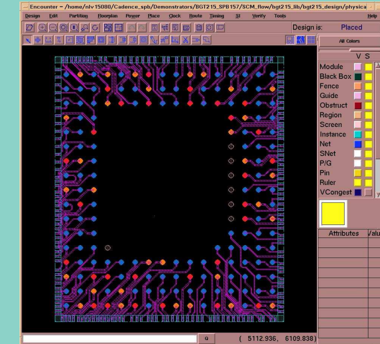
- Facilities for IO cell placement and IO ring creation
- Easy way to modify the netlist
- Complete IC DRs checks,
- SSO and ESD checking

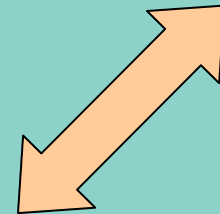
3- Features offered by Cadence SPB tools

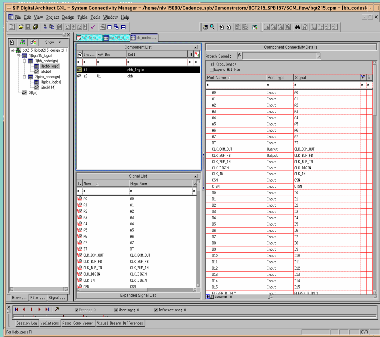
IC package co-design (3)

Need also to co-design RF ICs coming from Virtuoso layout.

Encounter I/O planner







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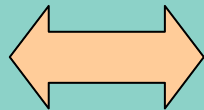
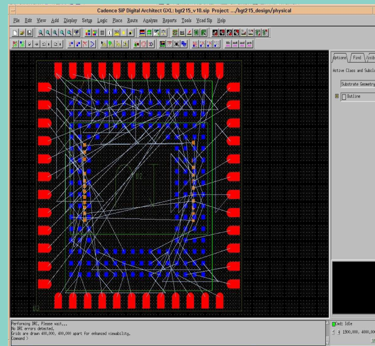
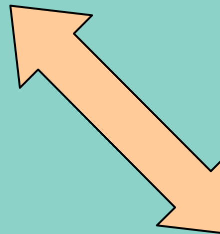
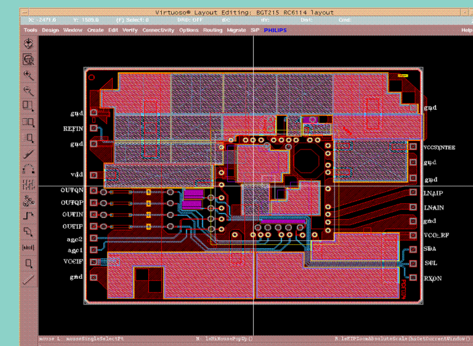




CDNSIP



Virtuoso IC



IC-package co-design with other tools would bring added value

4- Summary

TAKS	NXP opinion	Comments
IC part Import	++	
Packaging and Assembly Design Kit implementation	++	
Export manufacturing data	++	
Physical layout verification	+	DRs databases should be merged
Layout design	+	Performances recently improved (wirebonding)
Schematic or logic capture	0	2 separate flows are co-existing: NXP need a merged / unified flow
IC package co-design	-	IC-package co-design is not mature yet

5- Conclusions

- Cadence SPB 15.7 is a good starting point for our NXP SIP DE.

- To successfully deploy Cadence SPB and enhance SiP design productivity within NXP, we need improvement and enhancement of the tools:

  - In IC-package co-design.
    Cadence SPB is a good starting that can be enhanced to create real added value.

  - In logic capture.
    A merged and unified (schematic and spreadsheet based) logic capture tool is of essential importance.

6- Acknowledgement

- To members of NXP SIP DE project team:
  - Pieter Oude Egberink
  - Stefan Lukanovski
  - Saoer Sinaga
  - Jesse Li
  - Sidina Wayne
  - Gene Felten

- To Cadence Vcad team:
  - Martin Biehl
  - Janez Jaklic
  - Heiko Dudek