TECHNICAL PAPER

cadence®

DIGITAL HIGH-SPEED PACKAGING DESIGN AND VERIFICATION

UTILIZING A FLOW-BASED APPROACH TO COUNTER DIGITAL PACKAGE DESIGN CHALLENGES

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1 OVERVIEW

This paper provides a high-level overview of Cadence Design System's view on a flow-based methodology to design digital high-speed packages. This will be done by first outlining the challenges that digital packages present to design teams and manufacturing groups and then by identifying what we believe is the best-in-class flow for facing these issues head on. For the purposes of this paper, it is assumed that this is a single die on a ball grid array (BGA) package. The majority of this flow can be, and has been, adopted for multichip modules (MCMs) as well. Only the single die is addressed in order to simplify the flow examples given.

With ever-increasing performance demands on electronic products, all areas of design and manufacturing must be exploited for maximum electrical performance at minimal cost. In order to meet these cost and performance goals, exploration of the desired results must be done as far in advance as possible. If electrical performance issues are discovered too late in the design cycle, it can result in costly re-spins that will not only waste engineering dollars, but also delay critical time-to-market goals. Issues such as this can, and have, resulted in failed projects. If a design does go to completion and meets electrical performance goals, yet fails to meet cost expectations, this too can quickly doom a project to failure. All aspects of a project's cost and performance goals must be met in order for the project to be a success.

In order to ensure that all goals of a project are met, early exploration of cost and electrical performance must be part of your design methodology. In addition, concurrent design can be leveraged substantially to reduce design cycle times and time to market. The key to this is having the information available in a characterized flow. Key data must be present for the next step in the cycle to commence, and as the next step begins, that data must be portable in order to leverage further checks and validations. With a concurrent methodical flow, utilizing best-in-class CAD tools, maximum performance and profit can be extracted from your designs.

2 HOW DO YOU GET THERE FROM HERE?

We believe that by adopting a concurrent characterized flow, the aforementioned issues can be handled in a repeatable and reliable fashion. *Figure 1* outlines the high-level view of this flow. The flow commences with initial input. This is when initial project data is collected, including cost targets, performance requirements, form, fit, and function goals. Some level of definition of these elements is desired before the next phase.

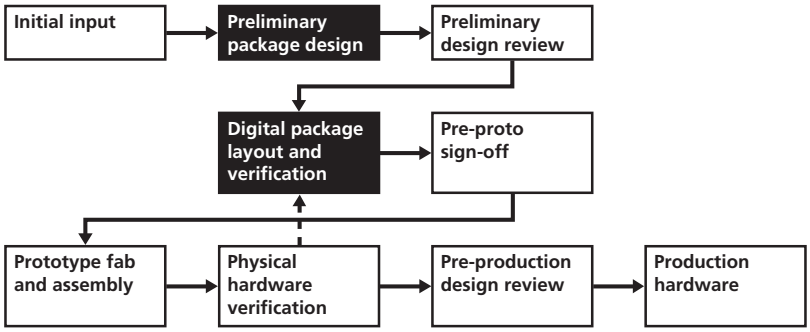

Figure 1: Overall process flow

The next phase, preliminary package design, is when the target data pushes into the commencement of actual design. *Figure 2* shows the preliminary package design phase in greater detail.

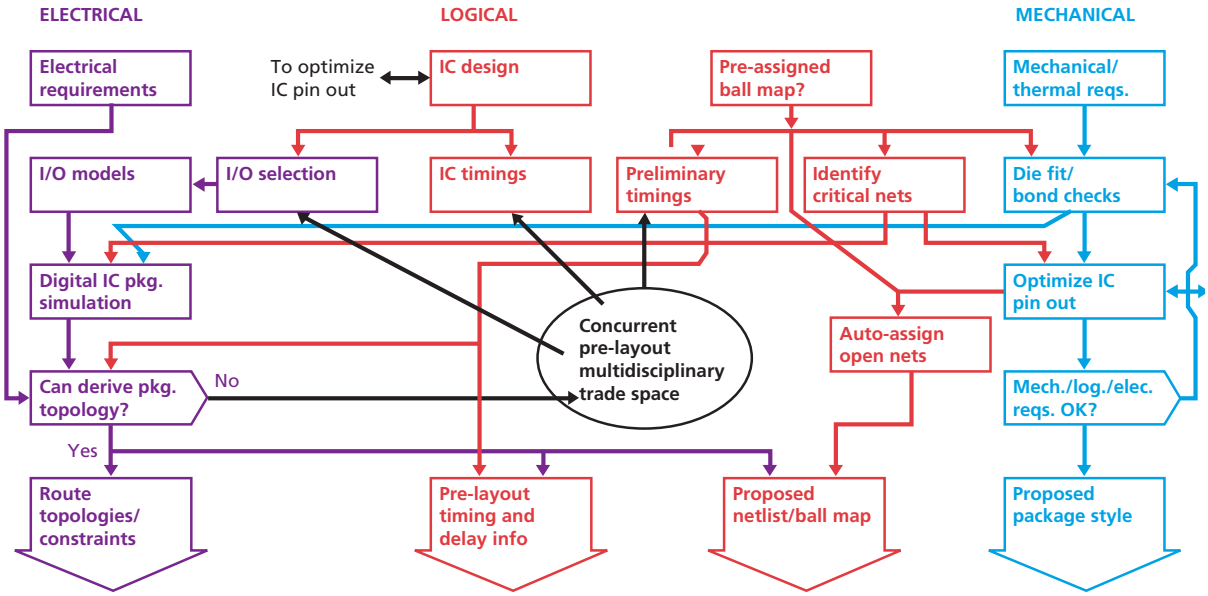

Figure 2: Preliminary package design sub-process

During the preliminary package design sub-process, data gathered from initial input is utilized to start the design process. There are three different aspects of this phase.

- The electrical area derives the performance aspects required of the package (shown in purple). Some important steps in this process include identification of I/O models for driver simulation, verification that performance requirements can be met on the lowest cost package, and validation that the I/O drivers on the IC are not over- or under-powering the signal.
- The logical area derives the performance aspects of signal behavior within the package (shown in red). Some aspects of this step include validation that timing goals can be met on the package, verification that adequate power/ground goals can be met, and determination of the ball assignment for the BGA (if the BGA is not pre-assigned).
- The mechanical area investigates the physical aspects of the package (shown in blue). Some of the more important aspects of this include ensuring that the die will fit on the BGA, verifying that wirebonds can be bonded out based on the die pin placement, if the design is wirebond, or verifying that the die pin array can be escaped to appropriate routing layers if the design is a flip-chip.

These three steps create what we call the concurrent pre-layout multidisciplinary trade space. These steps are not independent—concurrent pieces of information from each step are needed by the other steps in order to validate and create the necessary data for the next step to commence. The data goals for this process are shown on the bottom row of *Figure 2*. Once the data for route topologies, timing, netlist and package style is determined, the design is ready for the next step—preliminary design review (see *Figure 1*).

Once the preliminary design review is completed, the design can proceed to the digital package layout and verification phase (see *Figure 3*). This process takes the data from the preliminary package design sub-process in electronic form and builds upon that data to perform the detailed physical design of the package. Having the data conveyed to this process in electronic form ensures that the agreed-upon design intent set forth in the preceding steps is embedded effortlessly into the package database. This phase has four primary areas of action—preliminary, electrical verify, route, and verify/cleanup. These steps occur in a fairly linear fashion following the flow outlined below with validation steps and action loops as shown.

It is important to note that at various steps in the process, the design data can be validated to ensure that it meets the electrical performance goal set forth in the earlier phases of the flow. At this phase in the process, package models, package pin delay reports, and physical pin layout (footprint) information can be generated. This data can be used by the PCB teams to validate data in process or as a starting point for electrical analysis. This data can also be used as the backbone of a design kit, a collection of electrical data that can be used by downstream customers to leverage the design within other products. In some cases this electrical verification is not necessary, based on relaxed design requirements, but we find this to be an increasingly rare occurrence.

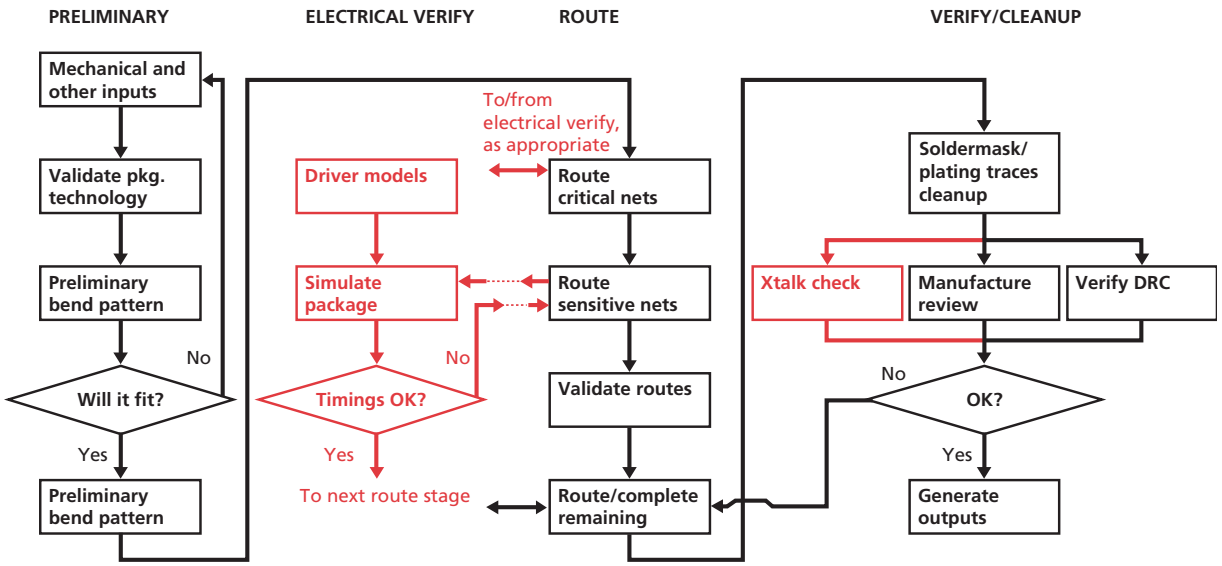

Figure 3: Digital package layout and verification sub-process

Once the design has been cycled through the process to the point that outputs can be generated, it is ready to proceed to the next phase of the process. As the design proceeds through the flow, there are opportunities to re-enter the digital package layout and verification phase if issues with manufacturing occur. But with a thorough review of the data at the pre-production design review phase by qualified manufacturing team members, we find this impact to be minimal. The goal of the flow is to circumvent issues before the design moves too far down the cycle, and we feel that with adequate oversight and review in the phases outlined, this is avoidable.

3 CONCLUSION

With a trained team of physical designers, signal integrity engineers, and manufacturing engineers, this is a repeatable and reliable flow for the design of digital high-speed packages. The flow is broken into two sub-processes shown in *Figures 2* and *3*. These sub-processes ensure that the data is qualified before it moves through the next gate. There are checks and data handoffs at quantifiable points in the process and these can be used to synchronize the injection of data into the design at the correct time. This flow is being used by many corporations and has yielded significant improvements, not only in electrical performance, but also in cost performance.

The Cadence Design Systems Services group has a mechanism in place to measure your process against those considered to be best-in-class. If you would like our Services group to engage with you and help to measure your process and suggest areas or means of improvement, please contact Alan Porter at aporter@cadence.com or 800.340.0774.

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