# cādence°

### Cadence 3D Design Viewer

Visualize, debug, and verify complex IC packages

Cadence<sup>®</sup> 3D Design Viewer is a full, solid model 3D viewer and 3D wirebond design rule checking (DRC) solution for complex IC package designs that is tightly integrated and included with Cadence SiP Layout. It is also available separately to be used standalone or tightly integrated with Allegro<sup>®</sup> Package Designer (APD). It allows users to visualize, investigate, and wirebond DRC check an entire design, or selected design subset, reducing design cycle time and improving product manufacturability.

#### An Intelligent 3D Design View

Virtually all of today's EDA tools that perform physical layout—IC, IC package, or PCB—are two-dimensional. While 2D may work fine for substrate layout, interconnect planning, or metal fill creation, this "plane-view" does not lend itself well to the design, management, and verification of multi-tier wirebond die or stacked-die designs. The design complexity and density involved require a more realistic three dimensional approach.

The Cadence 3D Design Viewer meets this need by providing an IC package designer with the capability to physically visualize a design as it will actually look during manufacture. A designer can interactively zoom, pan, and rotate the 3D view as well as select from a set of predefined views from fixed orientations such as top, bottom, or northeast corner.

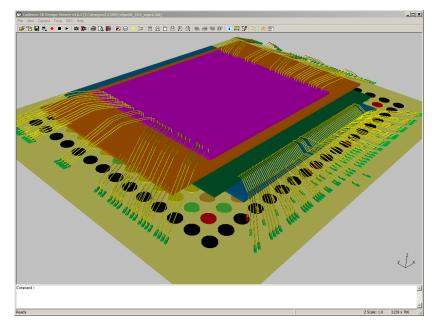


Figure 1: Cadence 3D Design Viewer lets users visualize the same design as it will actually appear

## Embedded with IC Package Layout

The 3D Design Viewer is included with SiP Layout, but when acquired as a standalone product, can be accessed from the APD user interface. When invoking the "3D View" the designer has the opportunity to modify the settings for package ball dimensions, colors and multiple wire profiles (npoint models) as well as select multiple 3D wirebond DRC rules. The design data compiled by APD and provided as input to the 3D viewer is saved and can be shared with others using the standalone Cadence 3D Design Viewer, such as manufacturing engineers.

The benefits of working with the third dimension are clear when the same design is viewed in 2D and then in 3D. For demonstration purposes a stacked die design using four die on ball grid array (BGA) substrate is used. The base die is flip-chip attached; the top three die are wirebond attached. In the 2D editor view (Figure 2), visualizing and validating the die stack and the wirebond ring is challenging, even for a seasoned package designer. And, due to the complexity, it would be almost impossible to hold a design review with an architect or lead engineer. When the same design is loaded into the 3D Design Viewer (Figure 1) the designer and the engineering team can not only easily visualize, investigate, and create collaborative. markups but they can also perform detailed 3D wirebond checking, including the ability to define, modify, and assign new wirebond profiles.

#### Easy Design Investigation

Cross referencing is easy as the 3D Design Viewer uses the same color/layer/object settings as defined in Allegro Package Designer. Layer visualization can be turned on/off and layer transparency set. For detailed design investigation, the 3D Viewer has similar "show element" information command capability that can be used by "object" or by "net." Importantly, the user has control over the highlight color and the level of transparency applied to none selected objects.

The 3D Viewer is especially effective when trying to understand and visualize complex via arrays, especially on designs using build-up layers. Figure 3 illustrates how difficult it is to understand the connectivity path of high density

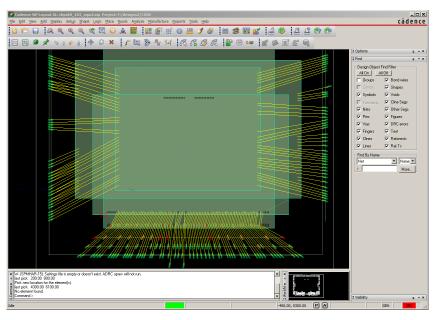


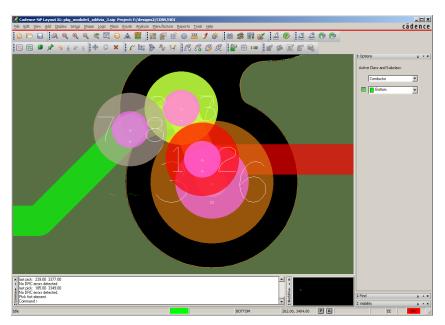
Figure 2: A multi-die stack on a BGA substrate viewed in 2D

interconnect (HDI) from a top package substrate layer to a bottom layer viewed in 2D.

Contrast this figure with the 3D view of the same HDI. The designer can easily visualize the interconnect path from the top to the bottom layer.

#### **Advanced Features**

When preparing for 3D viewing in SiP Layout or APD, it may be desirable to focus on a sub-section of the package. For this reason, the user is offered the option of taking a section of the package and viewing that piece in the 3D viewer.



*Figure 3: It is difficult to understand the connectivity path between the metal interconnect as it transitions between layers in 2D* 

This can be particularly useful in design reviews where a section of the design is being examined. (See Figure 5).

Another useful feature is the ability to append multiple designs within one single 3D view. This is commonly used with Package-on-Package (PoP) designs or in cases where a multiple routing substrates are used within a single package.

#### **Interactive Markup**

During 3D design viewing an engineer can create "markup" jpeg snapshots for design reviews and/or design documentation that include the ability to add basic shapes, arrows and text. This is especially useful for communications with the design chain partners and test and assembly manufacturing departments.

#### 3D Wirebond Clearance Design Rule Checking

Stacked die or multi-tier single die designs with dense wirebond patterns run the risk of manufacturing issues where wires may touch each other. In order to maximize yield, manufacturing engineers require adequate spacing between wires. Otherwise wire sweep and sway may cause a short during the molding process. The 3D Design Viewer provides the functionality needed to validate these spacing requirements. Because the 3D Design Viewer leverages wire curvature information provided by wire bonding equipment providers as well as detailed height information in the design die stack, design rule checking can provide very accurate spacing checks.

The rules are defined and stored as part of the Allegro Package Designer design session. Completely user-defined, they can be used to check wire to wire and wire to die interference checks.

Figure 6 shows how the 3D Viewer enhances the designers debug capability—the "info" command highlights the DRC marker and the associated wirebonds as well as indicating the rule, rule value, and actual value.

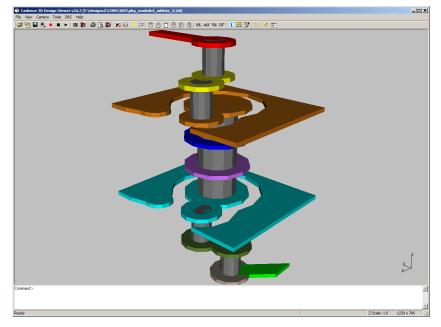


Figure 4: In a 3D view the designer can precisely visualize the transitions in and out of complex HDI vias

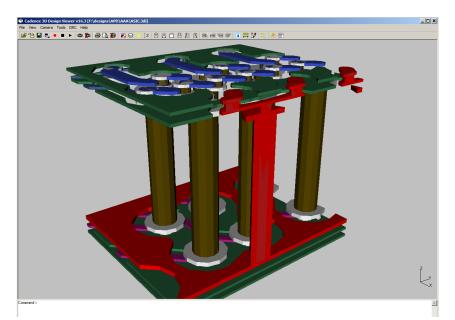


Figure 5: Cadence 3D Design Viewer allows for detailed study of sections of a design to be sectioned out and visualized in 3D

#### Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

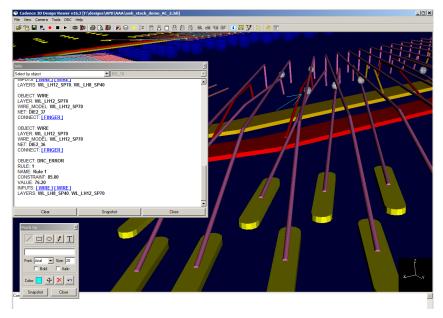


Figure 6: A design rule violation is highlighted using the info command. 3D visualization lets you see precisely where 3D spacing rules are violated



Cadence is transforming the global electronics industry through a vision called EDA360. With an application-driven approach to design, our software, hardware, IP, and services help customers realize silicon, SoCs, and complete systems efficiently and profitably. www.cadence.com

© 2010 Cadence Design Systems, Inc. All rights reserved. Cadence, the Cadence logo, and Allegro are registered trademarks of Cadence Design Systems, Inc.

21397 10/11 KM/DM/PDF