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Interview: SiP16.0 extends RFSiP Implementation to Parasitics/Simulation

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SiP16.0 release extends the RFSiP Implementation flow offered in 15.7 to Parasitics/Simulation flow. In this cdnusers interview, Taranjit Kukal, Cadence RFSiP/PSpice product engineer lead, briefly discusses the most important features.

cdnusers: Kukal, tell us about your background working with the SiP 16.0 product release

Taranjit Kukal: We launched the Cadence SiP technology in 2006. I am Product Engineer (PE) for the RF SiP technology. I was responsible for developing initial RF SiP flow requirements and worked with early development partners to validate those requirements. As PE owner of the RF SiP solution, I work closely with customers and the Cadence field organization to develop future requirements for the solution. Once the solution gets implemented, I take it to the Field and AEs in order to train them and seek feedback for any gaps that need to be bridged. Since I also own the PE for the Allegro® AMS Simulator and Cadence PSpice® solution, SiP16.0 was of special interest to me since the flow was around enabling smooth simulations for RF SiP designs.

cdnusers: What is the one new thing designers should know about this release?

Taranjit Kukal: SiP16.0 enables the creation of a single, circuit-simulation capable, top-level SiP RF module schematic that includes the RF/analog ICs and substrate level passive components that are part of the final SiP design. The capabilities like test-bench (partial circuit extraction) generation and parasitic back-annotation allow designers to quickly analyze portions of designs through simulations. The selected portion of design is extracted into a separate test-bench design and can be simulated with parasitic information annotated.

cdnusers: Tell us how it works in Virtuoso 6.1.1

Taranjit Kukal: Integration with Virtuoso 6.1.1 allows designers to leverage multi-mode simulations, where Silicon DIE(s) put on a single SiP and using different technology nodes can be simulated without going through the problems of renaming models across different technology model files. It also provides access to the new RF constraint management system introduced in Virtuoso 6.1.1. This integration works on OpenAccess and has new look and feel with jazzy features like hallows.

cdnusers: What is the one new thing designers should know about this release?

Taranjit Kukal:There are many features that strengthen what was offered in the initial release of SiP

like DIE export enhancements, support of replicated blocks, symbol ECOs and improvements in abutment of SiP layout routes into tline sub-schematics.

Items like package connectivity import allows designers to add large pin package in SiP layout and later import it into schematic as logical symbol with all its connectivity. Without this feature, designers could spend hours in manually creating and adding package symbol in schematic.

Another important feature is capability to generate lumped models for transmission line elements that get annotated into schematic as 1st order back-annotation of routes in SiP Layout. This helps quick simulation and analysis using simulator like Spectre.

cdnusers: Now some personal questions. How do you concentrate when working? Any tricks?
Taranjit Kukal: Since PE role requires one to do multi-tasking with interface to customers, AEs, Marketing and Engineering, concentration is a real challenge. I use my early mornings or Saturdays to do any work that requires full concentration. The trick is to send my wife to her parent's house on Saturdays (grin)

cdnusers: Where do you do your best thinking?
Taranjit Kukal: It is not costly in India to keep a chauffer; so I use my office shuttle hours to do my deep thinking, sitting at rear of the Car.

cdnusers: What do you do after a long day or week of working on routing problems to relieve your stress levels?
Taranjit Kukal: Meditation. I just sit in a room for 15 minutes -- talk to formless GOD and remind myself that life is virtual reality. So work hard but do not be Tense.

About the author
Taranjit Kukal is a Lead Product Engineer at Cadence Design Systems, Inc. responsible for RF SiP and PCB analog solutions.