Modeling and Analysis Methodologies of Complex Digital Systems-in-Package Designs

Zhen Mu

INVENTIVE

cādence

Topics

- **Design Challenges of System in Package (SiP)**

- **Modeling and analysis solutions**
  - **Co-Design methodologies**
  - **SI and PI analysis**

cādence™

Topics

- **Design Challenges of System in Package (SiP)**

- **Modeling and analysis solutions**
  - **Co-Design methodologies**
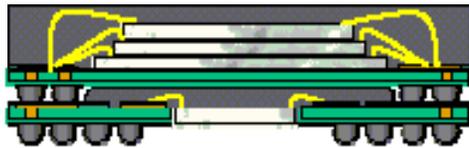 - **SI and PI analysis**

cādence™

What is SiP?

- SiP
  - Single package that combines all of the electronic components (digital ICs, analog ICs, RF ICs, passive components or other elements) needed to provide a system or sub-system.
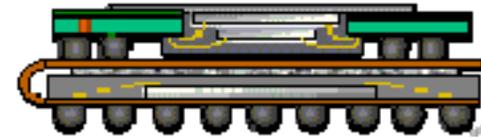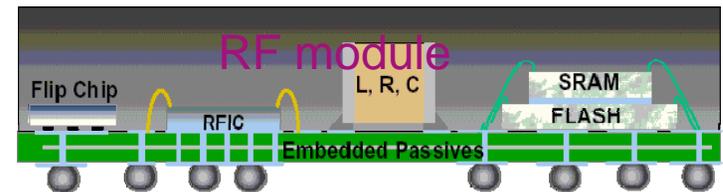
Courtesy of Philips

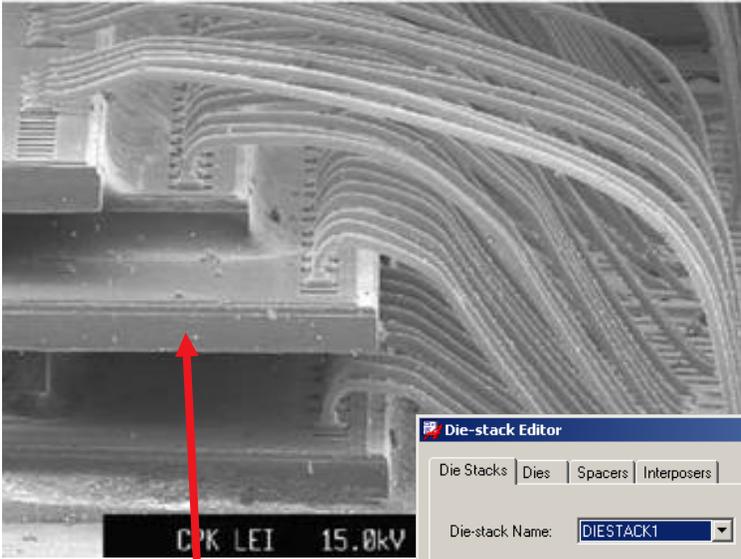**cādence**™

Multiple die connections

Die stacking

Package-on-package

3D IC

RF module

Flip Chip

RFIC

L, R, C
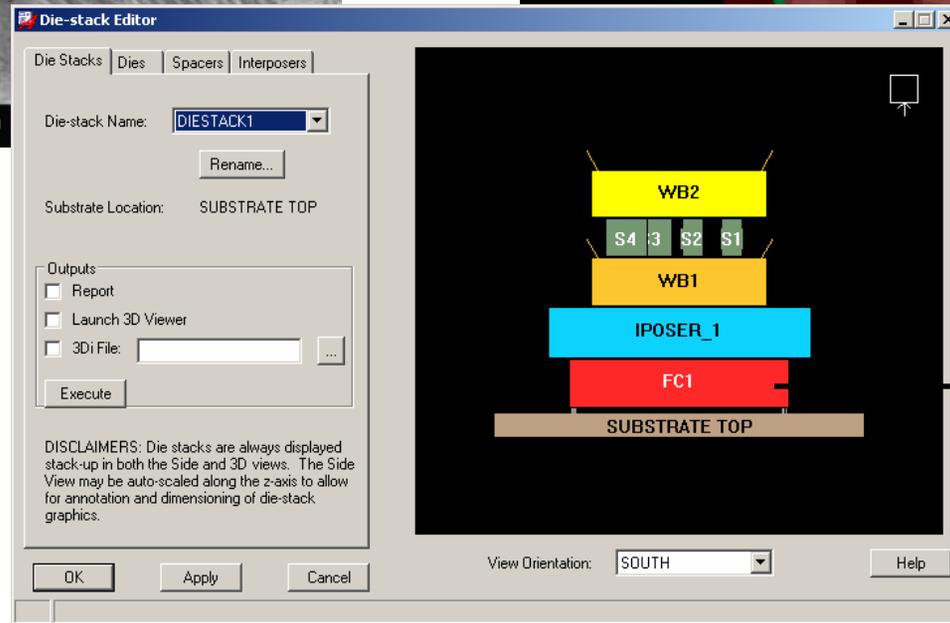
SRAM

FLASH

Embedded Passives

cādence™

Complex die stack design

Actual Stack Design
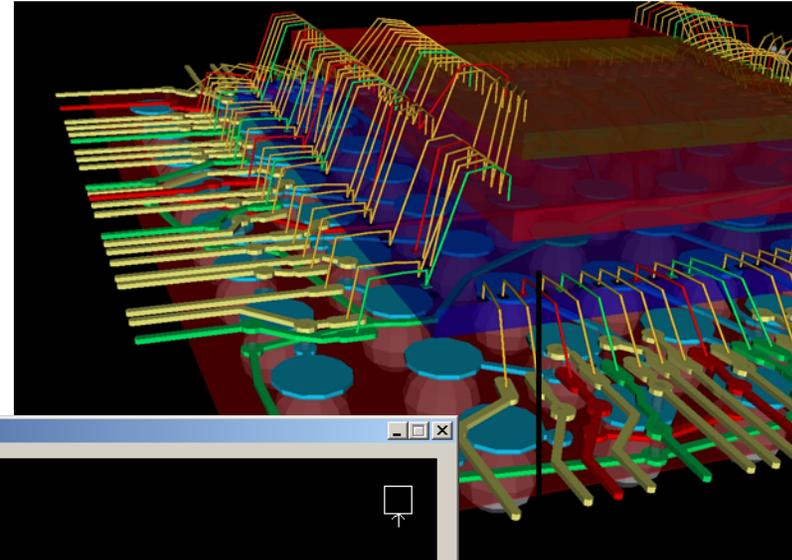
3D Stack Viewer

3D Stack Design

cādence™

Topics

- **Design Challenges of System in Package (SiP)**

- **Modeling and analysis solutions**
  - **Co-Design methodologies**
  - **SI and PI analysis**

cādence™

Modeling and analysis challenges

- Optimization requires design automation
- Recongnicing the differences between SiP design and classic single package and PCB designs
- Issues
  - Multiple stacked dies are placed vertically or horizontally
  - Connection between multiple dies are realized by wirebonding, interposer, interconnect, or flip-chip technology
  - IC design needs to consider package design, while package design needs to consider IC requirements
    - How to make die information available to package designers, and how to pass package models back to IO designers to simulate entire signal path
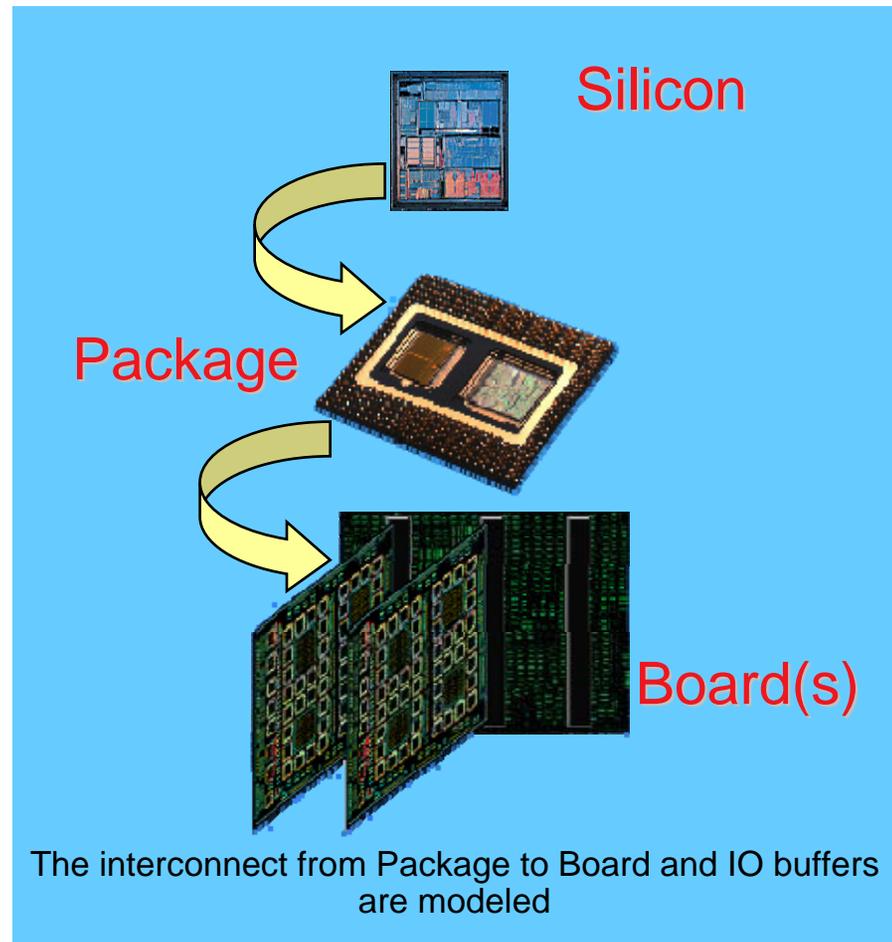   - Data passing and property mapping

cādence™

Modeling and analysis challenges (cont')

- Fundamental requirements for SiP tools
  - An environment with IC/package/board co-design and co-simulation capabilities
  - To provide engineers with Signal Integrity (SI) and Power Integrity (PI) solutions
   - Concurrent pre-route analysis and post-route verification

cādence™

Co-design methodologies in high-speed design

- Problem1: Signal path from silicon to board through package
  - Reflections, xtalk, timing

Silicon
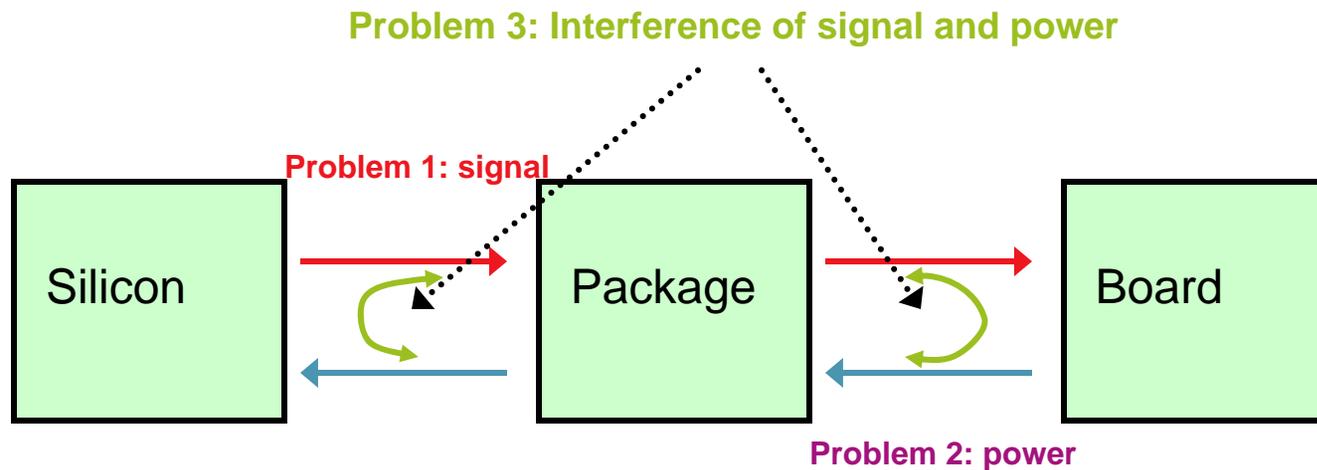
Package

Board(s)

The interconnect from Package to Board and IO buffers are modeled

cādence™

Co-design methodologies in high-speed design (cont')

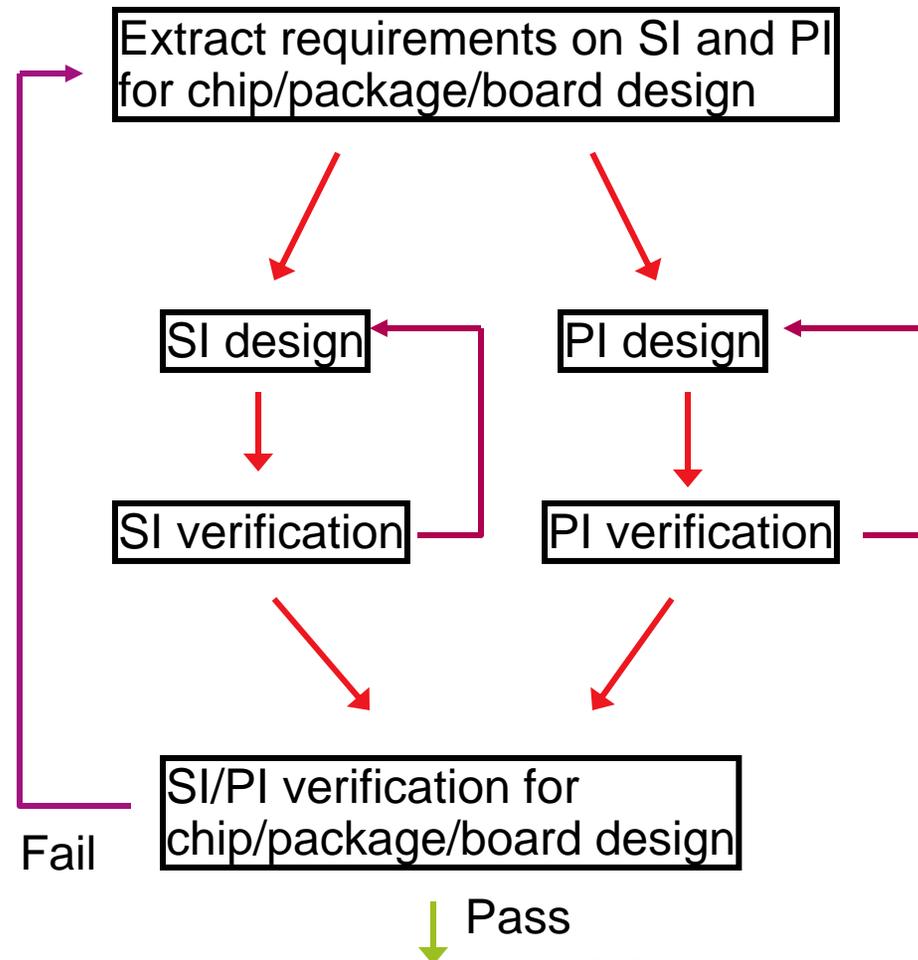- Problem 2: Power delivery path from board to silicon through package

Silicon

Package

Board(s)

Power is delivered from PCB to Silicon through Package

cādence™
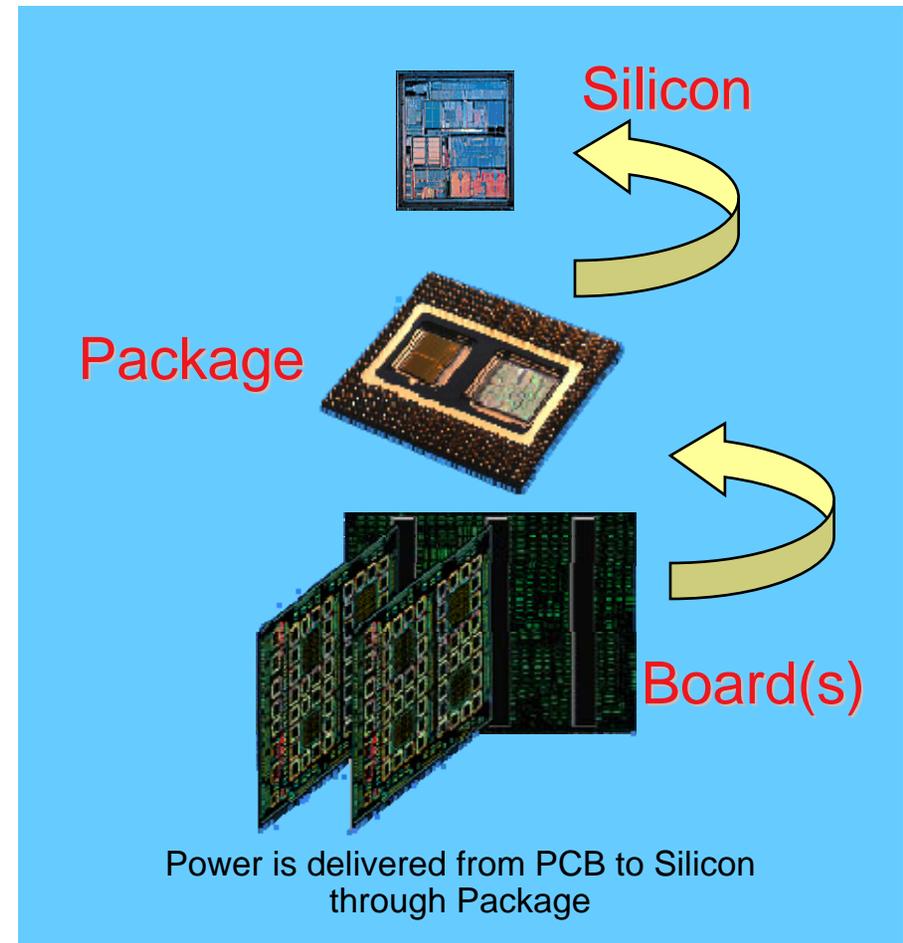
Co-design methodologies in high-speed design (cont')

- Problem 3: Effects between signal and power supply

Problem 3: Interference of signal and power

Problem 1: signal

| Silicon | Package | Board |

Problem 2: power

cādence™

Co-design methodologies in high-speed design (cont')

- A general flow for co-design
  - Not only to include silicon/package/board co-design, but also SI and PI co-design and co-simulation

```
        Extract requirements on SI and PI
        for chip/package/board design
               │                    │
               ▼                    ▼
        ┌─────────────┐      ┌─────────────┐
        │  SI design  │◄──   │  PI design  │◄──
        └─────────────┘  │   └─────────────┘  │
               │         │          │         │
               ▼         │          ▼         │
        ┌──────────────┐ │   ┌──────────────┐ │
        │SI verification│─┘   │PI verification│─┘
        └──────────────┘     └──────────────┘
               │                    │
               ▼                    ▼
        SI/PI verification for
        chip/package/board design
```

Fail

Pass

cādence™

Problem 1 - Signal analysis: stackup design

- Crossection details

Problem 1 - Signal analysis: establishing constraints

- Early exploration on multi-die connection

cādence™
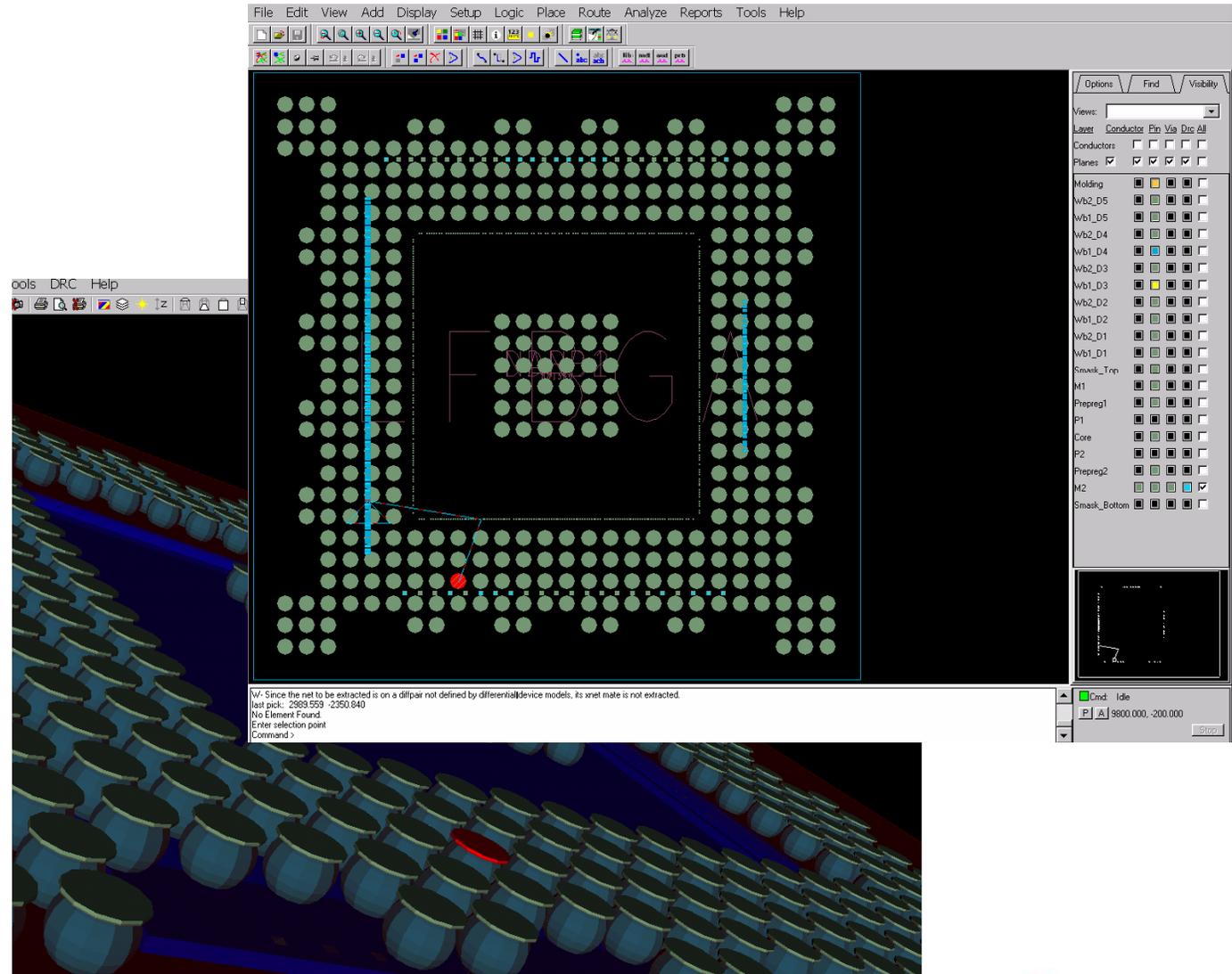
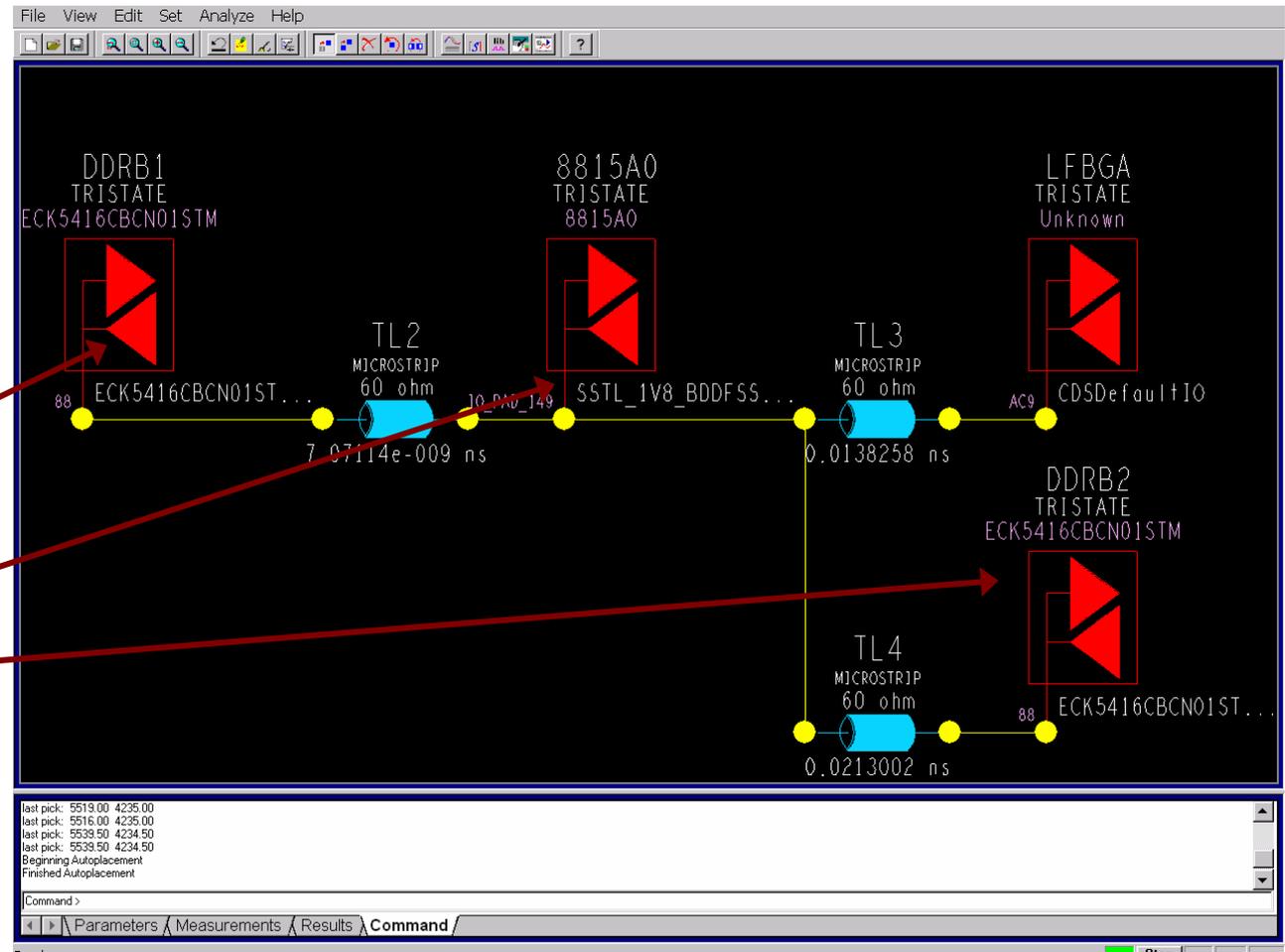# Problem 1 - Signal analysis: establishing constraints

- Extracted circuit for solution space simulation
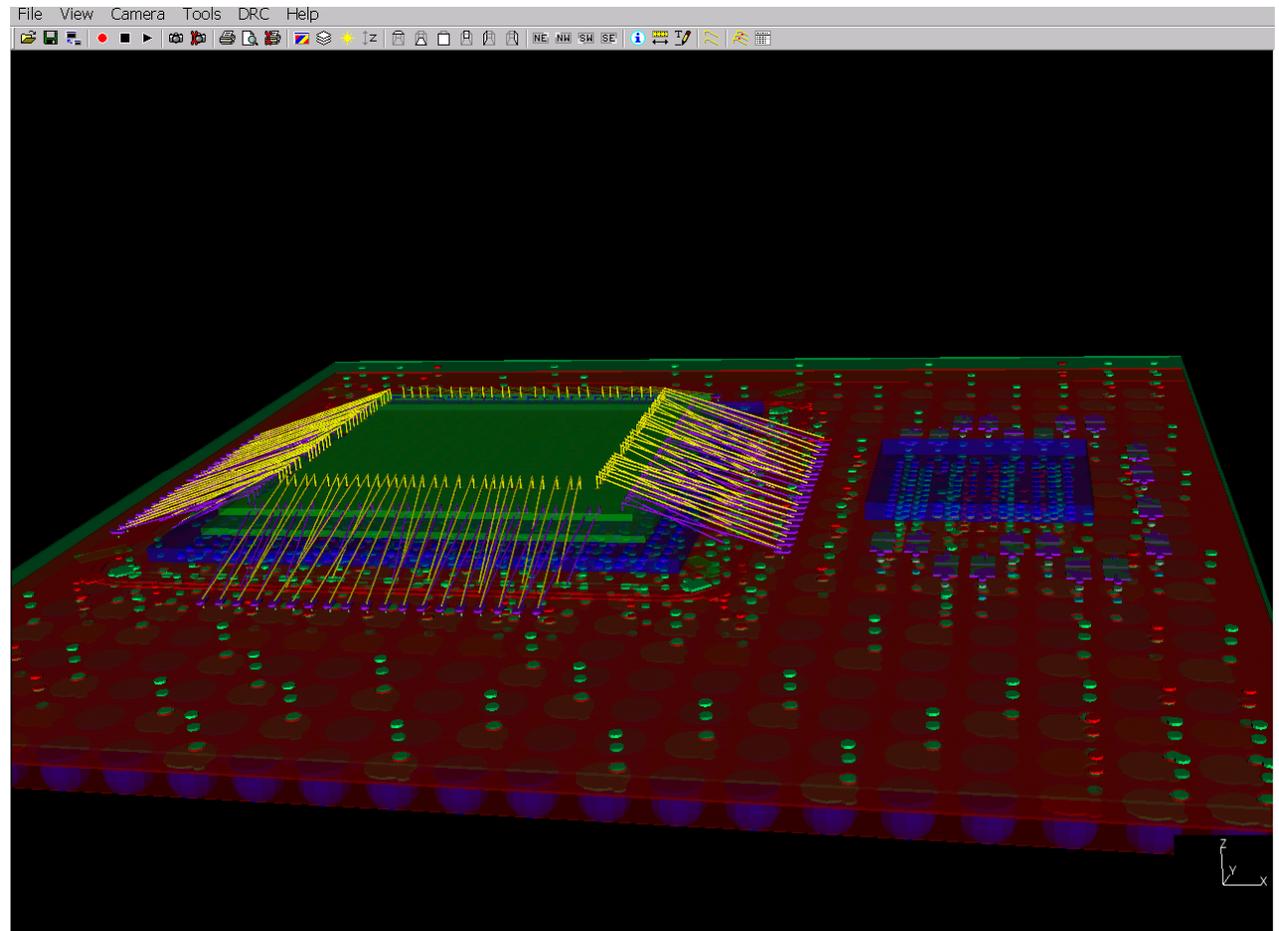
Three dies

cadence™

Problem 1 - Signal analysis: interconnect modeling
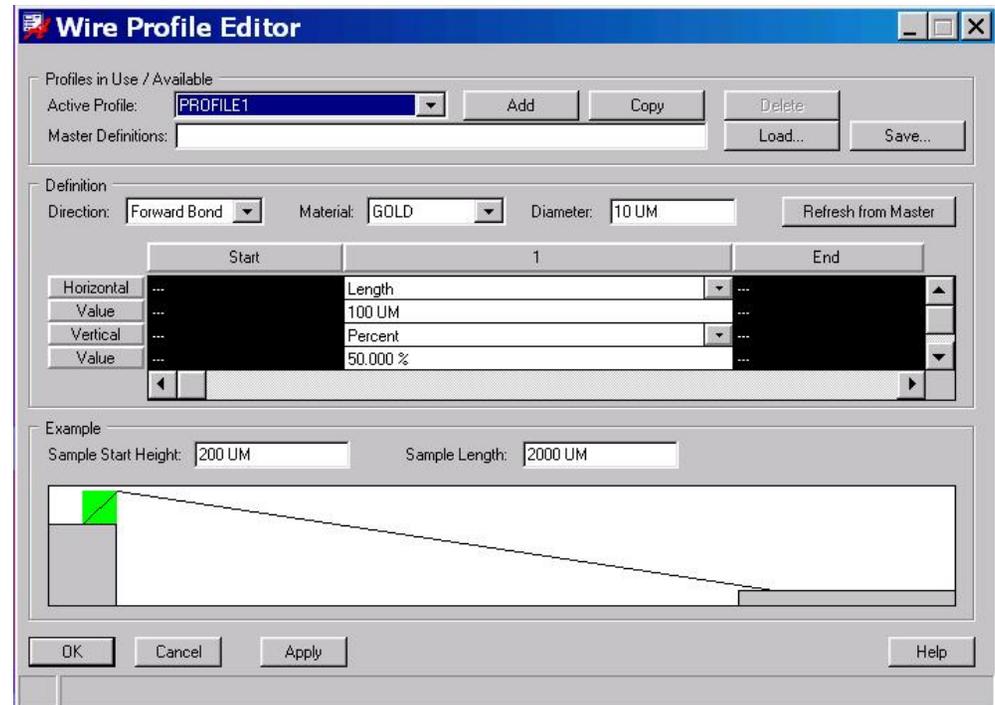
- Detailed interconnect modeling
  - Wirebonds

Problem 1 - Signal analysis: assistant to analysis

- Detailed interconnect modeling
  - 3D view

cādence™

Problem 1 - Signal analysis: wirebond constraints

- Perform what/if analysis by changing wirebond profiles
  - Work with existing design and/or start new design
  - Edit the parameters
  - Update (or extract) constraints

cādence™

Problem 1 - Signal analysis: coupled wirebond modeling

- Create 3D models of multi-coupled wiorebonds

cādence™
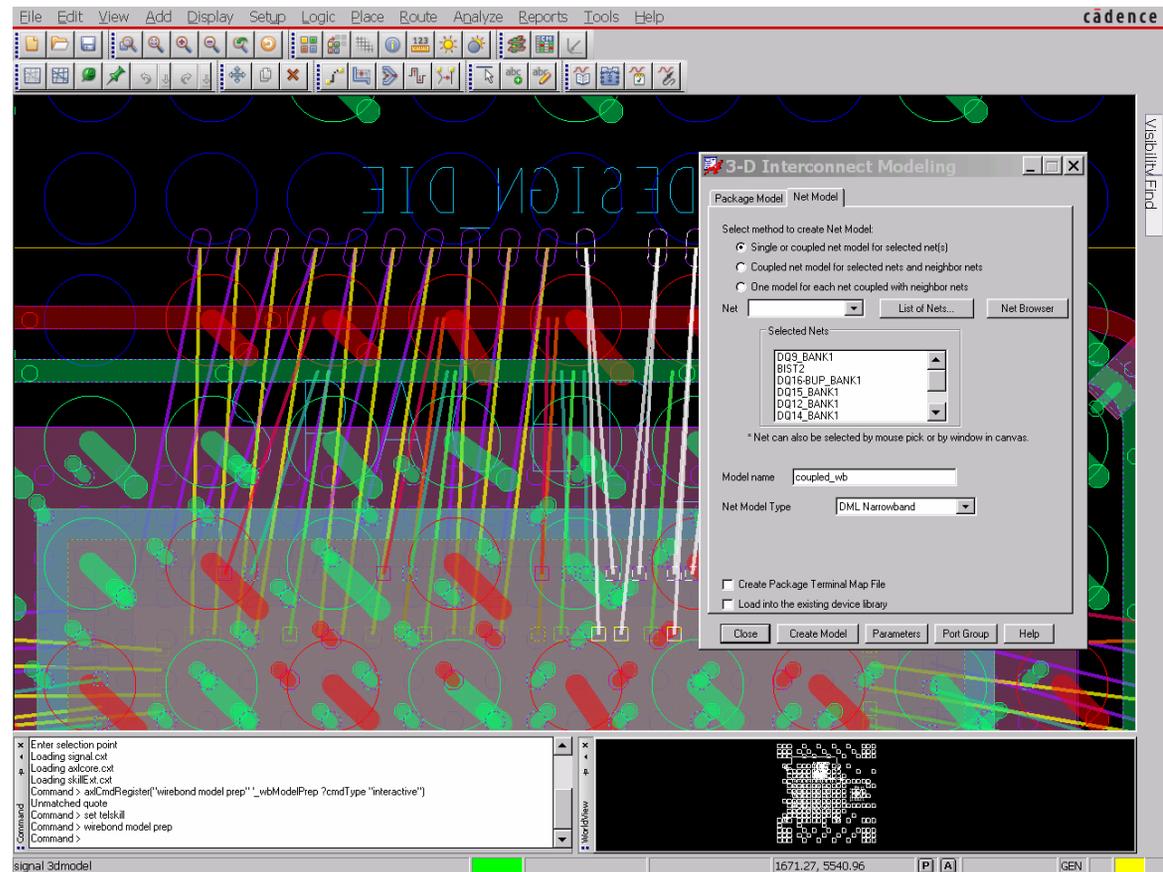
Problem 1 - Signal analysis: coupled wirebond modeling (cont')

- Interested wirebonds

cādence™
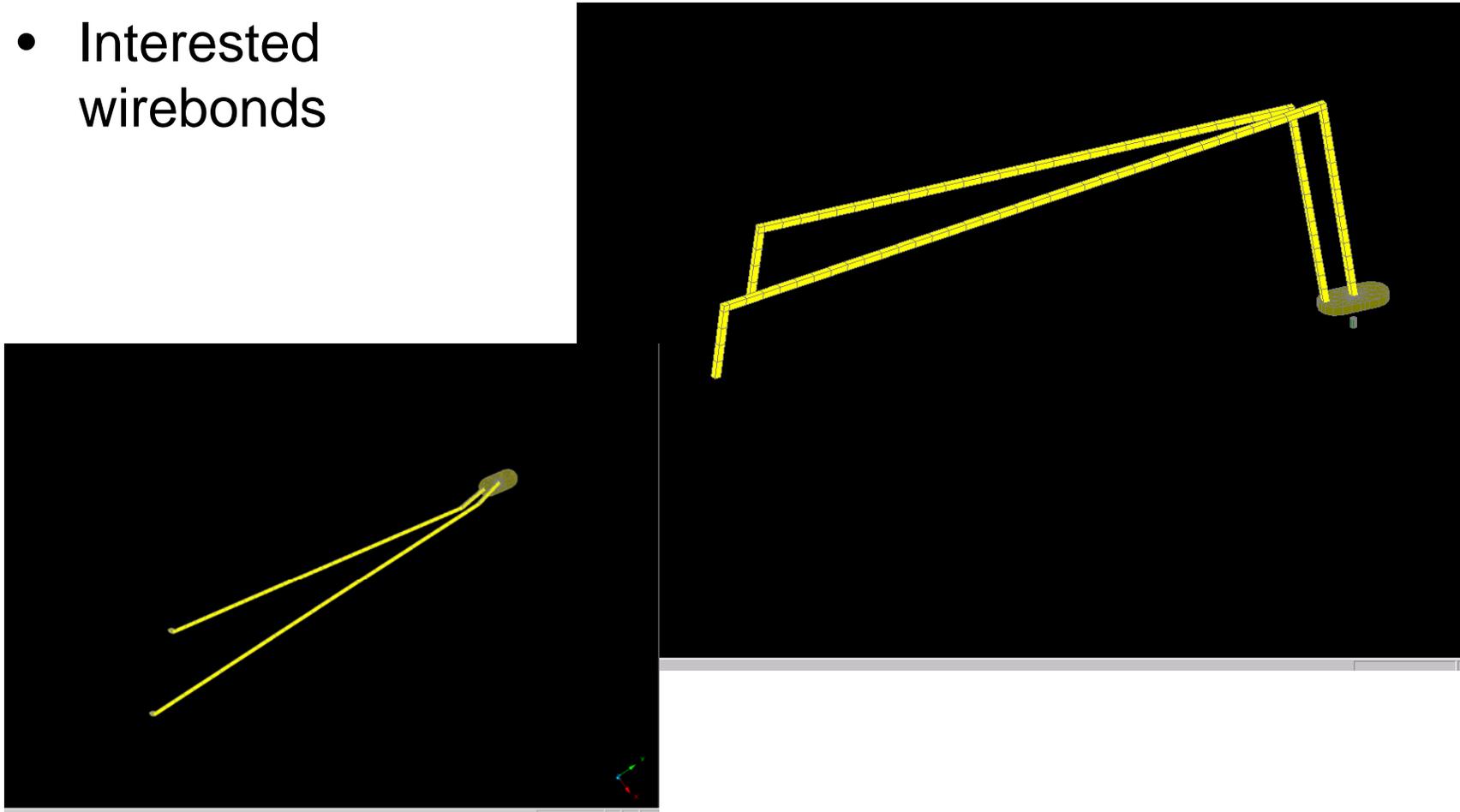
Problem 1 - Signal analysis: coupled wirebond modeling (cont')

- Model validation with topology simulation

cādence™
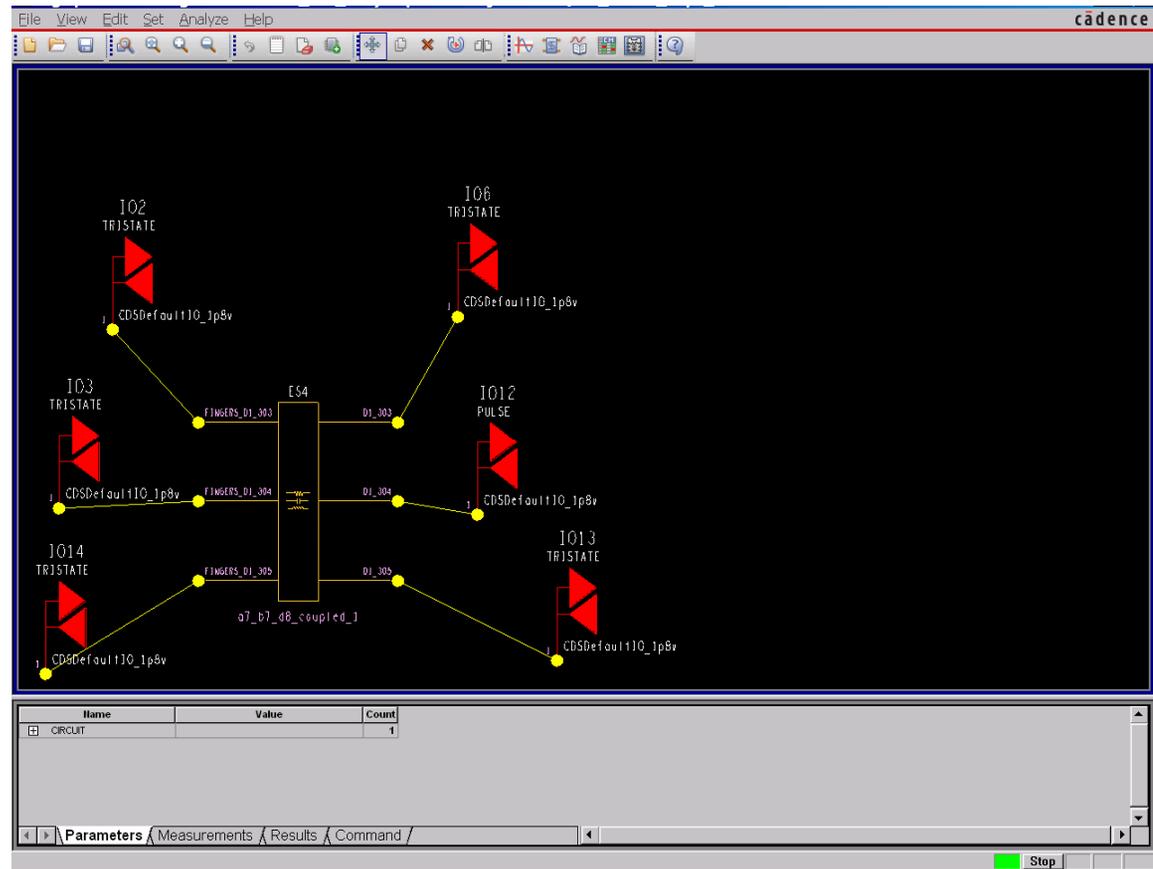
Problem 1 - Signal analysis: reflections, crosstalks, timing

- **Building simulation circuits**
  - Simulating routed nets
  - Using 3D models
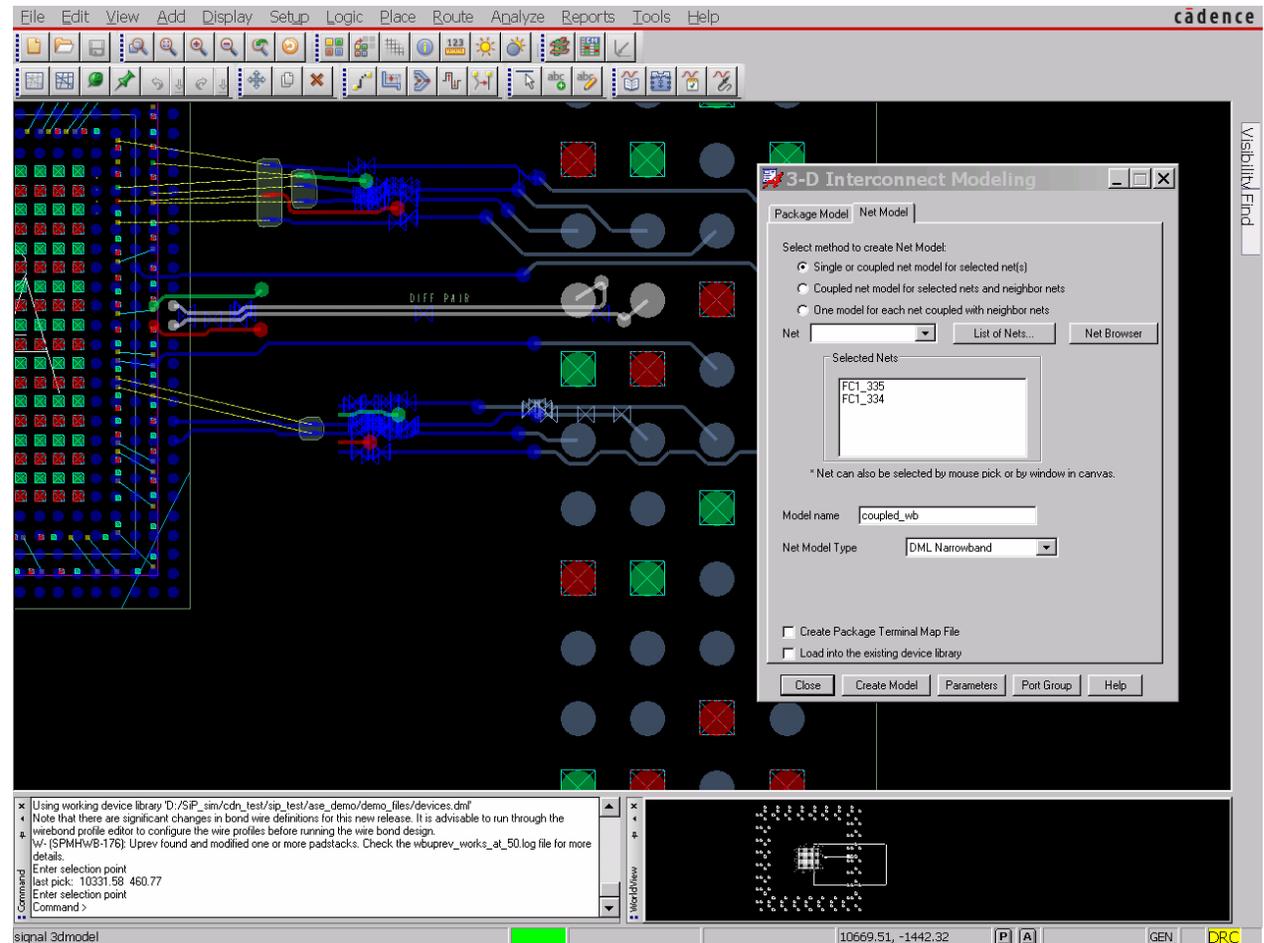
Problem 1 - Signal analysis: reflections, crosstalks, timing (cont')

- Simulation circuit

cādence™
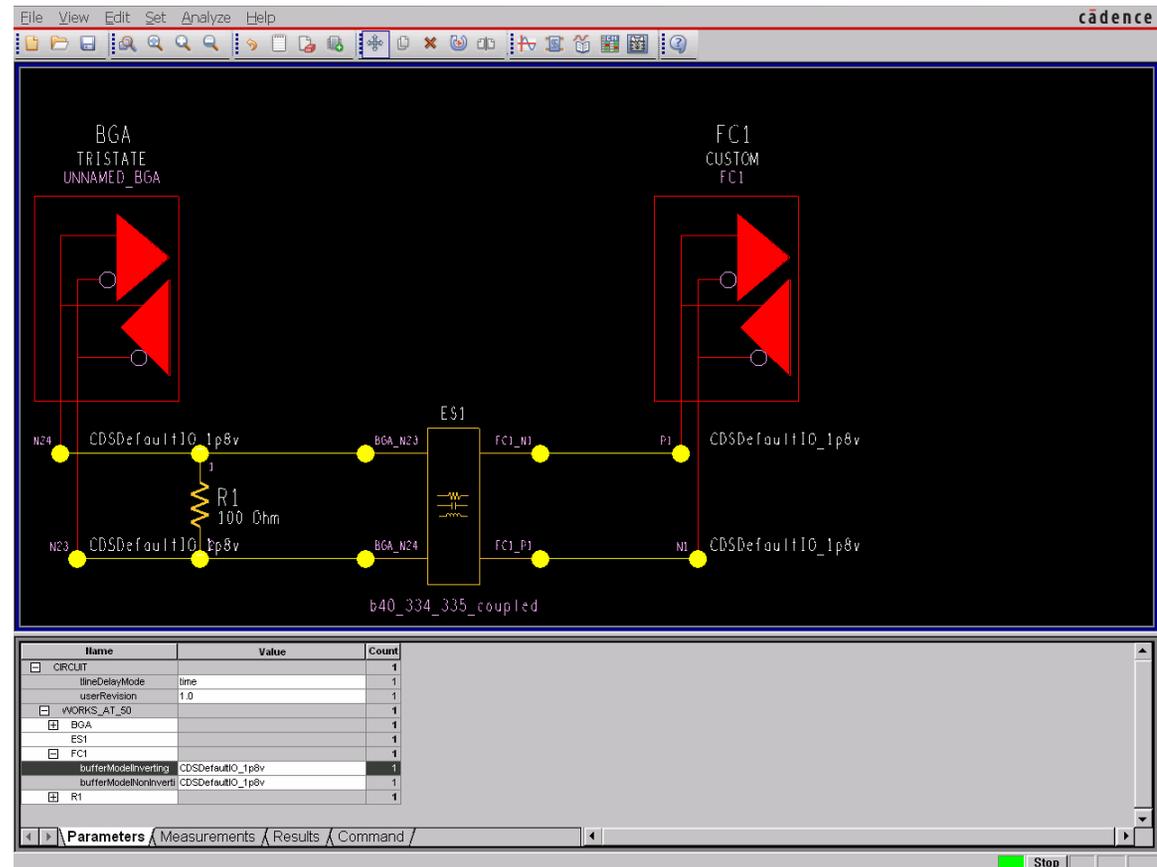
Problem 2 - Power analysis: power delivery on SiP

- Power delivered to multiple chips through substrate
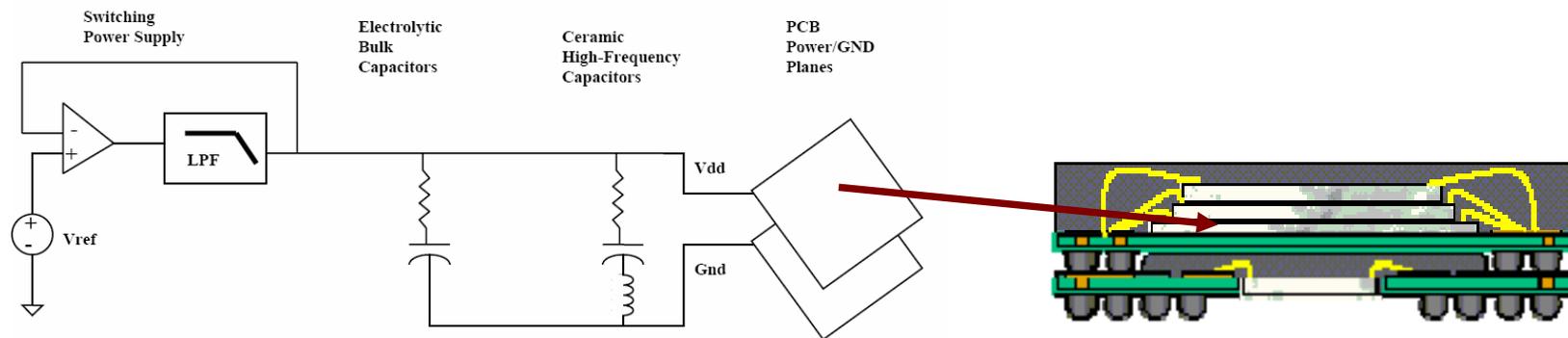
cādence™

Problem 2 - Power analysis: power delivery

- Power delivery to multiple dies

cādence™

Problem 2 - Power analysis: power delivery

- Power delivery to multiple dies

cādence™
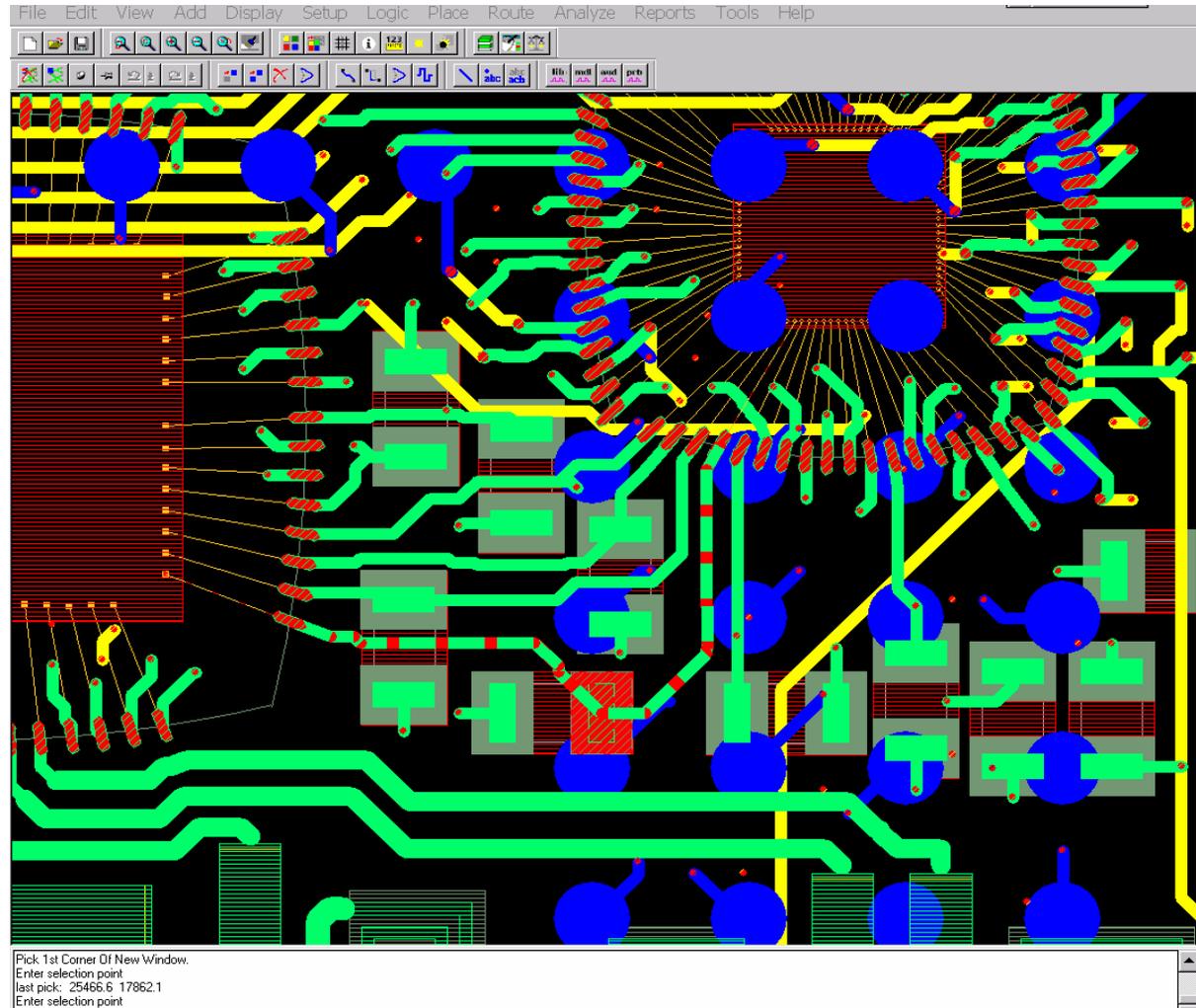
Problem 2 - Power analysis: power delivery

- Power delivery to multiple dies

  - Decoupling capacitor selection and placement

cādence™
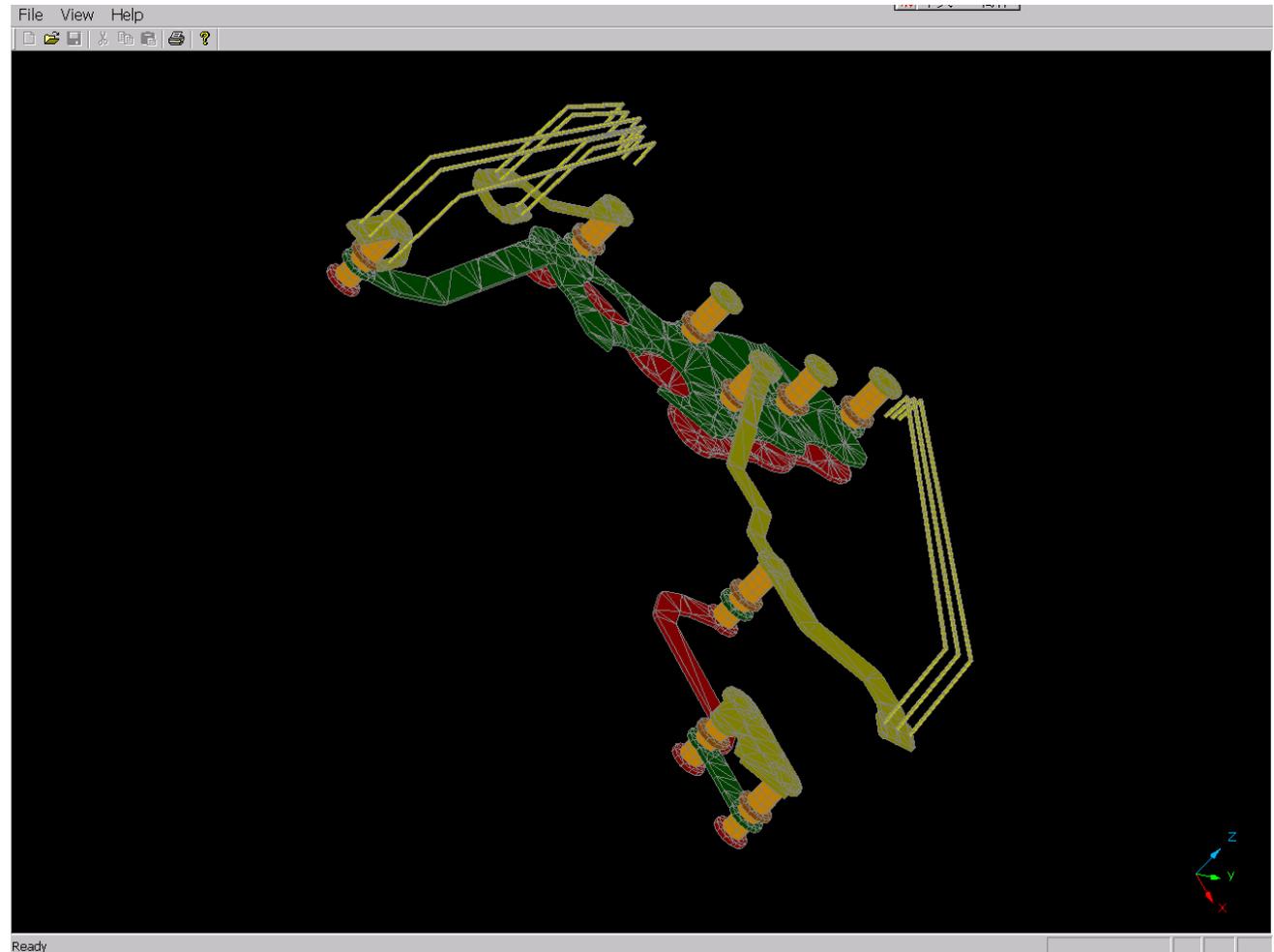
Problem 2 - Power analysis: decoupling analysis on SiP

- Select power and ground nets that deliver power to multiple dies
- Create coupled 3D models of power/ground nets
- Performa frequency domain analysis on the extracted power/ground model
- Place decoupling capacitors at die pins or at BGA pins, if needed
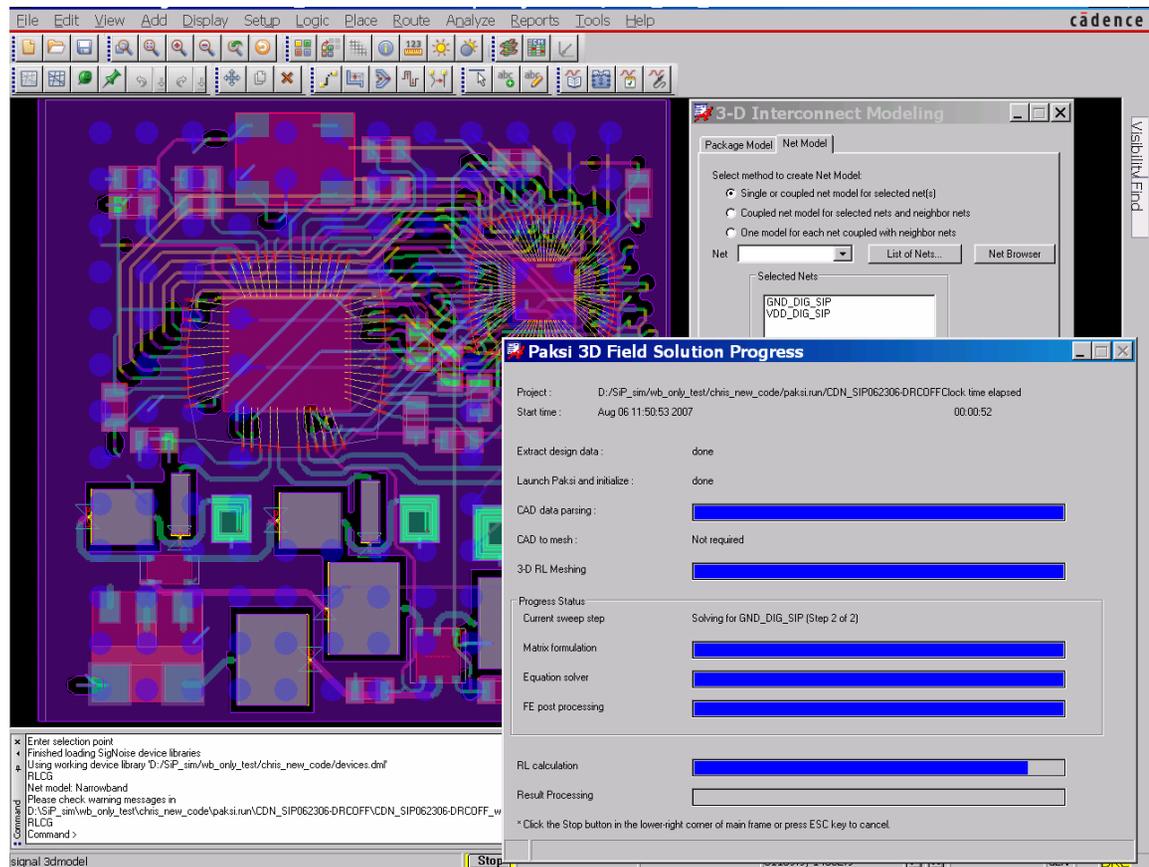
Problem 2 - Power analysis: decoupling analysis on SiP (cont')

- This is the impedance profile at different pin locations
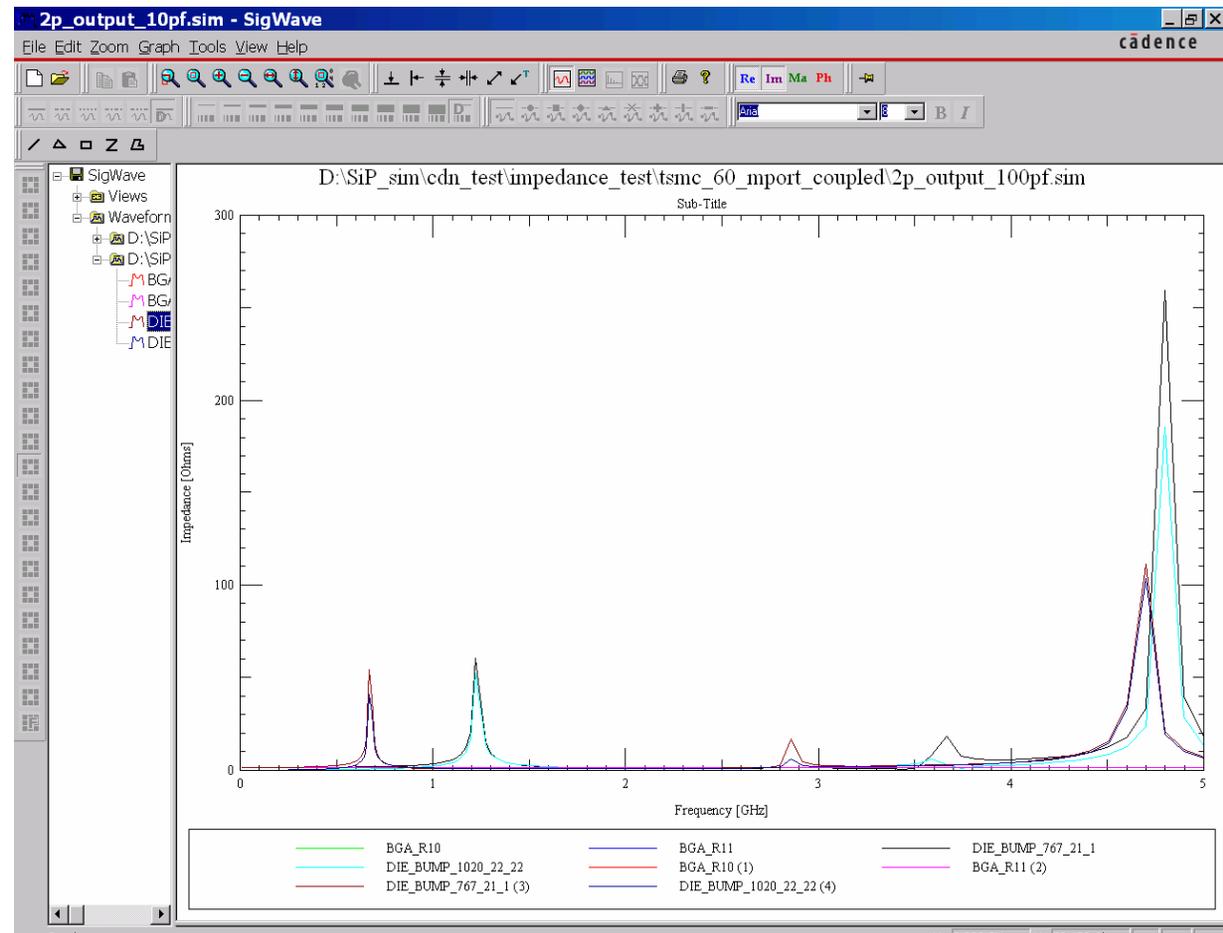
Problem 2 - Power analysis: decoupling analysis on SiP (cont')

- Observe the difference in impedance profile when placing decoupling capacitor at BGA side or at die side
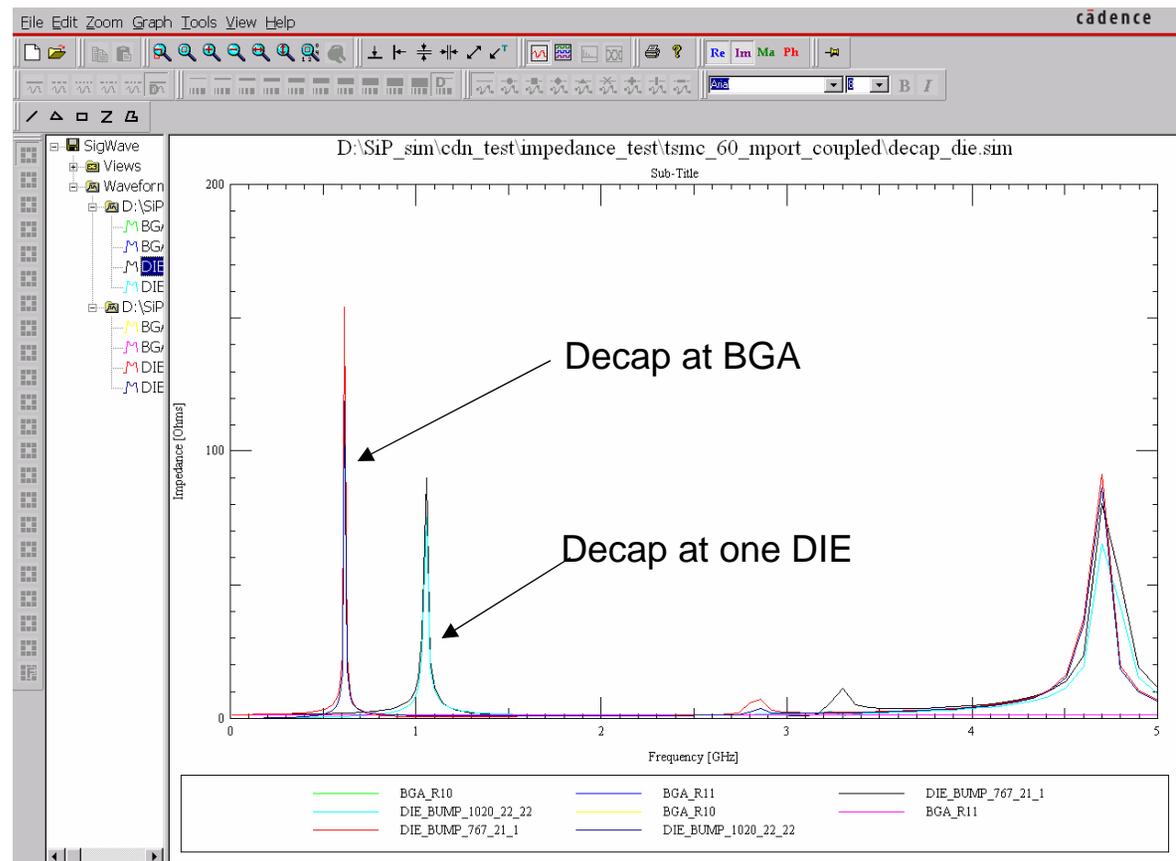
Problem 2 - Power analysis: time domain simulation on SiP

- Observe time domain waveforms at BGAs and die pins
  - This is voltage drop across package in time domain
- Change capacitance values to verify decoupling capacitor effects

Problem 2 - Power analysis: DC resistance extraction on SiP

- When frequency is set to zero, DC resistance can be obtained

    - Using port grouping function, the resistance between any two pins on any net can be extracted

    - Then, current drop of the entire path on a DC net can be easily derived

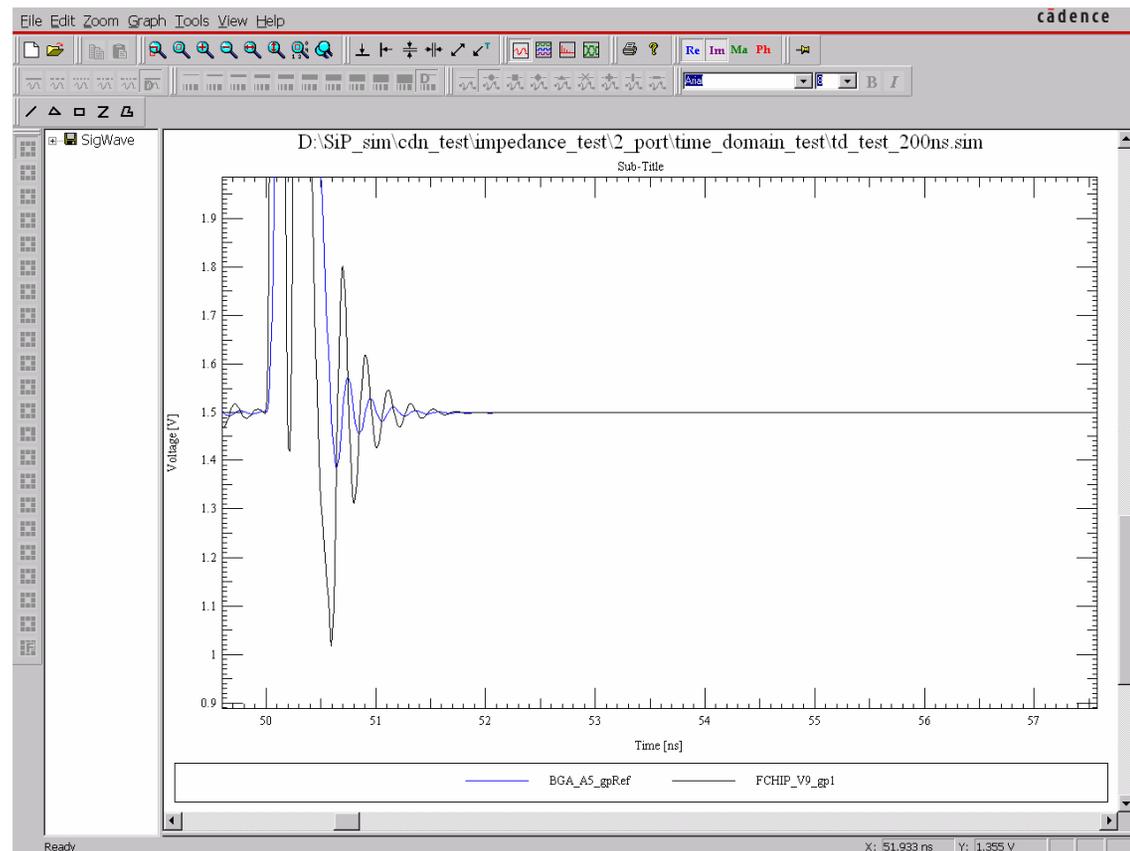|	A	B	C	D	E	F	G	H
1	Parasitic Extraction Results ----- (performed on August 06. 2007) Net Name							
2								
3	Neti	NetJ	Rij (mOhm	Lij (nH)	Cij (pF)	Gij (uMho)	Td (ns)	
4	PLL_VDD_	PLL_VDD_	3.45E+01	2.43E+00	2.32E+00	0	7.52E-02	
5	PLL_VDD_	NET0365<	0.00E+00	2.14E-02	1.15E-02	0		
6	NET0365<	PLL_VDD_	0.00E+00	2.14E-02	1.15E-02	0		
7	PLL_VDD_	NET0365<	0.00E+00	1.85E-02	1.15E-02	0		
8	NET0365<	PLL_VDD_	0.00E+00	1.85E-02	1.15E-02	0		
9	PLL_VDD_	NET0204	0.00E+00	3.37E-02	2.97E-01	0		
10	NET0204	PLL_VDD_	0.00E+00	3.37E-02	2.97E-01	0		
11	PLL_VDD_	RESET	0.00E+00	1.93E-04	6.55E-02	0		
12	RESET	PLL_VDD_	0.00E+00	1.93E-04	6.55E-02	0		
13	PLL_VDD_	POL	0.00E+00	5.46E-03	3.05E-02	0		
14	POL	PLL_VDD_	0.00E+00	5.46E-03	3.05E-02	0		
15	PLL_VDD_	NET294	0.00E+00	2.75E-04	1.09E-01	0		
16	NET294	PLL_VDD_	0.00E+00	2.75E-04	1.09E-01	0		
17	PLL_VDD_	NET284	0.00E+00	-9.27E-05	1.17E-02	0		
18	NET284	PLL_VDD_	0.00E+00	-9.27E-05	1.17E-02	0		
19	PLL_VDD_	NET251	0.00E+00	-1.35E-03	1.17E-02	0		
20	NET251	PLL_VDD_	0.00E+00	-1.35E-03	1.17E-02	0		
21	PLL_VDD_	NET249	0.00E+00	-1.61E-03	1.07E-02	0		
22	NET249	PLL_VDD_	0.00E+00	-1.61E-03	1.07E-02	0		
23	PLL_VDD_	F_44MHZ	0.00E+00	-2.68E-03	2.34E-02	0		
24	F_44MHZ	PLL_VDD_	0.00E+00	-2.68E-03	2.34E-02	0		
25	PLL_VDD_	CHS<3>	0.00E+00	-1.53E-03	2.32E-02	0		
26	CHS<3>	PLL_VDD_	0.00E+00	-1.53E-03	2.32E-02	0		
27	PLL_VDD_	CHS<2>	0.00E+00	-1.86E-03	2.33E-02	0		
28	CHS<2>	PLL_VDD_	0.00E+00	-1.86E-03	2.33E-02	0		
29	NET0365<	NET0365<	5.99E+02	1.03E+01	1.97E+00	0	1.43E-01	
30	NET0365<	NET0365<	0.00E+00	4.47E-01	6.78E-02	0		
31	NET0365<	NET0365<	0.00E+00	4.47E-01	6.78E-02	0		
32	NET0365<	NET0204	0.00E+00	3.03E-02	1.20E-02	0		
33	NET0204	NET0365<	0.00E+00	3.03E-02	1.20E-02	0		
34	NET0365<	RESET	0.00E+00	-6.56E-02	2.43E-02	0		
35	RESET	NET0365<	0.00E+00	-6.56E-02	2.43E-02	0		
36	NET0365<	POL	0.00E+00	1.25E-01	2.43E-02	0		
37	POL	NET0365<	0.00E+00	1.25E-01	2.43E-02	0		
38	NET0365<	NET294	0.00E+00	1.33E-03	1.20E-02	0		

cādence™

Summary

- ## System-in-Package is the right integration solution for wireless and consumer products
  - It posts great challenges to designs and analyses (differences between single package and PCB designs)

- ## IC-Package-Board co-design and co-simulation methodologies are key to successful SiP designs

- ## Cadence provides a design and analysis environment to meet digital SiP design requirements
  - SI and PI solutions need to support multiple die designs
    - Interconnect designs, stacked die configurations, etc…
  - SI and PI solutions are implemented in Cadence's Digital SiP environment

cādence™