DATASHEET

CADENCE RADIO FREQUENCY (RF) DESIGN METHODOLOGY KIT

The Cadence® RF Design Methodology Kit leverages the latest technologies and advanced verified methodologies from Cadence to enable wireless design teams to shorten design cycle time by increasing silicon predictability and enabling greater RF design productivity. This Kit delivers verified methodologies packaged in a system-to-tapeout RF IC design flow, demonstrated on a segment representative design.

CADENCE RF DESIGN METHODOLOGY KIT

The Cadence RF Design Methodology Kit demonstrates advanced methodologies for managing RLCK parasitics, inductance synthesis and modeling. The Kit links system-level design with IC implementation, and accurately, yet rapidly, verify the complete design which spans system-level, digital, analog, and RF design domains. These capabilities are demonstrated on a 802.11 b/g CMOS reference design that includes the RF transceiver with integrated PA, PLL and analog baseband. Fully extracted RLCK views are used to accurately verify the chip at the top level with detailed information to ensure silicon predictability. Intelligent RC reduction and simulation strategies are deployed to ensure rapid simulation results.

Applicability Consulting

System-to-Tapeout RFIC Design Flow
- Link to System Level Design
- Passive Component Synthesis and EM Modeling
- RFIC Simulation and Verification
- Phase Lock Loop Design
- Managing Parasitics

Comprehensive Kit Documentation
Workshops, Simulation Plans, etc.

802.11b/g Zero-IF WLAN Transceiver
180nm CMOS gPDK

Figure 1: Cadence RF Design Methodology Kit components

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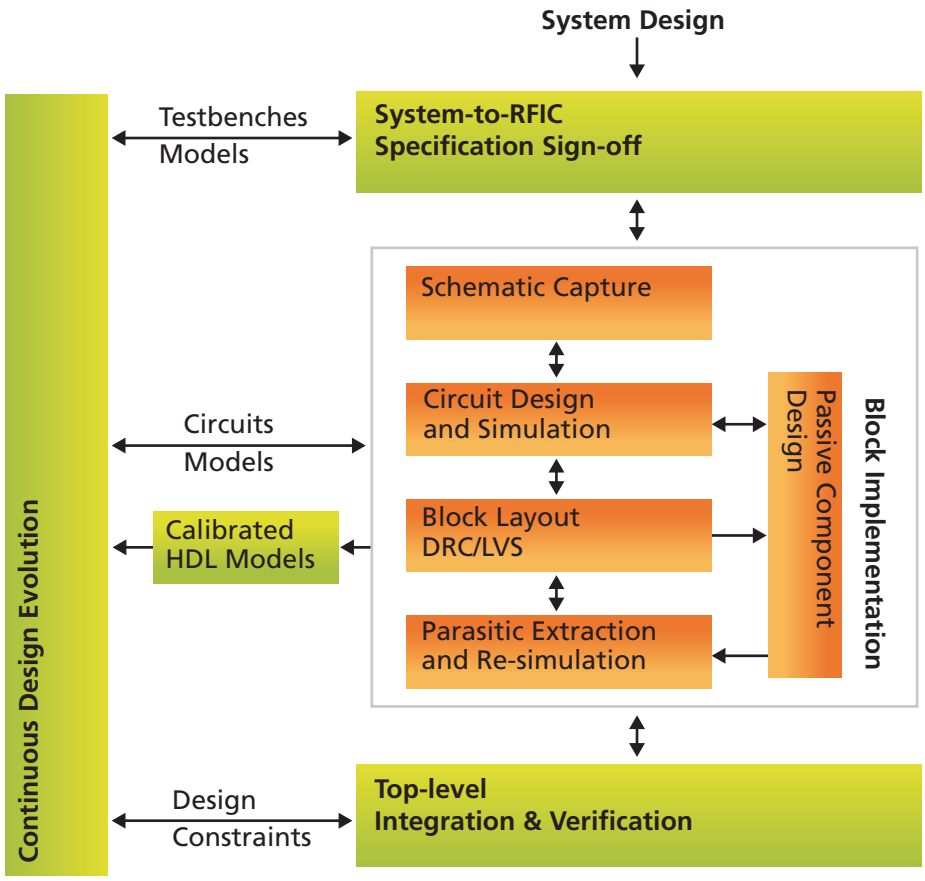

Figure 2: RF Design Flow

Re-usable, pre-setup components including test benches, models, and simulation plans for blocks including the LNA, down conversion mixers, Rx/Tx band pass filters, and power amplifiers are fully contained in this Cadence Kit to ensure fast, silicon accurate design capabilities.

A design team can use the segment representative design as a basis to understand the methodology, and then map the demonstrated techniques and technologies to their own designs, thus creating a realizable action plan to improve their own design process. The step by step approach allows a team to absorb and understand a wide array of technologies that can optimize complex RF designs.

BENEFITS

The Cadence Radio Frequency (RF) Design Methodology Kit helps customers to address wireless opportunities with methodologies in the following areas:

- System conformance validation of the RFIC through MATLAB/ Simulink co-simulations
- Complete Spiral Inductor synthesis through EM Verification Flow
- PLL simulation guide
  - New technology to model and characterize PLL at transistor-level accuracy
  - Using PPV method to tremendously speed-up top-level simulation
- Enabling full-chip verification through new "local" envelope technique
- Full-chip functional verification methodology
  - Development and validation of FVM (functional verification model) with build-in assertions
  - Top-level integration as part of FV test suite
- Analyzing noise distribution and quickly prototyping of noise isolation schemes
- Leveraging system-level considerations by performing conformance testing to system-level specifications and matching against these specs throughout the IC design process
- Seamlessly managing a concurrent top-down and bottom-up design processes
- Performing functional, performance, and closed-loop verification, across multiple design domains including system-level, digital, mixed-signal, and analog/RF
- Managing IC parasitics effectively by intelligently simulating full chip with RCLX extracted views, optimizing for simulation accuracy and completeness

KIT COMPOSITION AND INTEGRATION

The Cadence RF Design Methodology Kit includes the following:

- Complete behavioral models, transistor-level schematics, and layout for the reference design
- Detailed step-by-step documentation to enable users to verify/validate the overall flow enabled by enhanced hands-on-workshops
- Proven and validated RF IC and System IC methodologies
- Re-usable, pre-setup components including test benches, models, and simulation plans for all RF transceiver blocks
- Expert consulting designed to map the verified and demonstrated methodologies to a specific customer design

The RF Design Methodology Kit relies on and integrates with the following technologies (not included):

- Virtuoso® Multi-Mode Simulation
- Virtuoso AMS Designer Simulator
- Virtuoso Spectre® Circuit Simulator
- Virtuoso Spectre RF Simulation Option
- Virtuoso UltraSim Full-Chip Simulator
- Virtuoso Passive Component Modeler
- Virtuoso Schematic Editor
- Virtuoso Analog Design Environment
- Virtuoso Specification-Driven Environment / Characterization and
- Modeling Environment
- Virtuoso Layout Editor / XL Layout Editor
- Assura® Design Rule Checker (DRC)
- Assura Layout vs. Schematic Verifer (LVS)
- Assura RF Extraction

For more information, email us at **info@cadence.com** or visit **www.cadence.com**

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