cadence®

# Cadence IC Package Design

## Efficiently design complex packages with first-pass success

Market demand for more functionality is driving the move to multi-layer flip-chip packaging to accommodate high-pin-count designs. To efficiently design these complex packages requires a sophisticated implementation tool that addresses both electrical and physical constraints. Cadence® IC package design technology is recognized worldwide for its efficient, flexible, and reliable implementation of dense, advanced package designs. Integrated signal and power integrity analysis ensures that electrical and physical challenges can be jointly addressed throughout the design cycle. Using Cadence IC package design technology, designers can meet compressed schedule demands with first-pass success.

## Cadence IC Package Design Technology

IC packaging is now a critical link in the silicon-package-board design flow. The Cadence Allegro® environment offers complete and scalable technology for the design and implementation of PCBs, packages, and systems-in-package (SiPs). Cadence IC package design technology allows designers to optimize complex, single, static/fixed wirebond or flip-chip package designs for cost and performance while meeting short project time-lines.

This constraint-driven, industry-standard technology enables traditional fixed-die package design. Cadence IC package design technology focuses on efficient wirebond design techniques, constraint- aware substrate interconnect design of both wirebond and flip-chip packages, and detailed interconnect extraction, modeling, and signal integrity/power delivery analysis.

Cadence IC package design technology is available in several different products and tiers, including:

- Allegro Package Designer (with License)
- Allegro Package Designer (with XL license)

*Note: XL license additionally licenses Cadence SiP Layout**

- Allegro Package SI (with L license)
- Allegro Package SI (with XL license)

*Note: XL licence additionally licenses Cadence SiP Digital SI**

** Cadence IC/package co-design technology is available to anyone utilizing an XL license for IC/ package design. View the Cadence SiP product datasheet for more information.*

## Benefits

- Supports the full front-to-back IC package design flow
- Simplifies and speeds the design process
- Manages design reuse
- Optimizes substrate performance and cost
- Allows users to determine best package and substrate technology early in the IC design cycle
- Makes physical, electrical performance, power delivery, and cost tradeoffs easily and accurately (Allegro Package SI)
- Accurately creates full or partial 3D package models through embedded integration with a third-party 3D field solver (supplied separately)
- Design partitioning enables multi-designer asynchronous design (available with XL license)
- Provides interconnect analysis from die to die, connecting the IC packages to the complete system interconnect (Allegro Package SI)

## Layout Features

### Constraint-Driven Physical Layout

Cadence IC package design technology includes all the functionality and features needed to design today's advanced packages. Full online design rule checking (DRC) supports the complex, unique requirements of all combinations of laminate, ceramic, and deposited substrate technologies. Multiple cavities, complex shapes, and interactive and automatic wirebonding are all supported. The easy-to-use Design Wizard walks you through each task and automates the process of creating the building blocks of an IC package, including the creation of die, package, plating bars, and

power/ ground rings. The die and BGA wizards automate definition of these library elements with your choice of text file standard formats (D.I.E., DEF, AIF), or a form-driven user interface, such as "textin" wizards.

## Sophisticated Substrate Modeling and Rule Checking

Design accuracy can be verified against a complete set of physical and electrical design rules (constraints). Physical constraints are physical design guidelines, established in a user-defined technology file, that ensure manufacturability. Electrical constraints are signal delay and distortion specifications for critical nets. Designs can be dynamically checked against these constraints throughout the design process to ensure they are meeting manufacturing and electrical specifications. Immediate feedback is provided by way of DRC markers as well as flagging violations in the spreadsheet- based Constraint Manager.

## Process Technology Reuse

Both substrate stack-up and constraint information are captured in a technology file, which can then be reused for other designs of similar structure to further reduce cycle time on future designs. Substrate suppliers can provide tech files that typically contain critical design rules to help drive a correct design methodology. Multiple tech files can be used from different suppliers to ensure manufacturability at secondary suppliers.

## Wirebond and Flip-Chip Escape Patterns

As wirebond attach is still the most popular packaging method, Cadence IC package design technology is designed to provide fast, powerful, and flexible bondshell creation and editing. New ground-up, constraint-driven, automatic bondfinger array placement can be used with staggered die pads, multiple bond levels, multiple bondrings, and both symmetrical and non-symmetrical designs. Unique push-and-shove bondfinger editing enables extremely complex bondshells to be developed in minutes, delivering unparalleled capability and productivity. True wire profile support enables DFM-driven design using manufacturing-verified wire loop data. An included Kulicke & Soffa verified loop profile library ensures that wirebond patterns designed meet manufacturing signoff (see Figure 1). All this is supported by extensive wirebond rules and constraints that provide real-time design feedback. Wirebond-attached die flags and power/ground rings can be quickly created, edited, and optimized. Die flags can be wizard-driven and auto-created along with the power/ground rings, or can be imported through DXF. Powerful metal-shape editing tools allow rings to be customized, split, and assigned to multiple voltages with just a few mouse clicks. Interactive substrate routing and wirebond connections work intelligently through pad entry rules, any-angle pad exit routing, and wirebond finger stubs in either inward or outward direction stay aligned to bondfingers when the fingers are moved.

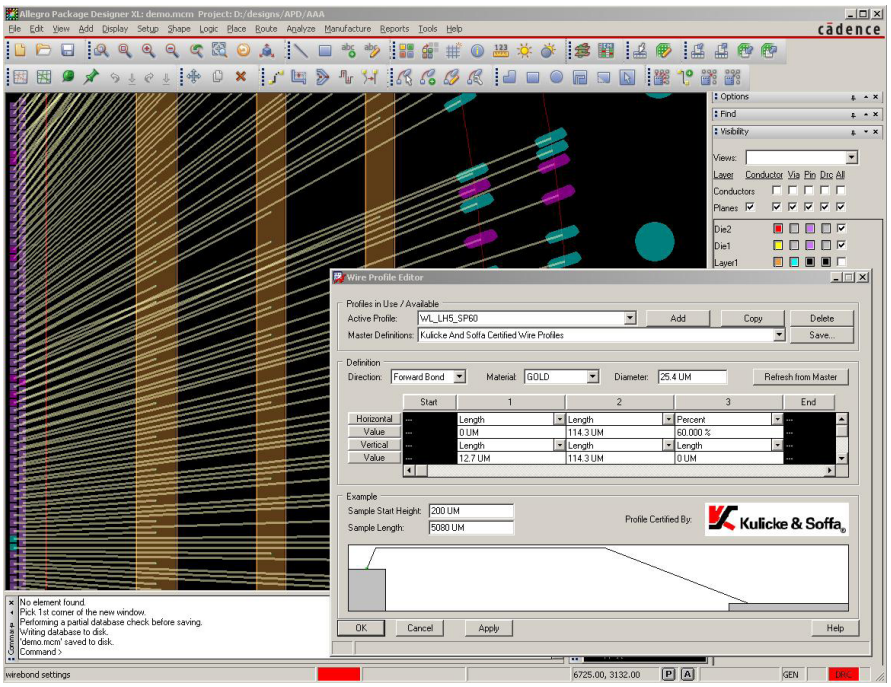


*Figure 1: Constraint-driven interactive wirebonding includes push-shove across multiple wire tiers. A 3D wireprofile viewer/editor allows for multiple wire profiles to be created and supported. An included Kulicke & Soffa-verified profile library enables manufacturing-aware design.*

For flip-chip technology, a proven set of tools assists the user in creating the complex routing escape patterns found in today's high-density designs. Both automatic and semi-automatic tools are included. Once the patterns are created, the designer can quickly propagate them around the die, creating either a full-custom or pattern-repeat breakout.

## Automatic Bump-To-Package Pin Assignment and Route Feasibility

Nearest-match, router-based, or constraint-driven algorithms determine best routable assignment based on existing design rules. Nets are assigned by layers based on net constraints and route channel availability. Differential pair-defined bumps are automatically assigned adjacent package pins accordingly. A net-per-layer assignment visualization tool also allows designers to visualize the completed assignment. Additional route planning can be done with flow designer technology that bundles net groups together (i.e. interfaces) and allows a route plan to be visualized.

## Interactive and Automatic Routing

Cadence IC package design technology integrates with Allegro PCB Router and SpiderRoute for interactive and automatic rules-based routing capabilities. The result is fast and accurate routing of any type of IC package design—whether an all-angle,

single-layer, wirebonded design with a plating bar, or a flip-chip on a multi-layer build-up substrate—with both interactive and automatic routing (see Figure 2). Route smoothing technology helps to quickly create manufacturing-quality interconnect.

### High-Density Interconnect (HDI) Design

HDI or build-up layer technology is pervasive in almost all IC package design using routable organic substrates and fine-pitch flip-chip devices. All levels of Allegro Package Designer and Allegro Package SI have comprehensive constraint-driven HDI design capabilities linked to automation-assisted interactive design. Comprehensive micro-via class rules linked to auto-assisted via array creation and editing capabilities enable the designer to achieve desired design and productivity goals (see Figure 3).

### Design Partitioning

(Available with an XL license)

IC package designs are getting more complex, but few design teams are offered any additional schedule time to deliver these designs. Without an efficient way to partition a design, teams are forced to work around the clock on a single database to meet the schedule. Manual workarounds that address multi-user challenges are time- consuming, slow, and prone to error. Cadence design partitioning technology provides a multi-user, concurrent design methodology for faster time to market and a reduction in layout time. Using this technology, multiple designers working concurrently on a layout share access to a single database, regardless of team proximity. Designers can partition designs into multiple sections or areas for layout and editing by several design team members. The partitioning can be vertical (cake slice) or horizontal (layer based).

As a result, each designer can view all partitioned sections and update the design view for monitoring the status and progress of other users' sections. This can dramatically reduce overall design cycles and accelerate the design process.

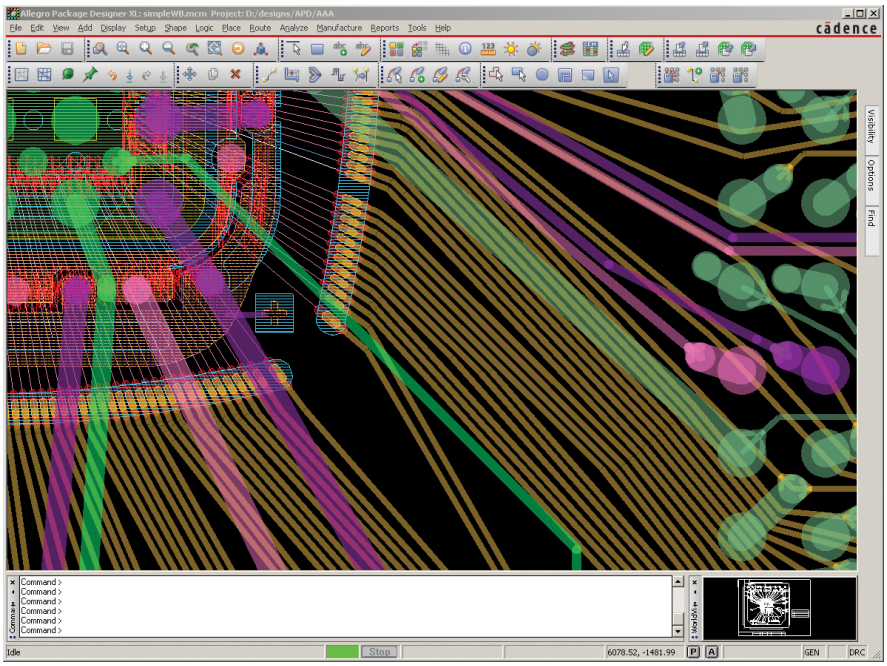


*Figure 2: SpiderRoute offers 45-degree or true any-angle routing and routability analysis that is ideal for wirebond attach substrates.*

### Assembly Rule Checking (ARC)

(Available with an XL license)

A comprehensive assembly and manufacturing rule checker provides more than 50 checks. Check can be executed as a check-group, individually, or as a custom selection. Check results appear in the Constraint Manager DRC tab and as graphical markers in the design.

### SiP Finishing

In preparation for manufacturing, Allegro Package Designer can open designs prepared with Cadence SiP Layout. Minor edits to the substrate and minor movements of wirebond wires (no adding or deleting wires) are allowed. This enables manufacturing preparation of SiP designs, but does not allow initial creation or major edits of SiP designs.

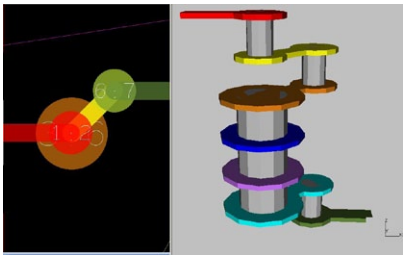

*Figure 3: Constraint-driven HDI design allows designers to rapidly implement complex via structures.*

### Extensive Manufacturing Output Capabilities

In preparation for manufacturing, a complementary set of manufacturing-specific creation utilities are available, including plating bar creation, etchback plating creation, metal-pour degassing, and metal layer balancing. All types of data likely to be required can be generated, from documentation to tooling. Users can easily create bond diagrams, dimension documents, format drawings, and various output files containing critical package data. Manufacturing output supports Gerber 4X00 and 6X00 series, 274X, Barco, DXF, AIF, and GDSII (see Figure 4).

Many package foundries currently use Cadence IC package design technology. This pervasiveness allows users to send an Allegro design database directly to the foundry as manufacturing input, greatly compressing throughput times and eliminating inaccuracies. The foundry can use the database to enhance manufacturing yields and implement any last-minute changes to the package without inadver-

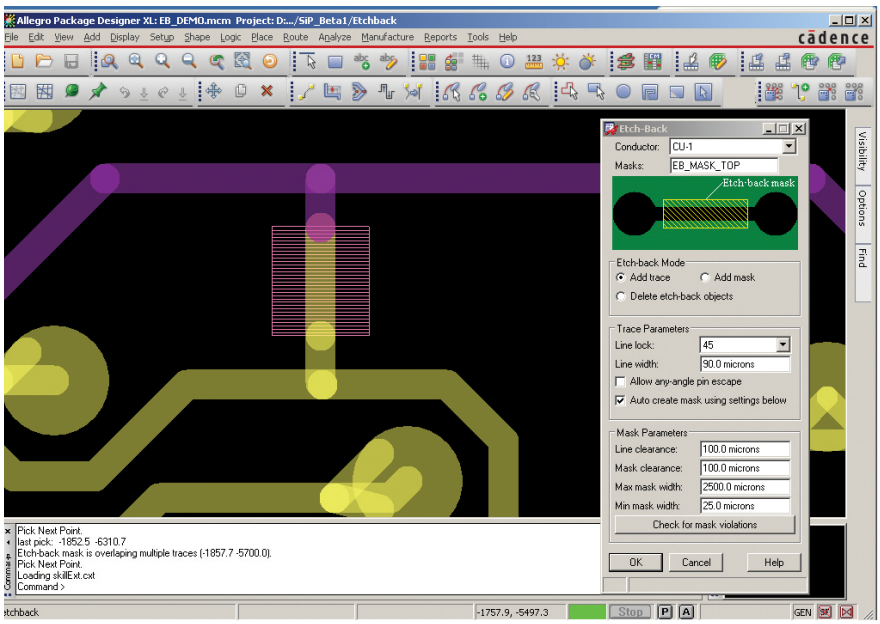


*Figure 4: Plating bar support includes intelligent recognition of etchback interconnect such that metal is made available to manufacturing output, but appropriately ignored with analyzing design data.*

tently compromising the original specifications. (Contact your foundry to confirm their specific capabilities.)

### PCB System-Level Handoff

Cadence IC package design technology not only bridges the gap between silicon and package design, but also links package and PCB design. All data required for PCB-level floorplanning and layout is automatically generated—physical footprint, schematic symbol, and device models in SPICE, IBIS, or Allegro PCB SI format. Also included is a symbol (die or BGA) export that can be read in spreadsheet tools such as Excel. These capabilities compress setup time and increase data accuracy for systems designers.

## Package Signal and Power Integrity Features

(Available in Allegro Package SI)

Allegro signal integrity (SI) for package design streamlines complex IC package virtual prototyping and interconnect exploration, analysis, and modeling. With its advanced substrate editing capabilities, powerful I/O buffer-to-I/O buffer system interconnect modeling, robust simulation engine support, and seamless integration with third-party 3D field solvers, it allows engineers to make tradeoffs among electrical and physical design requirements to meet cost and performance targets.

### Topology Exploration with SigXplorer

SigXplorer, a graphical interconnect topology editor and simulation module with proven solution space exploration for virtual system interconnect (VSIC) models, develops rules earlier in the design cycle to drive package and PCB design. It offers a graphical environment for exploring, analyzing, and defining VSIC models for interconnect implementation concept evaluation. Electrical engineers can explore different placement and routing strategies from an electrical standpoint and develop a comprehensive set of design rules, capture them as VSIC models, and reuse those models to efficiently author design intent. Pre-route topology exploration and solution space analysis for single-ended nets or differential pairs is provided. Constraint-driven design is enabled through the creation of electrical rules that drive package design. Embedded simulation capability provides time and frequency domain interconnect simulation, including industry-standard S-Parameter models. With SigXplorer, designers have an electrical view of the routed interconnect that aids in post-layout verification and debugging (see Figure 5).

### Sufficient and Efficient Power Delivery

A properly designed package power delivery network (PDN) ensures that sufficient power is delivered to the IC as efficiently as required. However,

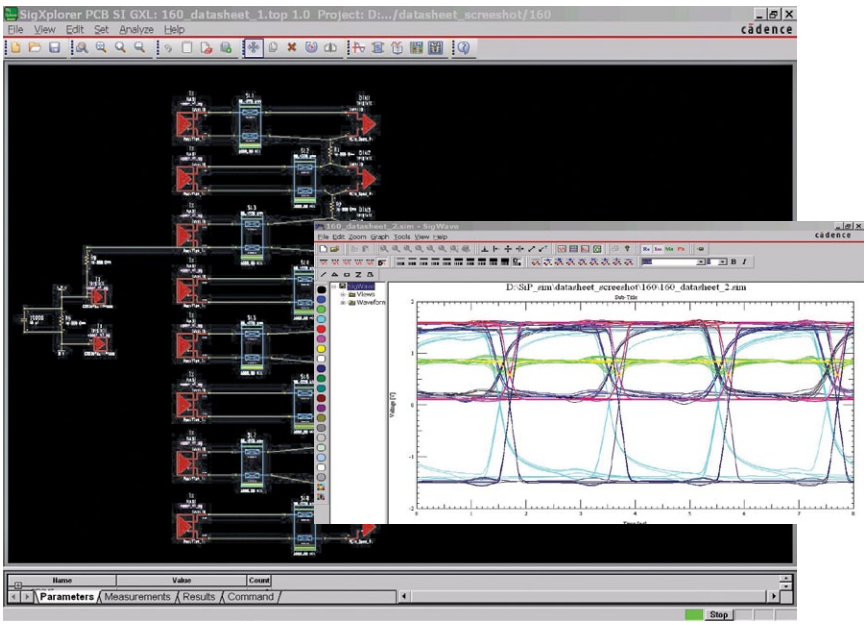


*Figure 5: Topologies can be manually created or automatically extracted into SigXplorer from package design data. From within the SigXplorer environment, "what if" scenarios can be run to determine the optimal package design.*

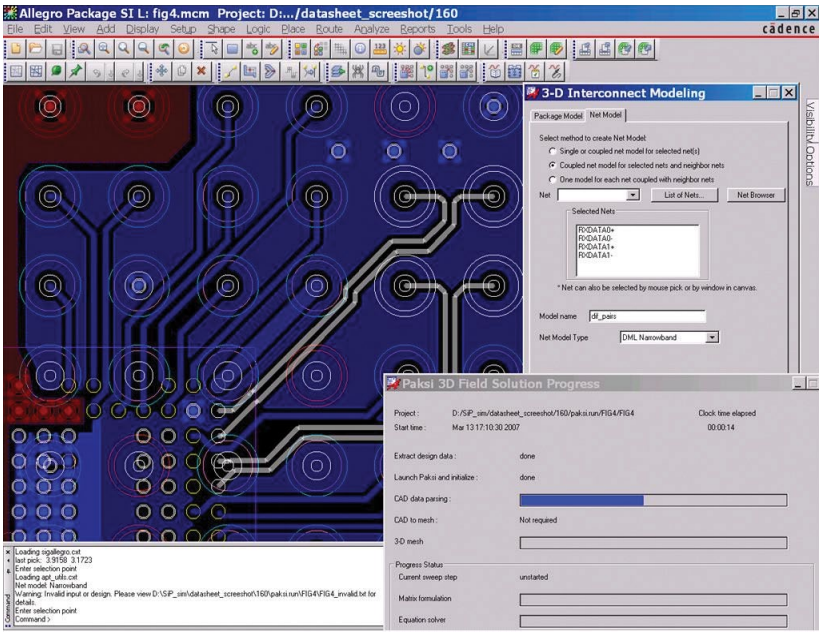


*Figure 6: Post-route interconnect can be extracted and modeled using an embedded third-party 3D field solver technology, and then explored and debugged to identify performance problem areas.*

design tradeoffs may have adverse effects on the PDN impedance. Power integrity (PI) analysis capabilities are available to ensure that efficient analysis of the PDN can verify that package power delivery goals are met.

### Power Stability

Stable power and ground rails are paramount to ensuring signal integrity in today's high-speed source-synchronous interfaces. As the signal speeds increase, voltage swings are decreasing, which in turn makes signals much more susceptible to any voltage ripple.

### SPICE-Based Simulation Subsystem and Embedded 3D Field Solver Engine

Embedded integration with third-party–supplied 3D field solvers allows users to focus on design and not the complexities of tool interfaces and design translation. It eliminates time-consuming design setup and time wasted on difficult-to-use standalone field solver and analysis tools. Users can output IBIS, RLGC, S-Parameter, or Cadence DML models for a select set of nets or the entire package (see Figure 6).

Other features include:

- Wideband or narrowband frequency models
- 2-port RLC model creation of power rails for IC core dynamic IR drop analysis using Cadence Encounter® Power System power analysis
- Grouped-port models for reduced model creation time, model size, and simulation runtime
- SigWave for comprehensive simulation results display, including FFT and eye diagrams
- Simulation support for IBIS, Cadence DML, Spectre®, and HSPICE models (HSPICE license required)
- Detailed simulation reports for flight time, overshoot, and noise margins

### Integrated Constraint Management

Integration with the Allegro Package Designer Constraint Manager provides a hierarchical, spreadsheet-like interface that allows users to ensure package design is progressing according to design intent. It manages tasks such as matched lengths, phase control for differential pairs, impedance, or delay rules (see Figure 7).

### Design Link

The Design Link feature provides interconnect analysis from die-to-die to connect IC packages to the PCBs they are intended to drive—great for ICs that target existing PCBs/backplanes.

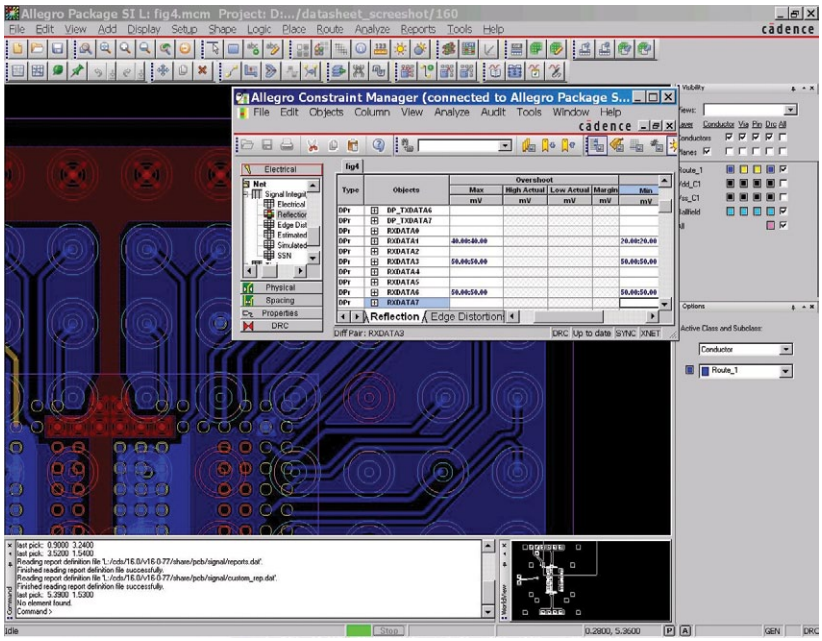


*Figure 7: Comprehensive substrate physical virtual prototyping allows the engineer to evaluate the effects of physical design changes to signal integrity and signal performance.*

### Floorplanning

A subset of Allegro Package Designer, substrate editing capabilities provide a virtual prototyping environment where engineers make changes to the design and evaluate performance impacts. This environment can also be used for post-layout detail debugging.

## 3D Design Viewer Features

(Enabled with an XL license or with an L license plus a 3D viewer license; view the Cadence 3D Design Viewer datasheet for more information)

The Cadence 3D Design Viewer is a full, solid model 3D viewer and 3D wirebond DRC solution for complex IC package designs. It allows users to visualize and investigate an entire design, or a selected design subset, such as multiple wirebond tiers with multiple wirebond profiles. It provides a common reference point for cross-team design reviews (see Figure 8).

### Intelligent 3D Design Viewing

Virtually all of today's technologies for fabric physical layout—IC, package, or PCB—are two-dimensional. While ideal for substrate layout, interconnect planning, and metal fill creation, this "plane-view" process does not lend itself well to the design, management, or verification of complex die stack towers/3D integration. The design complexity and density involved require a more realistic approach. The Cadence 3D Design Viewer meets this need by providing an IC package designer with the ability to physically visualize a design as it will actually look during manufacture. A designer can interactively zoom, pan, and rotate the 3D view as well as select from a set of pre-defined views.

### Interactive Markup

During 3D design viewing, an engineer can create "markup" jpeg snapshots for design reviews and/or design documentation that include the ability to add basic shapes, arrows, and text. This is especially useful for communications with design chain partners and test and assembly manufacturing departments.

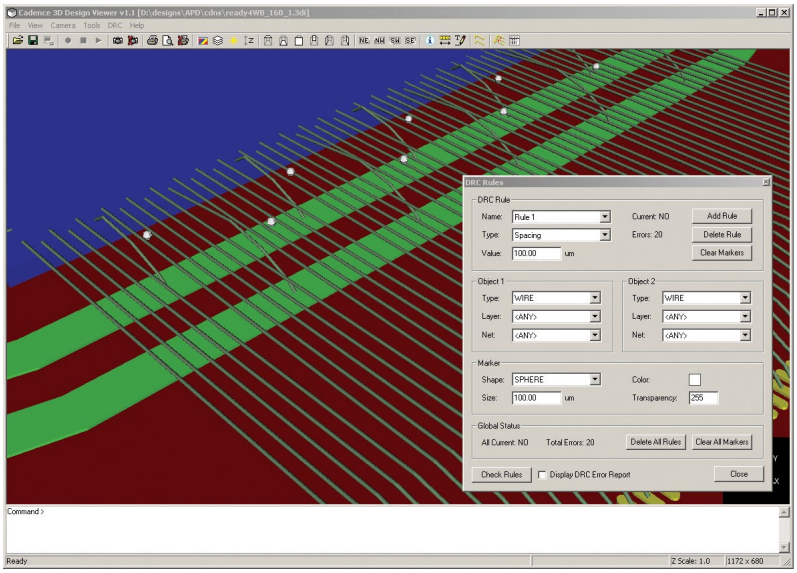


*Figure 8: Cadence 3D Design Viewer.*

### 3D Wirebond Clearance Design Rule Checking

Rules are defined and stored as part of the Allegro Package Designer design session. Completely user-defined, these rules can be used to check the following 3D clearances:

- All signals to all signals, all signals to named signal, or named signal to named signal
- Bondwire to bondwire, same bond tier, or tier 'n' to tier 'n'
- Bondwire to bondfinger, same bond tier, or tier 'n' to tier 'n'
- Bondwire to metal route, metal filled shape or die/spacer body on the same layer, or any adjacent layer

## Operating System Support

- Sun Solaris
- Linux
- IBM AIX
- Windows

## Cadence Services And Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

## Cadence IC/Package Design Feature Summary

| | Allegro Package Designer L | Allegro Package Designer XL* | SiP Layout XL* | Allegro Package SI L | Allegro Package SI XL** | SiP Digital SI XL** |
|---|---|---|---|---|---|---|
| Create/edit .mcm files | • | • | | • | • | |
| Finish .sip files (limited substrate edits only) | • | • | | • | • | |
| Create/full edit of .sip files | | | • | | | • |
| **Signal Integrity** | | | | | | |
| SigXplorer topology editor and simulator (pre-route) | | | | • | • | • |
| SigXplorer topology editor and simulator (pre- and post-route) | | | | • | • | • |
| S-Parameter interconnect modeling and SI simulation | | | | • | • | • |
| Source-synchronous bus simulation | | | | • | • | • |
| 3D PCB full-package simulation model creation | | | | • | • | • |
| Embedded integration with a third-party 3D field solver | | | | • | • | • |
| Co-planar coupling extraction | | | | • | • | • |
| Spectre transistor-level simulation engine | | | | • | • | • |
| Channel analysis for high-capacity SI simulation | | | | | | • |
| PDN optimization and verification | | | | • | • | • |
| Etchback stub effects simulation | | | | • | • | • |
| Package/pin delay length report | | | | • | • | • |
| **Substrate Design** | | | | | | |
| Constraint Manager (electrical/physical, DRC) | • | • | • | • | • | • |
| Import/export Allegro Package Designer (.mcm) database | • | • | • | • | • | • |
| Interactive and automatic component (packaged, bare die) placement | • | • | • | i/a only | i/a only | i/a only |
| Auto/interactive wirebonding including rapid auto-bond | • | • | • | | | |
| User-definable wirebond model profiles including XML import | • | • | • | | | |
| Full and partial design connectivity assignment and optimization (router based, closest match, interactive, constraint-based) | • | • | • | | | |
| Interactive and automatic interconnect routing (free-angle, multi-layer orthogonal) | • | • | • | | | |
| Online soldermask checking | • | • | • | | | |
| Recursive breakout pattern creator (flip-chip, wire-bond) | • | • | • | | | |
| **Advanced Design** | | | | | | |
| Hierarchical GDSII output | • | • | • | | | |
| Team-based design (design partitioning) | with legacy (16.2) DP Option | • | • | | | |
| Embedded component placement | • | • | • | | | |
| 3D Design Viewer and 3D wirebond DRC | with 3D Design Viewer license | • | • | with 3D Design Viewer license | • | • |
| Interconnect cline spreading | • | • | • | | | |

| | Allegro Package Designer L | Allegro Package Designer XL* | SiP Layout XL* | Allegro Package SI L | Allegro Package SI XL** | SiP Digital SI XL** |
|---|---|---|---|---|---|---|
| Interface Flow Planning | view only | • | • | view only | view only | view only |
| Symbol (die / BGA) editor | • | • | • | • | • | • |
| Constraint-driven HDI design | • | • | • | • | • | • |
| 3D die stack editor | | | • | | | • |
| Support for multiple die stacks | | | • | | | • |
| Enhanced die stack wirebonding | | | • | | | |
| DFM Preparation/Output | | | | | | |
| Die/BGA footprint compare using DEF/OA/.TXT | • | • | • | | | |
| Filled shapes (metal) creation and editing | • | • | • | • | • | • |
| Design documentation (dimensioning, annotation) | • | • | • | | | |
| Assembly rule checking (ARC) system | | • | • | | | |
| Etchback of plating traces | • | • | • | | | |
| Plating bar generation | • | • | • | • | • | • |
| Manufacturing/documentation export/import (stream, dxf, AIF) | • | • | • | | | |
| Substrate mask output (Gerber, GDSII) | • | • | • | | | |
| Full design-status reporting | • | • | • | • | • | • |
| Waived DRCs (creation and reporting) | • | • | • | • | • | • |
| Degassing of filled metal shapes | • | • | • | | | |
| Thieving (metal area balancing) | • | • | • | | | |

** The XL product license that enables this technology is from Cadence SiP Layout XL*

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Cadence is transforming the global electronics industry through a vision called EDA360. With an application-driven approach to design, our software, hardware, IP, and services help customers realize silicon, SoCs, and complete systems efficiently and profitably. www.cadence.com