

$$\frac{\partial}{\partial t}(\rho\phi) + \text{div}(\rho\vec{V}\phi - \Gamma_{\phi}\text{grad}\phi) = S_{\phi}$$

CAD integration

Temperature-Aware Design of Printed Circuit Boards

Co-design of PCBs for electrical, mechanical and thermal engineers

Based on EDA Design for Manufacturing Flows

CDNLive 2007

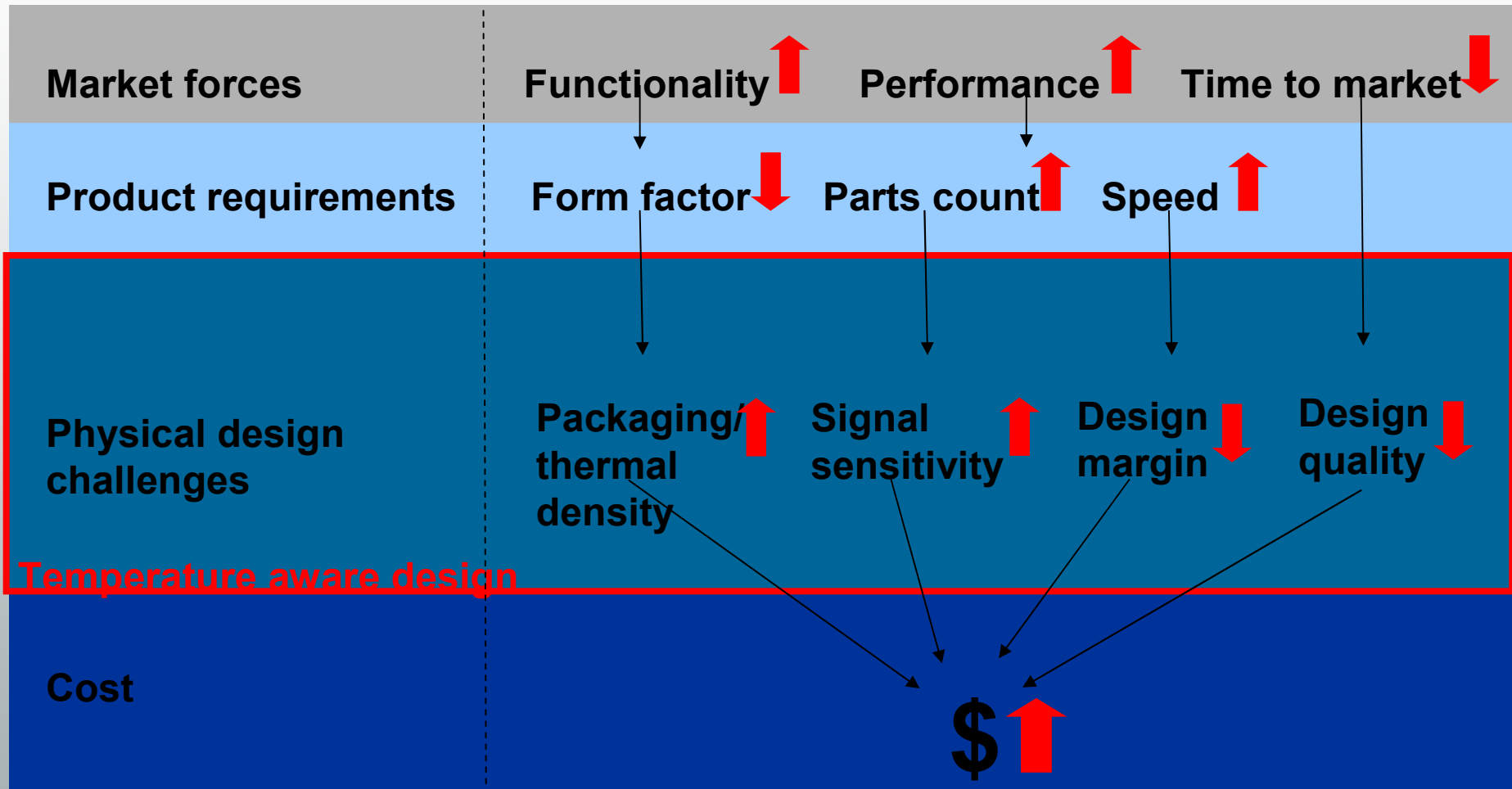
Dirk Niemeier
Support Manager
Flomerics Ltd.

AGENDA

- ▶ Drivers for temperature - aware design
- ▶ Impact on PCB design
- ▶ Making the Allegro design flow temperature - aware
- ▶ Case Study
- ▶ Summary & Conclusions

$$\frac{\partial}{\partial t}(\rho\phi) + \text{div}(\rho\vec{V}\phi - \Gamma_{\phi}\text{grad}\phi) = S_{\phi}$$

Drivers for Temperature Aware Design



$$\frac{\partial}{\partial t}(\rho\phi) + \text{div}(\rho\vec{V}\phi - \Gamma_{\phi}\text{grad}\phi) = S_{\phi}$$

CAD integration

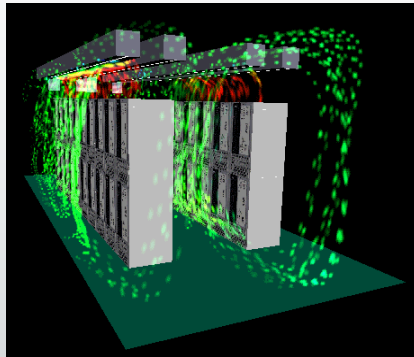
Product Requirements

- ▶ **Designs are complex**
 - High transmission speeds
 - High PCB layer count
 - High pin count ASICs
 - Embedded passives
 - Daughter cards
 - Extensive heat sinking
- ▶ **Design margins are small, risk is high**
 - Performance, reliability are compromised
 - 80-90% of nets are constrained, restricting component placement
 - Heat sinks are large and complex, requiring placement flexibility
- ▶ **Design closure is difficult and costly**
 - Signal integrity, thermal & component placement requirements clash
 - Co-design is critical
 - Performance is being impacted

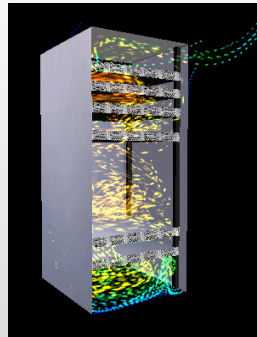
$$\frac{\partial}{\partial t}(\rho\phi) + \text{div}(\rho\vec{V}\phi - \Gamma_{\phi}\text{grad}\phi) = S_{\phi}$$

Physical Design Challenges: Five Year Thermal Density Trends*

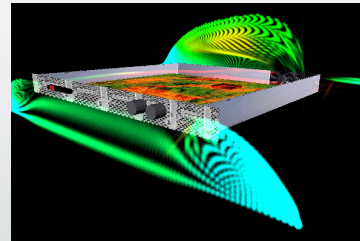
Datacenter



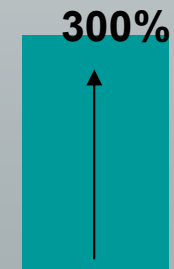
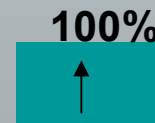
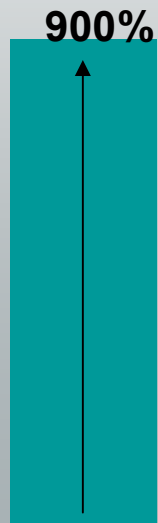
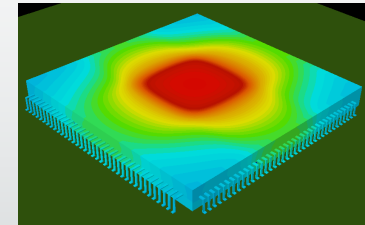
Rack



System/PCB

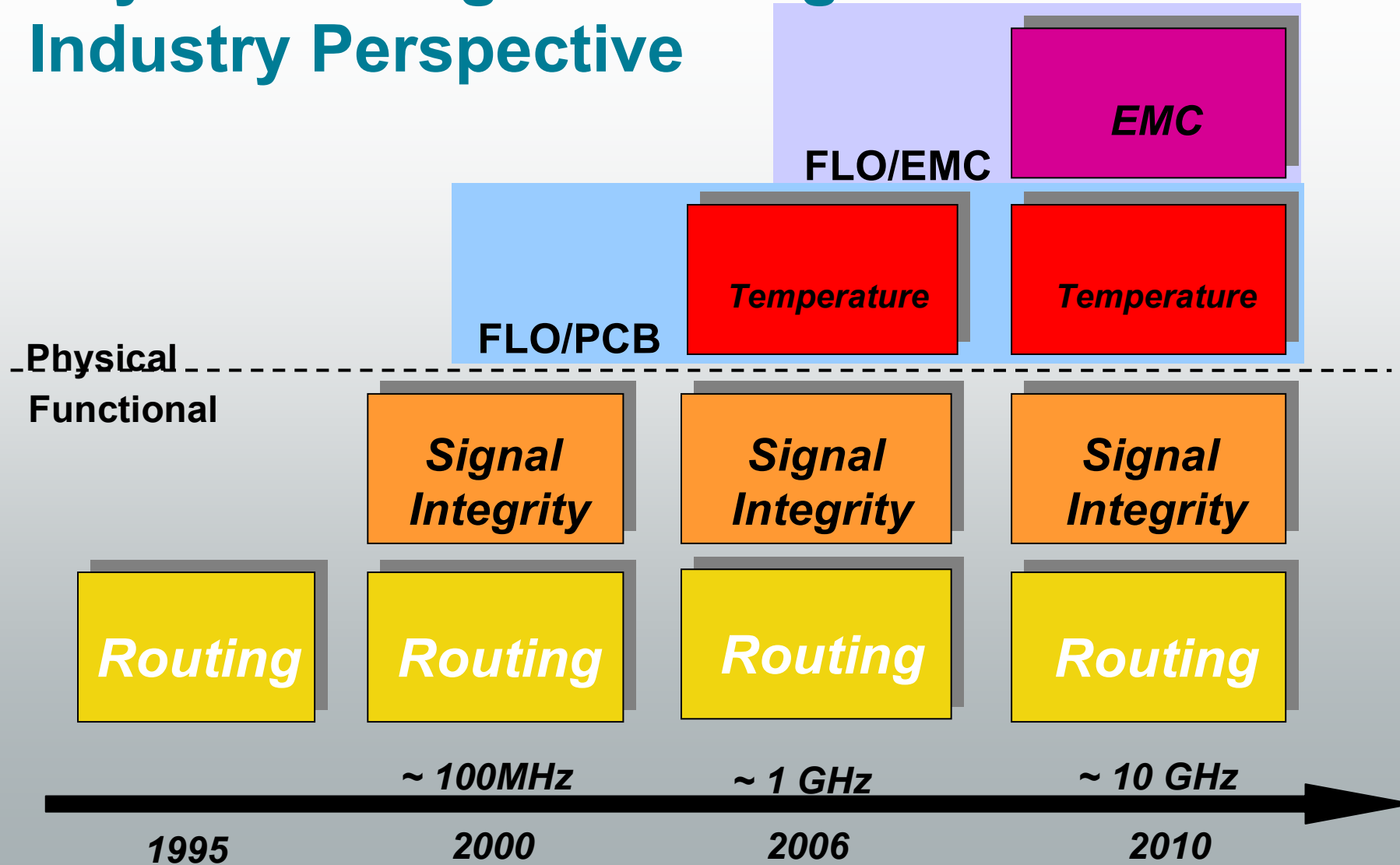


IC/package



*Flomerics customer survey data

Physical Design Challenges: Industry Perspective

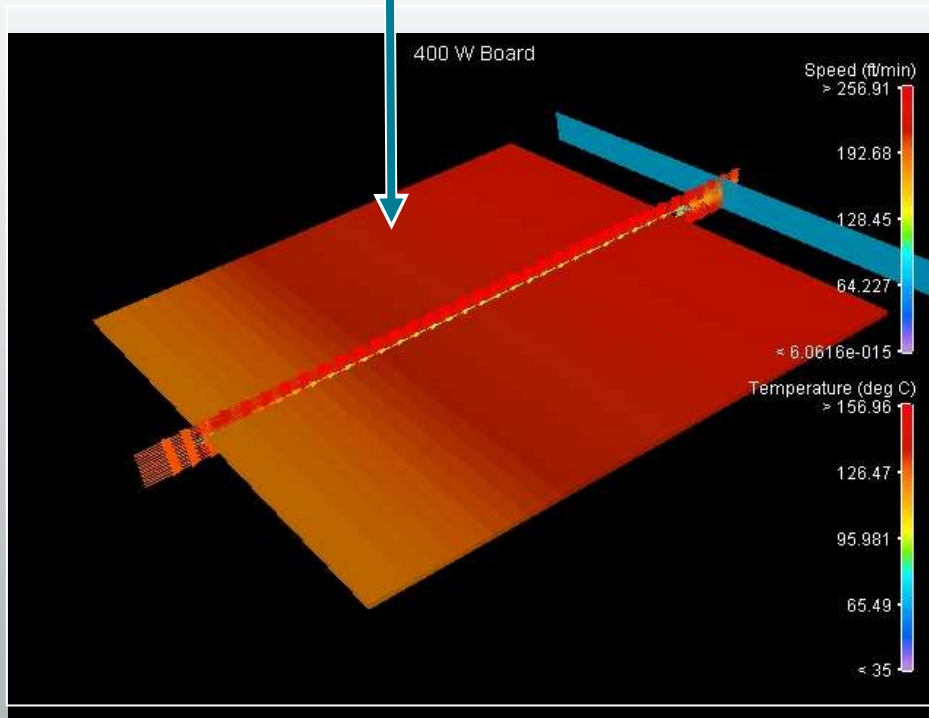


$$\frac{\partial}{\partial t}(\rho\phi) + \text{div}(\rho\vec{V}\phi - \Gamma_{\phi}\text{grad}\phi) = S_{\phi}$$

CAD integration

Physical Design Challenges

Components @ 120 °C



PCB at 1.5 W/in², 1 m/s

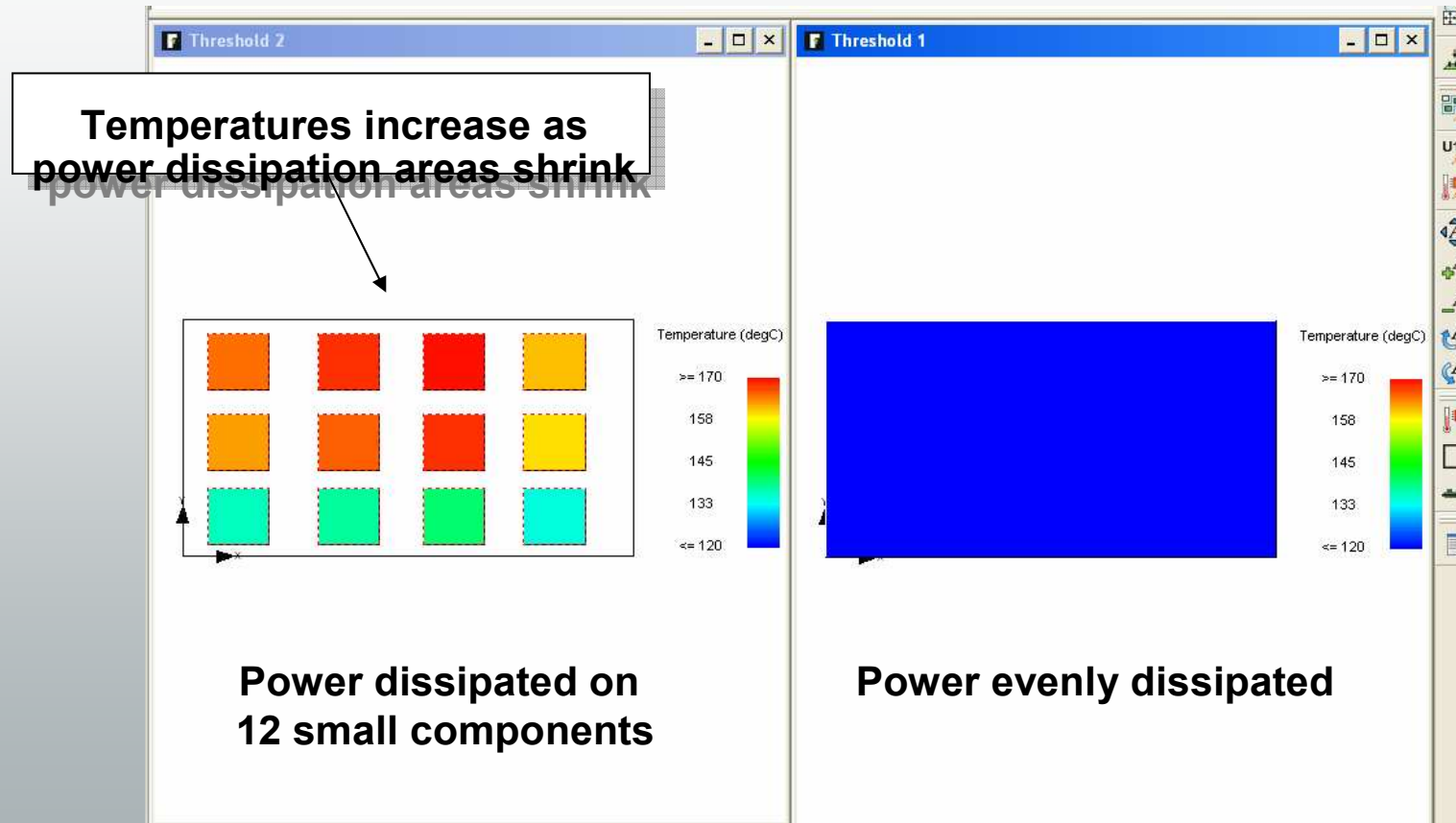
- PCB power densities are reaching 1.5 W/in² for high speed applications
- At this level, the PCB has reached its heat sinking limit
- Thermally unworkable designs are common
- 20% of Flomerics customers have reached this threshold and the percentage is rising
- The industry in general can see the approaching threshold

$$\frac{\partial}{\partial t}(\rho\phi) + \text{div}(\rho\vec{V}\phi - \Gamma_{\phi}\text{grad}\phi) = S_{\phi}$$

CAD integration

How Effective is a PCB as a Heat Sink?

15" x 8" PCB, 180 W, 1 m/s airflow

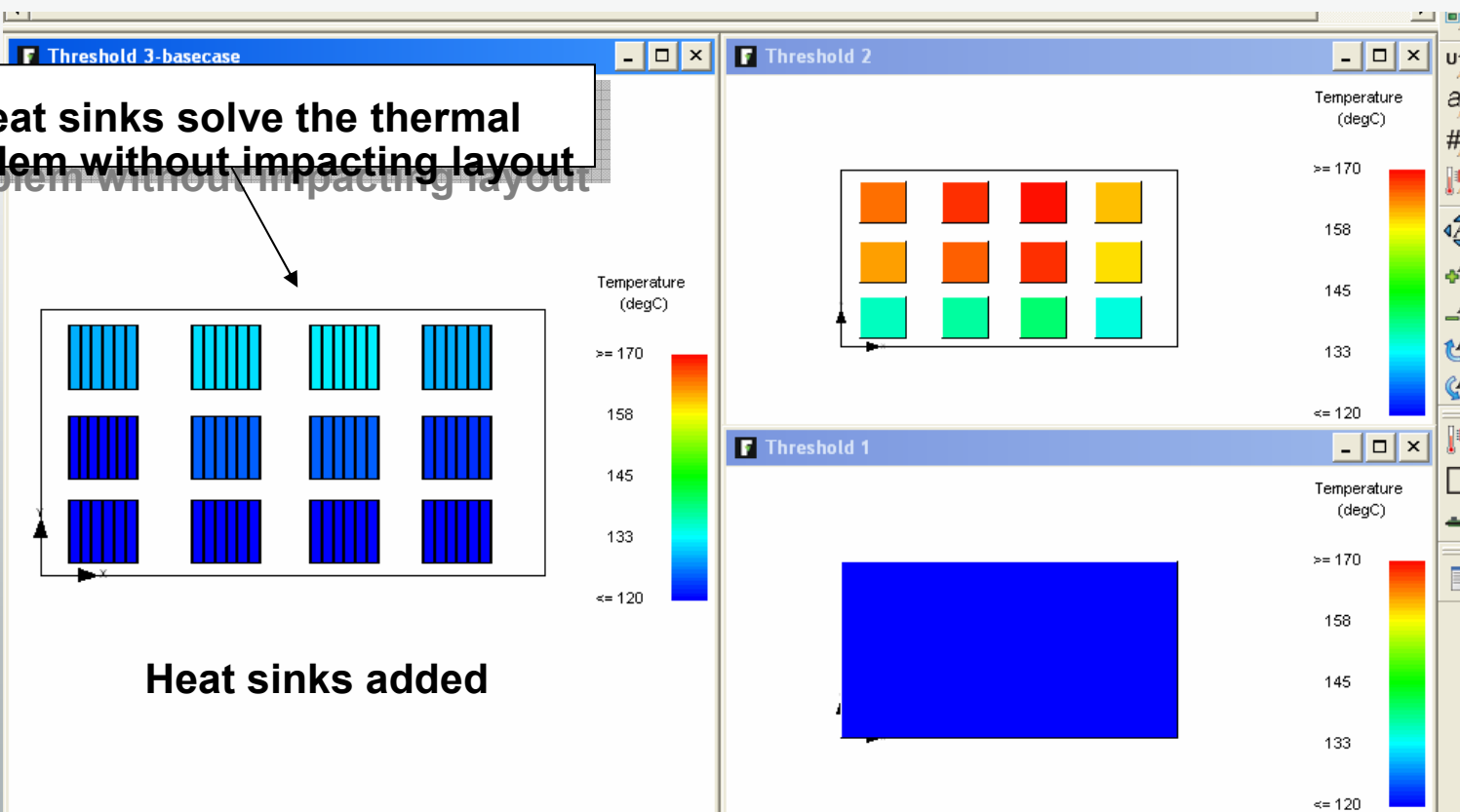


$$\frac{\partial}{\partial t}(\rho\phi) + \text{div}(\rho\vec{V}\phi - \Gamma_\phi \text{grad}\phi) = S_\phi \quad \text{CAD integration}$$

How Effective is a PCB as a Heat Sink?

15" x 8" PCB, 180 W, 1 m/s airflow

Heat sinks solve the thermal problem without impacting layout



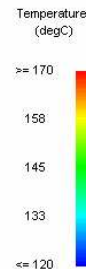
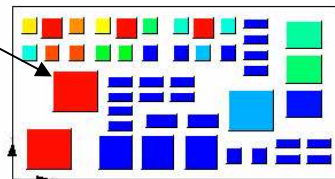
Heat sinks added

$$\frac{\partial}{\partial t}(\rho\phi) + \text{div}(\rho\vec{V}\phi - \Gamma_{\phi}\text{grad}\phi) = S_{\phi}$$

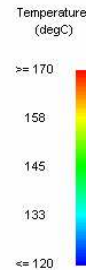
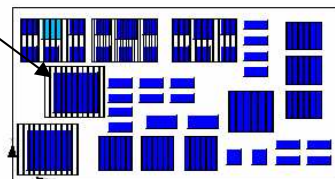
How Effective is a PCB as a Heat Sink?

15" x 8" PCB, 180 W, 1 m/s airflow

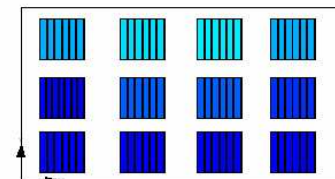
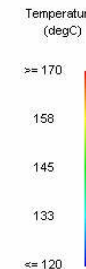
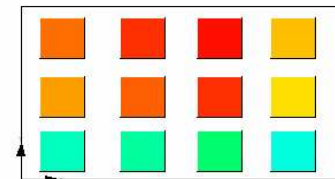
High temperatures due to high power density components



Heat sinking is to more complex



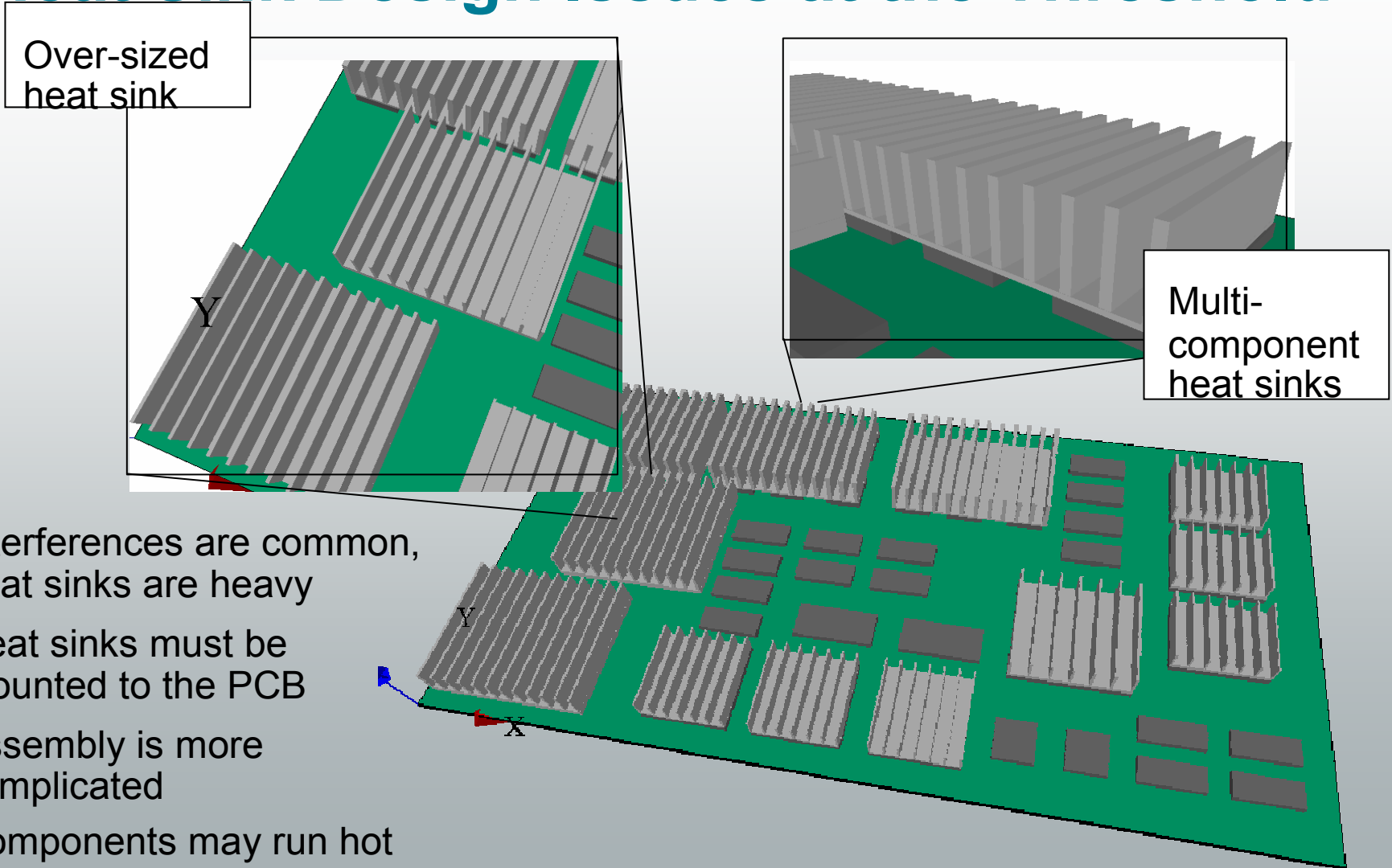
Real world PCB



Idealized PCB

$$\frac{\partial}{\partial t}(\rho\phi) + \text{div}(\rho\vec{V}\phi - \Gamma_{\phi}\text{grad}\phi) = S_{\phi}$$

Heat Sink Design Issues at the Threshold



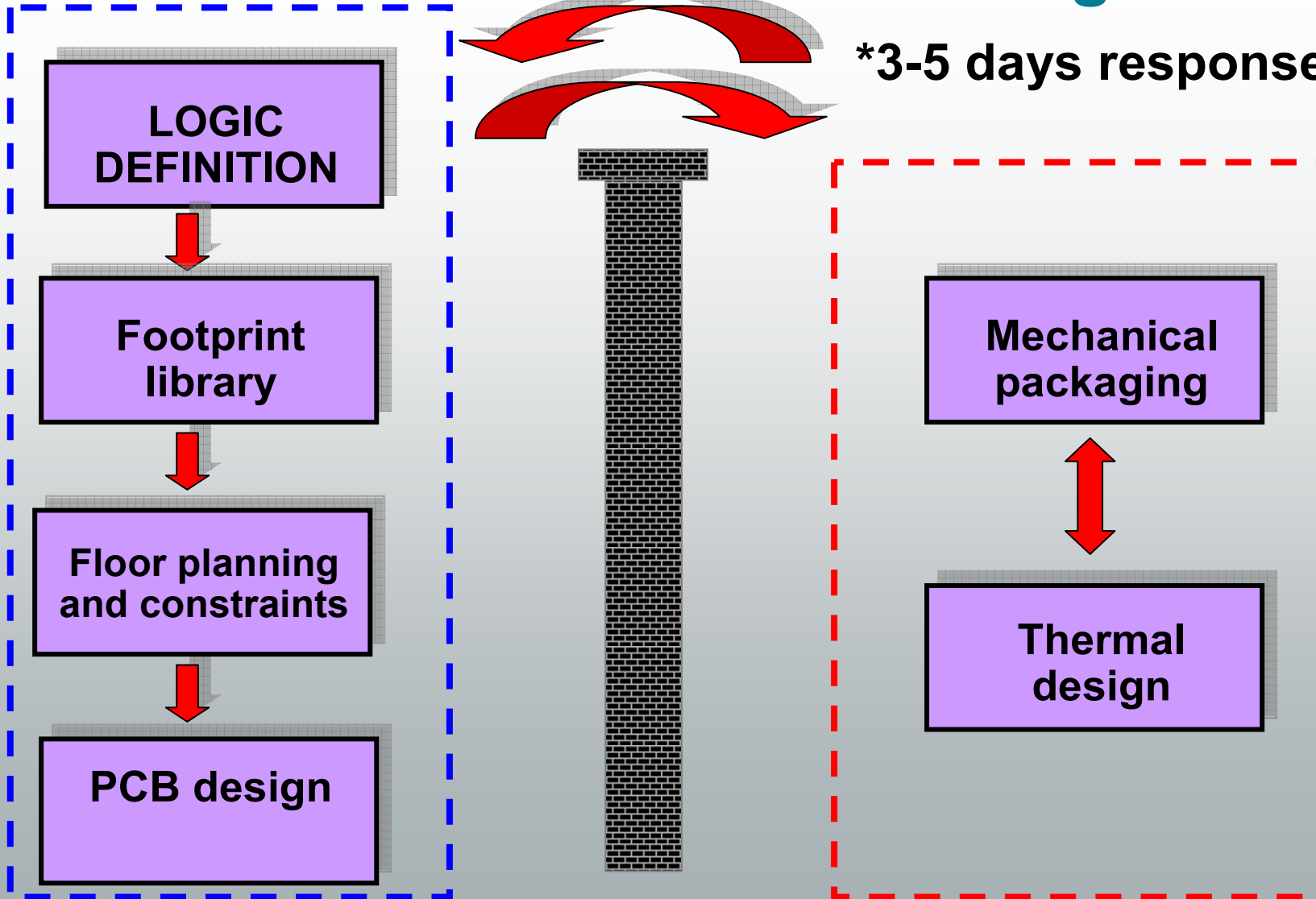
- Interferences are common, heat sinks are heavy
- Heat sinks must be mounted to the PCB
- Assembly is more complicated
- Components may run hot

$$\frac{\partial}{\partial t}(\rho\phi) + \text{div}(\rho\vec{V}\phi - \Gamma_{\phi}\text{grad}\phi) = S_{\phi}$$

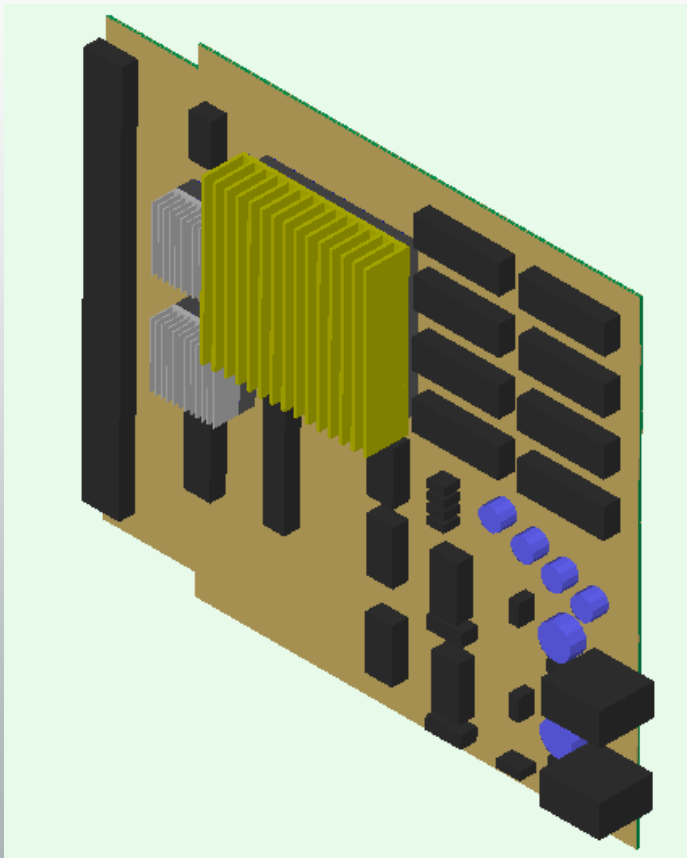
CAD integration

Traditional PCB Design

***3-5 days response time**



Traditional PCB Design

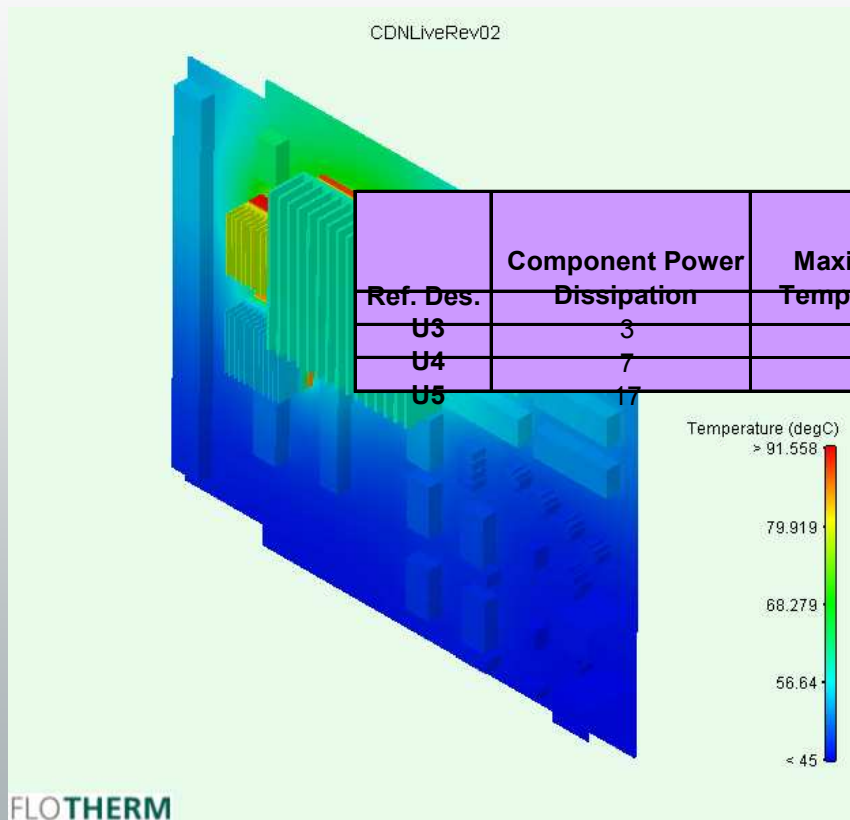


▶ Thermal Solution Design Requirements

- ▶ Junction temperature
- ▶ Shock and vibration
- ▶ Cost
- ▶ Mechanical fit
- ▶ Parts availability
- ▶ System level performance

$$\frac{\partial}{\partial t}(\rho\phi) + \text{div}(\rho\vec{V}\phi - \Gamma_{\phi}\text{grad}\phi) = S_{\phi}$$

Traditional PCB Design



► Attempt is made to meet cooling requirements by heat sinking based on design

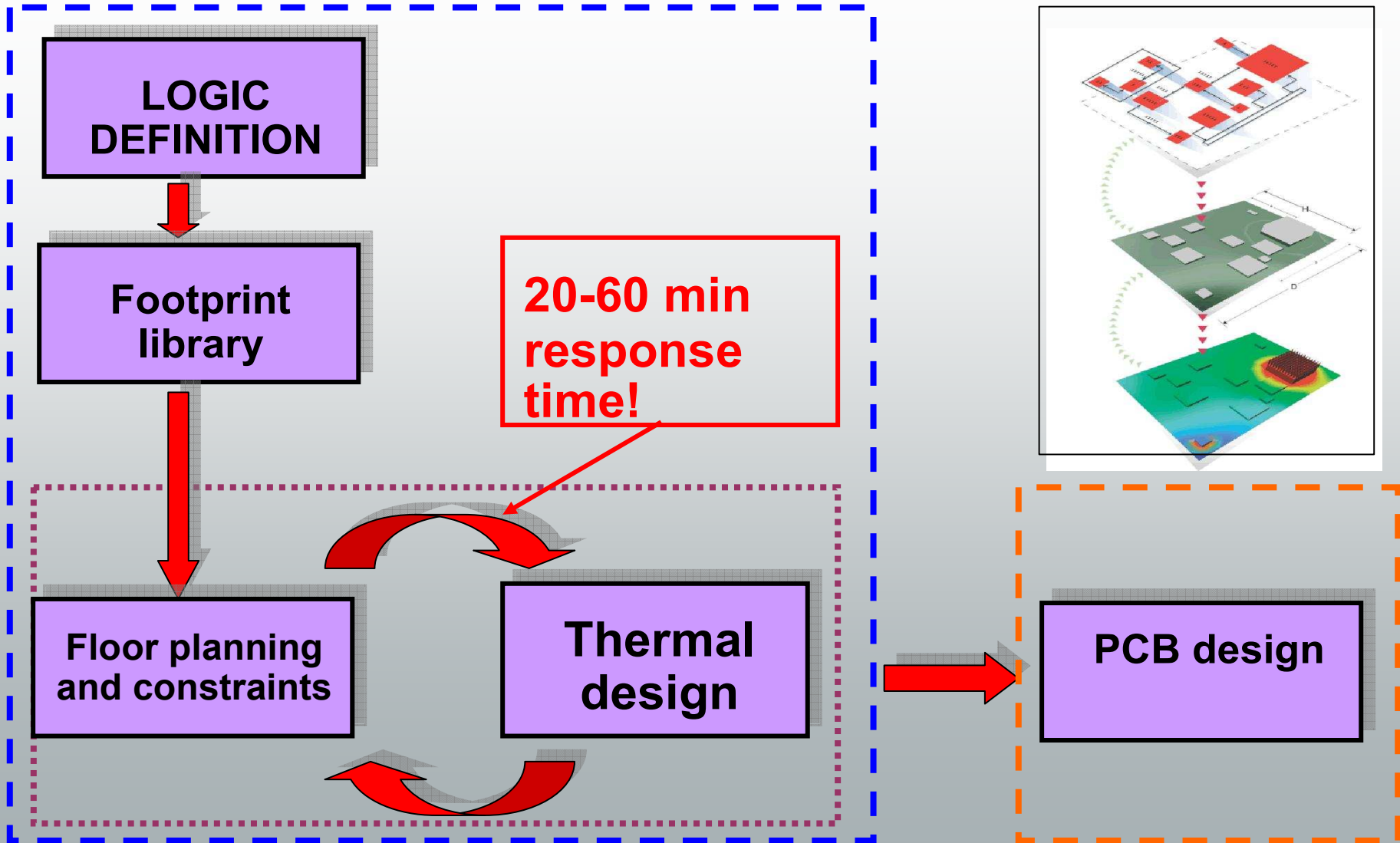
► Components cannot be operated at full estate problems

► Components are still operating above their required case temperature limit

► Use of Cu heatsink instead of cheaper, lighter heatsink (aluminum)

$$\frac{\partial}{\partial t}(\rho\phi) + \text{div}(\rho\vec{V}\phi - \Gamma_{\phi}\text{grad}\phi) = S_{\phi}$$

Temperature-Aware PCB Design



Temperature-Aware PCB Design

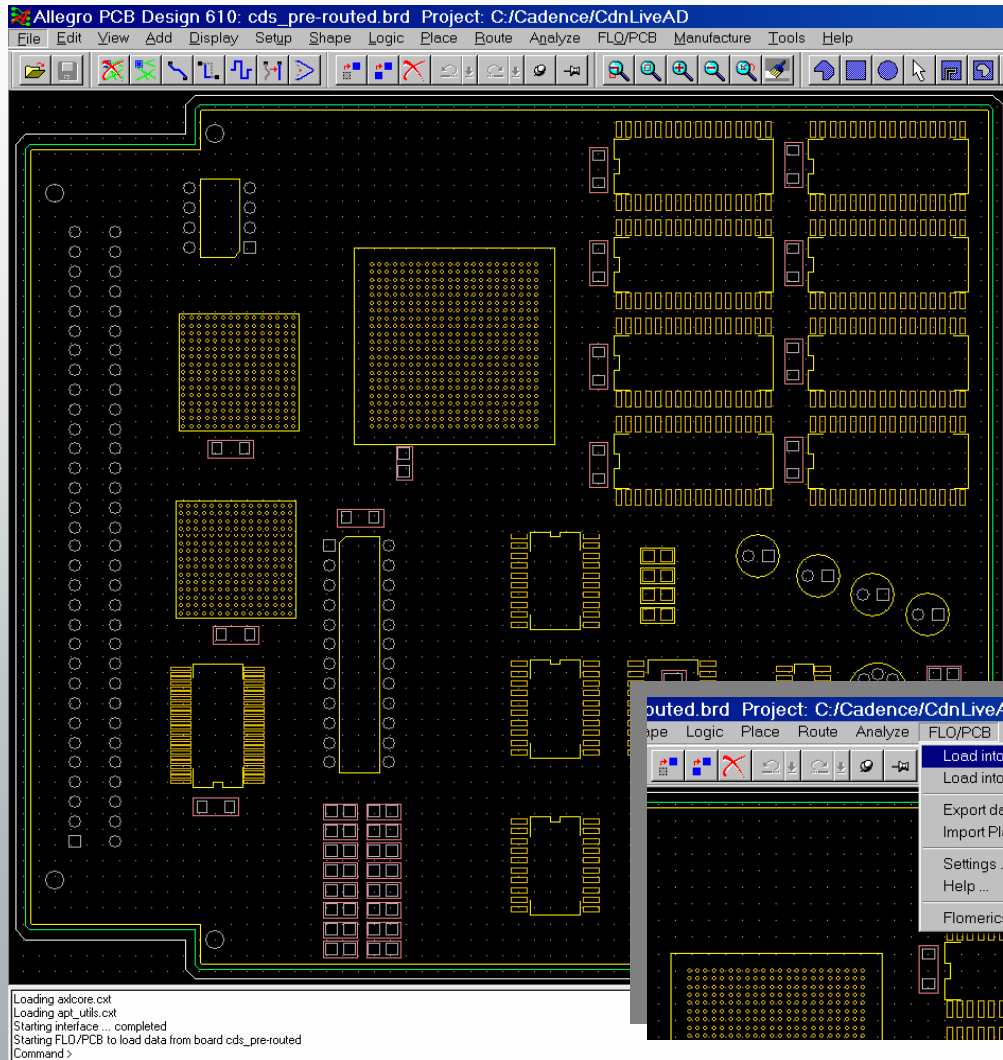
- ▶ Bi-directional model transfer
- ▶ High-degree of automation
 - Model transfer and filtering
 - Model-set up
 - Solver automation
 - Results viewing and interpretation
- ▶ Intuitive user control
 - Drag 'n Drop model modification
 - SmartParts
 - Intelligent modeling rules
 - Interactive 3D viewing
- ▶ The time to complete the loop from SI constraints to thermal design, back to SI constraints must be completed in minutes
- ▶ Traditional loop response time 3-5 days
- ▶ Temperature aware response time 20-60 minutes

$$\frac{\partial}{\partial t}(\rho\phi) + \text{div}(\rho\vec{V}\phi - \Gamma_{\phi}\text{grad}\phi) = S_{\phi}$$

Case Study of a Temperature-Aware Design Flow

$$\frac{1}{\sigma} (\rho \phi) + \text{div} (\rho \nabla \phi - \Gamma_p \text{grad } \phi) = S_p$$

SI Constraints -> Thermal Design



Allegro Constraint Manager (connected to Allegro PCB Design 610 15.5) - [Nets: Routing]

File Edit Objects Column View Analyze Audit Tools Window Help

Objects	Pin Delay		Prop Delay		Prop Delay	
	Pin 1	Pin 2	Min	Actual	Max	Actual
	mil	mil	mil		mil	
System						
cbs_pre-routed				722 MIL		-709 MIL
BD_BUS				722 MIL		-709 MIL
BD1				1309 ...		-689 MIL
BD2				1269 ...		-689 MIL
BD3						
BD4						
BD5						
BD6						
BD7						
BD8						
BD9						
BD10						
BD11						
BD12						
BD13						
BD14						
BD15				722 MIL		-122 MIL
BD16				722 MIL		-106 MIL
AFR						
AGRD						
AB						
A3						
A4						
A5						
A7						

Minimum allowable propagation delay/length for an object

► Constraints are set in Allegro PCB SI

► Launch thermal tool from within Allegro PCB SI

► Board Information, Component Footprints/Height etc are filtered and passed into FLO/PCB

$$\frac{\partial}{\partial t}(\rho\phi) + \text{div}(\rho\vec{V}\phi - \Gamma_{\phi}\text{grad}\phi) = S_{\phi}$$

SI Constraints -> Thermal Design

Component Filter Options

Combine Parameters By	Or	
Side Length Less Than	1	mm
Height Less Than	1	mm
Power Less Than	0	W
Power Density Less Than	0	W/m ²
Name Contains	Undefined	

Filter Delete Cancel Help

► Component filter allows for only the critical components to be passed

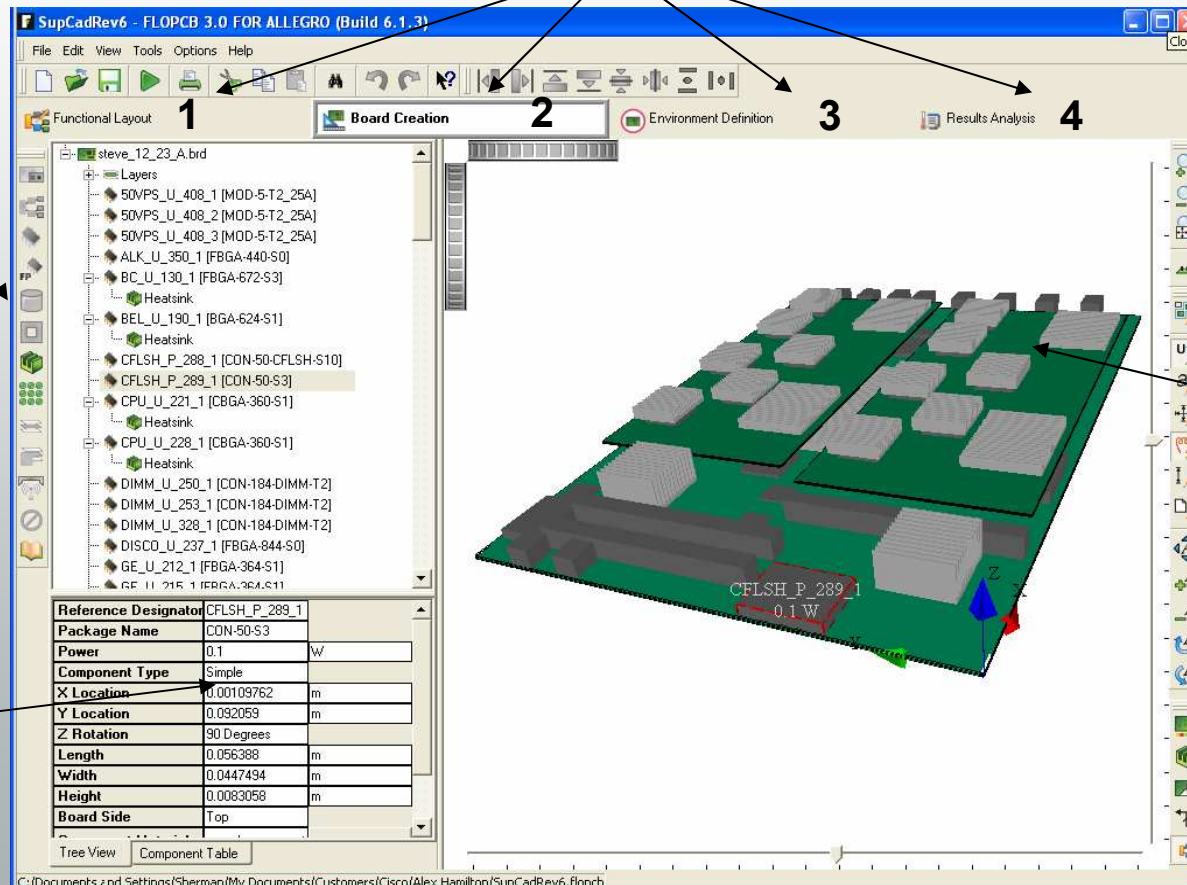
$$\frac{1}{\rho} \frac{d(\rho\phi)}{dt} + \text{div}(\rho\vec{V}\phi - \Gamma_{\phi} \text{grad} \phi) = S_{\phi}$$

FLO/PCB User Interface: Designed for Quick Thermal Verification

Four steps to model creation and analysis

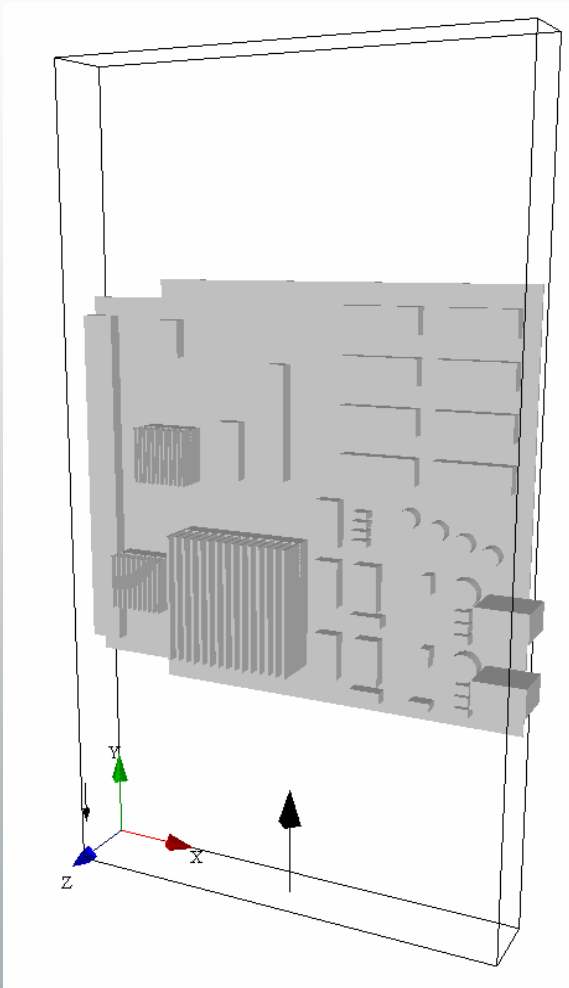
SmartParts

Property sheet input



3D model

Layout 1 Variant Definition



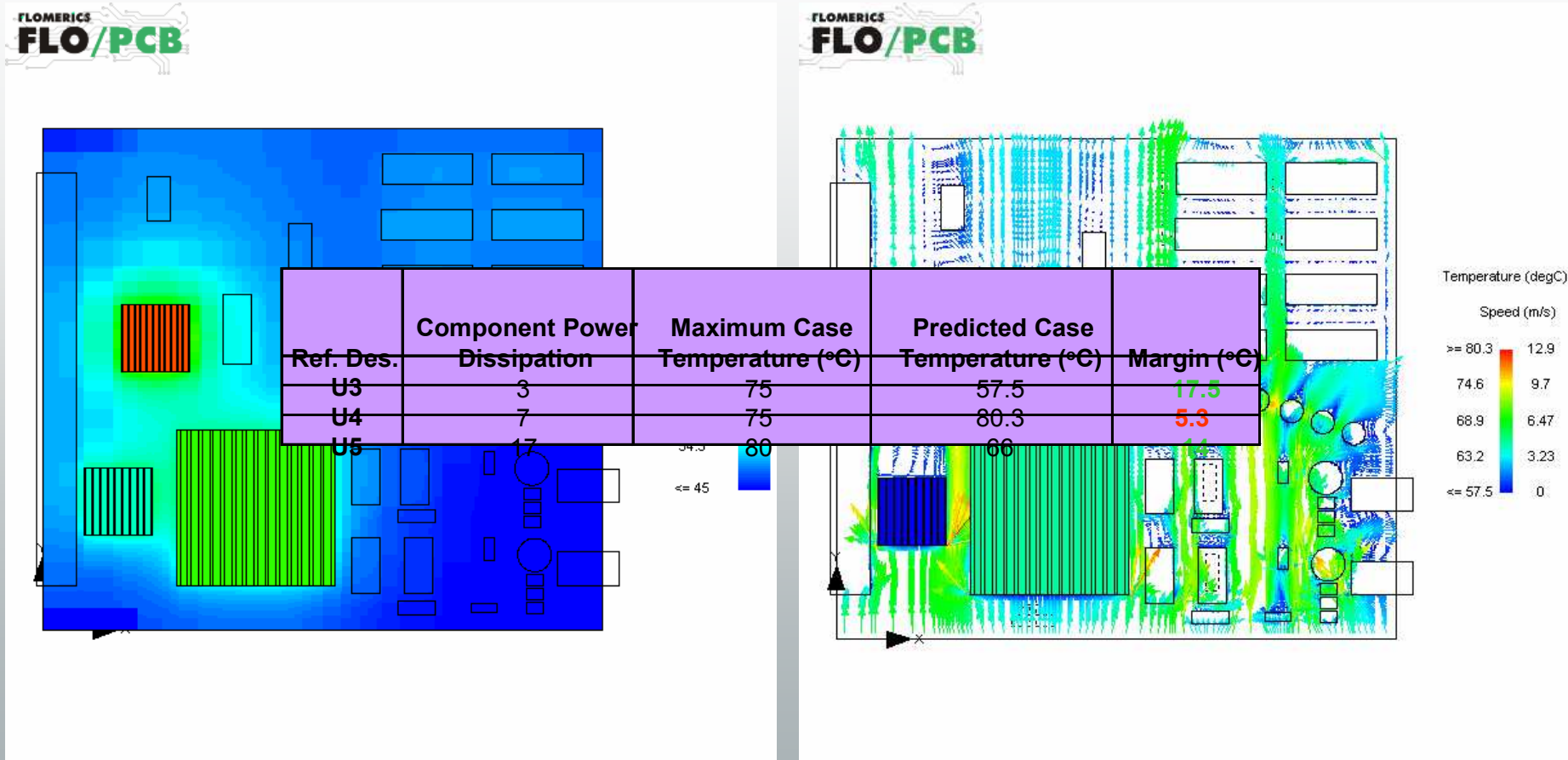
1. Heatsinks added to thermally critical components
 - Check mechanical fit
2. Proposed thermally optimized layout manually defined in thermal tool
3. Ensure that appropriate up-to-date power dissipation values are entered
4. Select the environment in which the design is to operate, e.g. card slot
5. Perform a thermal prediction and inspect results

Response time: 20 minutes!

$$\frac{\partial}{\partial t}(\rho\phi) + \text{div}(\rho\vec{V}\phi - \Gamma_{\phi}\text{grad}\phi) = S_{\phi}$$

CAD integration

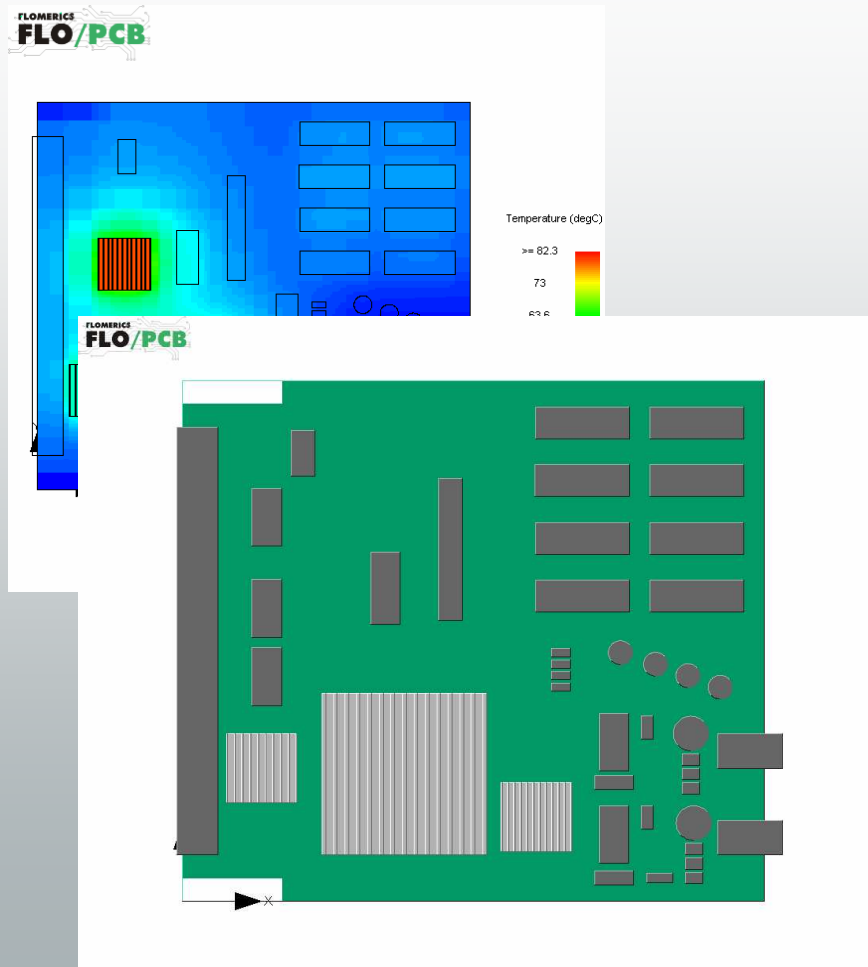
Layout 1 Variant Results



► Temperature Contour (thru the board)

► Velocity Contour (3 mm above board)

Layout 2 Variant



1. Critical component moved in an attempt to decrease its case temperature
 1. Check mechanical fit
2. All other settings retained
3. Perform a second thermal prediction!

Response time 10 minutes

$$\frac{\partial}{\partial t}(\rho\phi) + \text{div}(\rho\vec{V}\phi - \Gamma_{\phi}\text{grad}\phi) = S_{\phi}$$

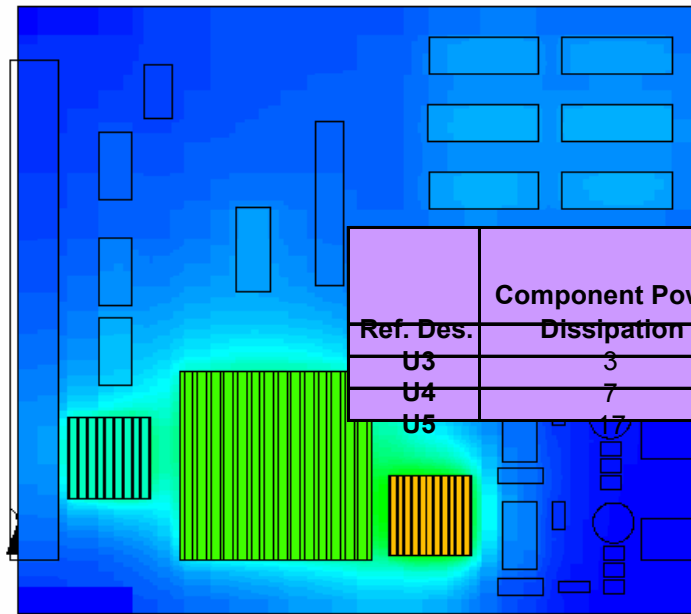
CAD integration

Layout Variants

- ▶ PCB properties
 - Layers
 - Copper patches
 - Material properties (Stablecor)
 - Thermal vias
- ▶ PCB layout
- ▶ Heat sinks
- ▶ Environmental conditions
 - Airflow
 - Air temperature

$$\frac{\partial}{\partial t}(\rho\phi) + \text{div}(\rho\vec{V}\phi - \Gamma_{\phi}\text{grad}\phi) = S_{\phi}$$

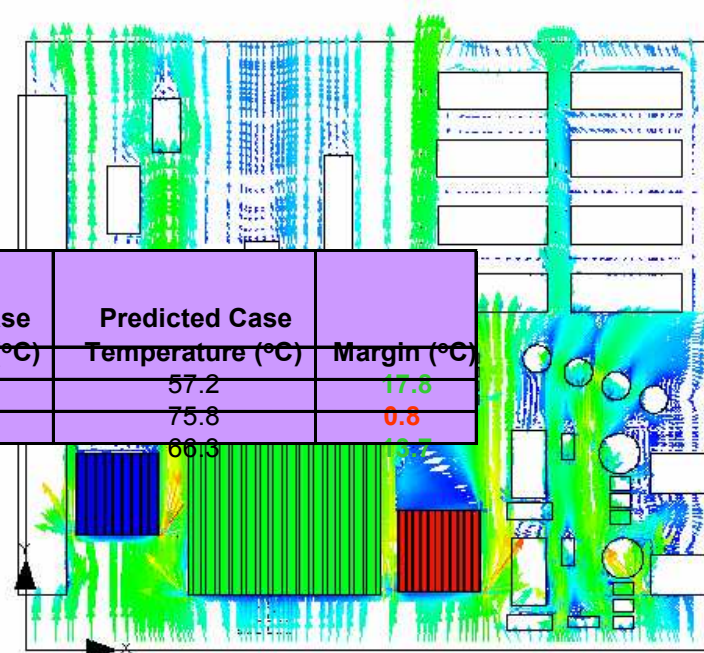
Layout 2: Results



Temperature (degC)

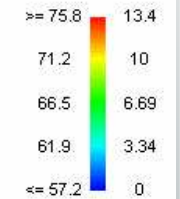
Ref. Des.	Component Power Dissipation	Maximum Case Temperature (°C)	Predicted Case Temperature (°C)	Margin (°C)
U3	3	75	57.2	17.8
U4	7	75	75.8	0.8
U5	17	80	66.3	13.7

<= 45



Temperature (degC)

Speed (m/s)



► Temperature Contour (thru the board)

► Velocity Contours (3 mm above board)

$$\frac{1}{\sigma} (\rho \phi) + \text{div} (\rho \vec{V} \phi - \Gamma_{\sigma} \text{grad} \phi) = S_{\phi}$$

Back Annotate the Proposed Design

Allegro PCB Design 610: cds_pre-routed_final.brd Project: C:/Cadence/CdnLiveAD

No Name - FLOPCB 3.0 FOR ALLEGRO (Build 5.50.2)

Allegro Constraint Manager (connected to Allegro PCB Design 610 15.5) - [Nets: Routing]

Objects	Pin Delay		Prop Delay		Prop Delay	
	Pin 1	Pin 2	Min	Actual	Max	Actual
System						
cds_pre-routed_final				606 nML		-2061 ...
BD_BUS				606 nML		-2061 ...
BD1				606 nML		-6 nML
BD2			300 nML	946 nML	900 nML	-946 nML
BD3			300 nML	946 nML	900 nML	-946 nML
BD4			300 nML	1472 ...	900 nML	-1472 ...
BD5			300 nML	1512 ...	900 nML	-1512 ...
BD6			300 nML	1851 ...	900 nML	-1851 ...
BD7			300 nML	1851 ...	900 nML	-1851 ...
BD8			300 nML	2818 ...	900 nML	-2818 ...
BD9			300 nML	2832 ...	900 nML	-2832 ...
BD10			300 nML	2875 ...	900 nML	-2875 ...
BD11			300 nML	2875 ...	900 nML	-2875 ...
BD12			300 nML	2984 ...	900 nML	-2984 ...
BD13			300 nML	2984 ...	900 nML	-2984 ...
BD14			300 nML	3648 ...	900 nML	-3648 ...

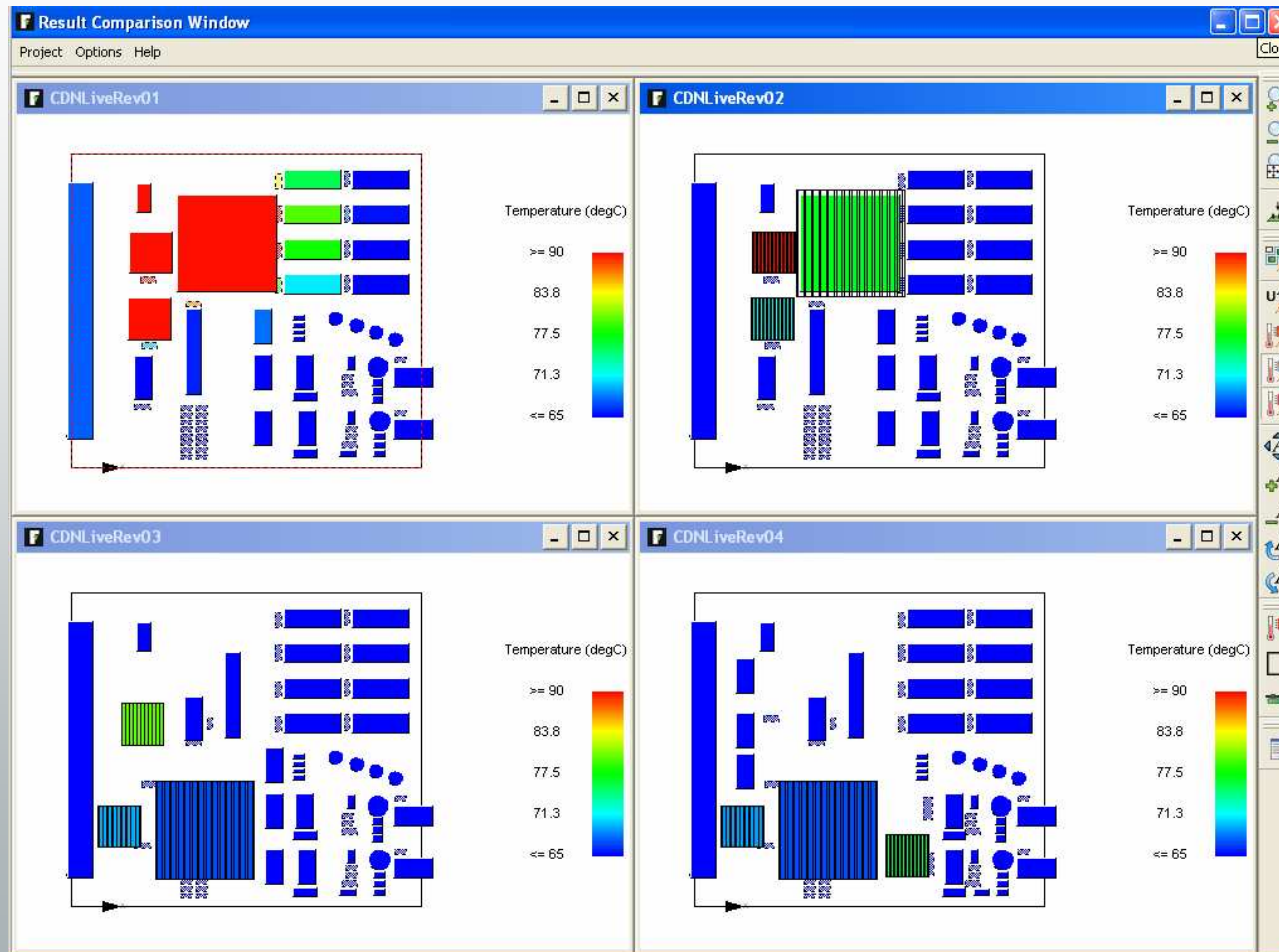
layout from thermal tool

- ▶ Multiple violations found by constraint manager
- ▶ SI rules must be revisited
- ▶ The new layout can then again be passed into thermal tool, automatically updating the existing model definition

Loading signal.cst
Performing a partial database check before saving.
Writing database to disk.
"cds_pre-routed_final.brd" saved to disk.
Command >

$$\frac{\partial}{\partial t}(\rho\phi) + \text{div}(\rho\vec{V}\phi - \Gamma_{\phi}\text{grad}\phi) = S_{\phi}$$

Fast Response Time



- ▶ 20 minutes for:
 - Data transfer
 - Thermal model set up
 - Solution
 - Results processing
 - Report generation
 - Back annotation
- ▶ Four design variants

$$\frac{\partial}{\partial t}(\rho\phi) + \text{div}(\rho\vec{V}\phi - \Gamma_{\phi}\text{grad}\phi) = S_{\phi}$$

CAD integration

Summary & Conclusions

- ▶ Temperature aware design makes SI, thermal and mechanical considerations an integral part of pre-route floor planning
 - Enough thermal detail is considered to “close” the floor plan design
- ▶ Thermal validation can be performed by EE or ME, depending on response time requirements
 - Thermal closure is typically the responsibility of the thermal engineer

Summary & Conclusions

- ▶ Temperature aware design is possible through design tool automation
 - ▶ Bi-directional compatibility
 - ▶ All thermal data stored in Allegro database
 - ▶ Intuitive user interface
 - ▶ High-degree of modeling and results processing automation
- ▶ Temperature aware design is interactive and dynamic as compared to traditional 'over the wall' thermal design
 - ▶ Common data transfer mistakes and oversights are eliminated
 - ▶ All players are working at the same rate and are synchronized
 - ▶ Design space for SI, mechanical and thermal closure is maximized
 - ▶ Overall design time and effort is minimized

Summary and Conclusions

- ▶ Reduce risk of late-cycle redesign by fully considering thermal requirements before routing
- ▶ Reduce communication bottlenecks and errors between electrical and mechanical engineers
- ▶ Increase data reuse by leveraging the EDA database for thermal design
- ▶ Reduce overall design cost and increase quality by opening design space

