Cadence Litho Electrical Analyzer

Electrical DFM Analysis and Optimization

Cadence® Litho Electrical Analyzer is a complete and silicon-correlated electrical DFM analyzer that allows designers to optimize and control the impact of lithography, mask, etch, RET, OPC, and CMP effects on chip parameters. Its contour-based analysis technology provides an accurate, model-based solution for designers to minimize the impact of manufacturing variations on design performance.

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Cadence Litho Electrical Analyzer allows designers using sub-90nm processes to identify and analyze parametric issues associated with manufacturing variability and to minimize their effect on chip performance—all within their existing flows for IP, custom analog, and cell-based digital design.

Cadence Litho Electrical Analyzer uses fab-certified technology to predict contours across the process window and to predict device and interconnect silicon electrical behavior. It gets its silicon-accurate critical dimensions (CD) from Cadence Litho Physical Analyzer, which delivers accurate full-chip contour shape predictions in a matter of hours. Cadence device and interconnect models for accurate prediction of silicon electrical behavior have already been validated in silicon at several semiconductor manufacturers.

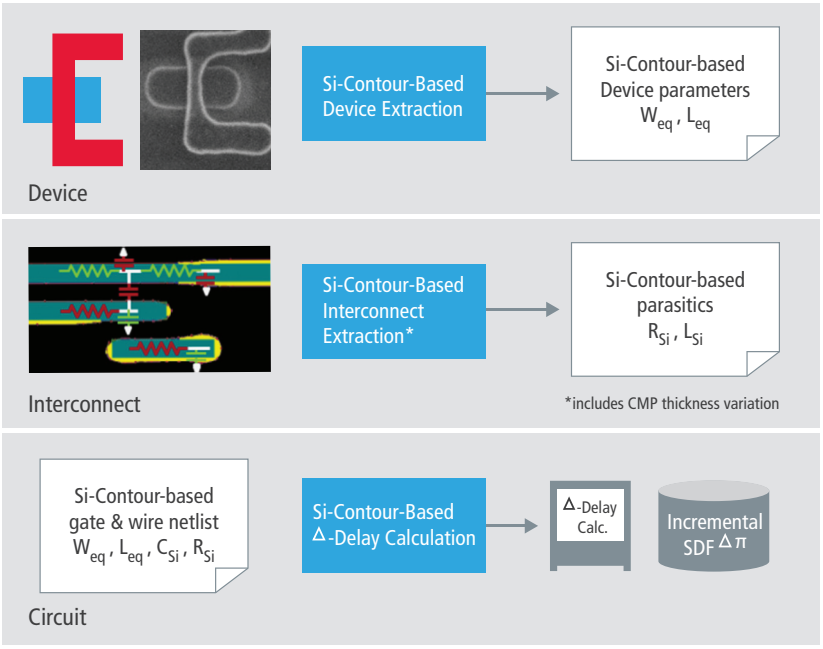

Figure 1: Principles of Cadence Litho Electrical Analyzer

Benefits

- Improves parametric yield and chip performance by accurately determining the impact of systematic variations during design
- Shrinks design margins, achieves higher performance, and accelerates timing closure through silicon-accurate prediction of device and interconnect electrical behavior
- Offers fast and accurate full-chip RC and device extraction based on contour data generated from ideal shapes in GDSII
- Detects and repairs timing and leakage hotspots caused by systematic manufacturing variations using manufacturing-aware delay calculation and full-chip leakage computation based on contours
- Integrates with most library, custom, and chip design flows
- Provides a dedicated environment for library designers to check context sensitivity of standard cells
- Integrates with Cadence QRC Extraction and Cadence Encounter® Timing System

Features

Variability-aware electrical design

In sub-90nm design, systematic variations are the greatest cause of chip failures, causing electrical issues such as timing, signal integrity, and leakage power. At 65nm, systematic variations of 3nm on a transistor gate can cause a 20% variation in delay and double the impact on leakage power.

With traditional corner-based design methodologies, margins are applied everywhere regardless of context. This over-design with excessive guardbanding stalls timing closure and can still result in unexpected parametric failures due to unforeseen systematic manufacturing variations. Over-designing to avoid DFM issues also results in penalties to both area and leakage power.

Cadence Litho Electrical Analyzer offers in-context model-based electrical DFM analysis that incorporates fab-certified

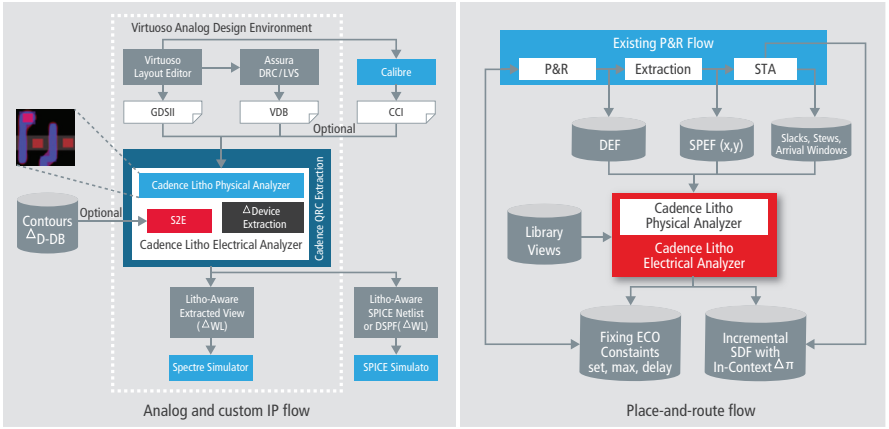

Figure 2: Electrical DFM methodology using Litho Electrical Analyzer for variability analysis

technology information on lithography, RET, OPC, CMP, mask, and etch. Designers can optimize their electrical parameters on-the-fly without any change to their library layout characterization, and they can tighten their design parameters knowing that the impact of variability has been carefully managed.

Fits into any design flow

Litho Electrical Analyzer plugs directly into the designer's existing flows for IP, custom analog, and cell-based digital design. It takes in the designer's timing and place-and-route data, along with encrypted fab technology files, and identifies timing and leakage parametric hotspots for violations due to systematic variations. It then produces timing optimization directives that drive the place-and-route tools.

Litho Electrical Analyzer fits into existing place-and-route and layout design flows, and it provides a closed loop between design and manufacturing. Cell-based chip designers simply input their DEF, SPEF, library information, and fab DFM technology files directly into Litho Electrical Analyzer. It is fast enough to quickly iterate with place-and-route: designers tighten their design margins, run place-and-route, and then use Litho Electrical Analyzer to identify hotspots and produce optimization directives.

For custom design, Litho Electrical Analyzer takes in a SPICE netlist and SPICE models to predict current density across channels, extracting device parameters for transistors from the embedded Cadence Litho Physical Analyzer model-based silicon contour predictions. Silicon-proven device modeling of contour-based (non-rectangular) transistor gates takes into account the short channel effect of a MOSFET inside the device channel to extract the proper device parameters. It then produces a backannotated transistor SPICE netlist. It also applies the changes in RC data to the designer's existing DSPF or SPEF file to represent the true effects of in-context silicon shape variations, without creating new nodes or parasitic elements. Designers can then simulate the backannotated netlist with their SPICE simulator to check the effect of variations on their design and detect potential failures before going to silicon.

Litho Electrical Analyzer integrates with Cadence QRC Extraction in a flow that extracts transistor parameters from contours and writes out a transistor-level netlist in SPICE or DSPF formats or as an extracted view.

For place-and-route designs, Litho Electrical Analyzer also calculates the change in delay and timing skew based on the in-context shape variations, and it provides delay variations back to static timing analysis tools in the form of an incremental SDF. Therefore, designers can verify and minimize the effects of variations on their cell-based design performance in their current design flow.

Litho Electrical Analyzer also provides a dedicated environment for library designers to check and minimize the context sensitivity to variations of standard cells. It includes user-controlled random context generation and

automatically runs Cadence Litho Physical Analyzer and compiles the timing and leakage variations for these contexts in an intuitive GUI, with comprehensive reports and a variability index. Library designers can easily detect which transistors are the most sensitive to variations and optimize their layout, or pass the variability index to chip designer for chip-level optimization. Chip-level implementation tools can leverage the variability index to 1) avoid using sensitive cells in critical paths and therefore reduce variability, and 2) determine cell-specific margins during timing analysis to reduce overall margins and accelerate timing closure.

Specifications

Foundry support

- Certified and supported by leading foundries and IDMs
- Flow-tested and qualified with foundry DFM data kits (DDKs)

Format support

- Design input: GDSII, LEF/DEF, DSPF, SPEF, SPICE, .LIB
- Design output: DSPF, SPICE, SPEF, SDF, SDC

Platforms

- Linux (32-bit, 64-bit)

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

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