TECHNICAL PAPER

CLOSING THE CHIP ARCHITECTURE IMPLEMENTATION FEEDBACK LOOP

Increasing visibility, improving predictability, and minimizing the risks associated with IC designs

cādence®

MAXIMIZE YOUR RESOURCES AND REDUCE YOUR COSTS

Clearly, traditional ASIC, ASSP and SoC design methodologies and flows have barriers between the various steps in the design flow. These can result from siloed functional groups, internal politics, geographic dispersion, lack of consistency in data representation between domains, or myriad other reasons. While steps have been taken to streamline various aspects or parts of these flows, little has been done to address the holistic challenge of actively and dynamically measuring and monitoring the process in real-time—from system-level design and architecture through final signoff prior to silicon fabrication.

However, the economics of today's semiconductor industry demand that the status quo must change, and that all stakeholders in the design process share in the responsibility of producing the highest quality of silicon at the lowest possible cost. As a leading supplier to the semiconductor design chain, and with the broadest and most complete solution portfolio of any EDA vendor in the industry, Cadence is in the best position to address this challenge.

Recently, Cadence unveiled a breakthrough solution to this problem. It provides design and implementation engineers with superior visibility and predictability of chip performance, area, power consumption, cost, and time to market across the full range of design activities, including system-level design and IP selection through final implementation and signoff. This unique and automated approach to semiconductor design has been achieved through the linking of Cadence® InCyte Chip Estimator and the Cadence Encounter® Digital Implementation (EDI) System technologies. The combination of these technologies increases the predictability of key metrics from design specification through final implementation while reducing overall IC project risk.

Using the new Cadence solution, designers are now able to quickly and accurately estimate die size, performance, power and cost of a design. The solution enables real-time IP and manufacturing process what-if analysis to ease IP selection and determine design architecture and feasibility, while leveraging the vast ecosystem of IP suppliers and foundries that contribute data to enable this accurate what-if analysis capability. Once system-level trade-offs and architecture are complete, designers can seamlessly progress to the design and implementation phase, leveraging the initial estimates as a starting point for logic design and physical implementation and drive to fast design convergence.

The Cadence EDI System completes the design, implementation and signoff of the project while monitoring and tracking aspects of block and full-chip progress, while also providing immediate updates to actual die-size, power consumption, performance and cost with full transparency to all stakeholders. As optimizations in the EDI System improve yield, size, performance, or power, users can immediately quantify those benefits in terms of the fully packaged chip cost.

BETTER VISIBILITY, GREATER PREDICTABILITY, AND REDUCED RISK

Decisions made during the architectural planning stages of the semiconductor design cycle largely determine the chip's resulting size, power consumption, performance, and cost. During these early stages, design teams can realize the biggest benefits by considering and quantifying a variety of architectural and IP options prior to final design, implementation and signoff. Traditionally, however, semiconductor designers have been forced to use a manual or disconnected approach, such as condensed spreadsheets or word-of-mouth, to make estimations and architectural choices without the benefit of visibility, flexibility, automation, accurate analysis based on actual physical data, or tight links to implementation tools.

It is generally accepted that 80% of a product's cost is determined in the first 20% of its development cycle. In the same way that the architectural portion of the flow offers the most to gain from making optimized decisions as early as possible, the implementation portion of the flow potentially offers the most to lose. Even small changes made during implementation – such as modifying the memory size and/or architecture, the choice to implement various low power strategies, adding additional input/output (I/O) pins, altering the aspect ratio of the macro to better fit the floorplan, optimizing the design to meet aggressive DFM requirements, or changing the process/library associated with a functional block – can significantly impact cost, performance, power and yield of the chip, and can dramatically impact the overall financial success of the project.

For example, one real-world scenario involved a single functional block (a PCIx host interface) on a large SoC that comprised a substantial number of functional blocks. When the design team discovered that they could not achieve the required performance using the specified library, they made the decision to switch to high-speed cells.

Unfortunately, this information was never relayed to the system architects and these high-speed cells came at a high price – the block consumed more power than had been budgeted for, and this necessitated the use of a significantly more expensive package that could dissipate the thermal load from this additional power. The end result was that the company's cost of producing the device was the same as their main competitor's selling price. The project was eventually cancelled, but only after the company had lost many millions of dollars in tools, engineering resources, and IP purchases.

In order to succeed in today's increasingly competitive marketplace, it is necessary to remove the barriers between the various steps of the design flow and replace them with automation that can increase visibility and facilitate communication throughout the flow as illustrated in Figure 1.

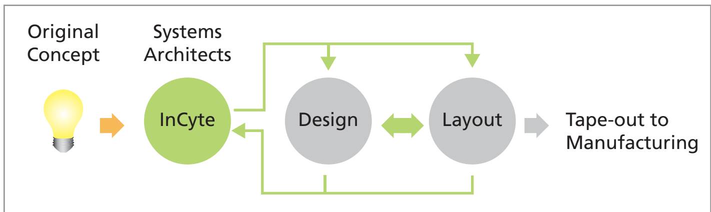

Figure 1. Increasing visibility and facilitating communication throughout the flow.

BREAKING DOWN WALLS AND IMPROVING COMMUNICATION

In order to understand the benefits of closing the loop between architectural feasibility and final implementation, it is necessary to comprehend the evolution of how semiconductor design methodologies developed over time. Figure 2 illustrates a typical design environment that can still be found in use today.

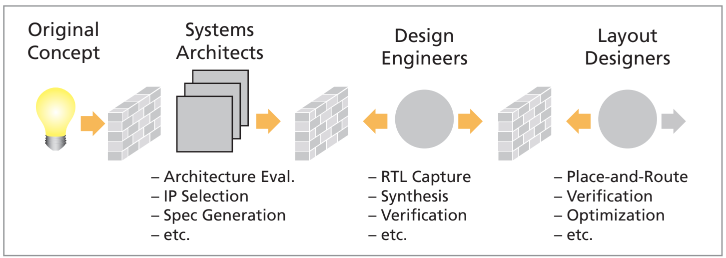

Figure 2. Barriers to communication

Obvious drawbacks to a work flow such as this are the walls between each of the steps in the process. These walls restrict communication explicitly or implicitly between the various domains and limit visibility across the entire flow.

To a large extent, the task of EDA vendors over the years has been to:

- dismantle these walls
- facilitate inter-domain communication
- increase visibility throughout the design flow

The first wall to be overcome was the one between design engineers and layout designers. As the size and sophistication of designs increased – coupled with the complexities inherent with ever-decreasing geometries – it became necessary for the design and layout of a chip to be brought closer together as illustrated in Figure 3.

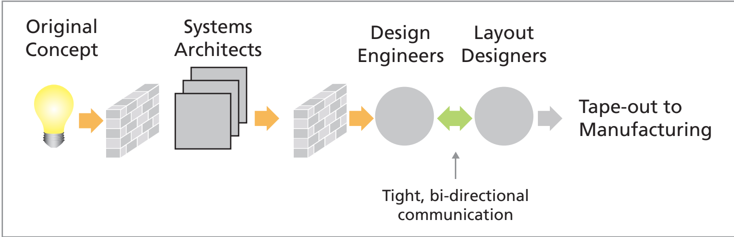

Figure 3. Breaking down the wall between design and layout.

There were several other contributing factors that drove this change, including the fact that the layout team now fell under the purview of the system house, and that the design, implementation, and verification tools were enhanced to support tight, bi-directional communication between these domains.

At the other end of the flow, the system architects are chartered with taking an original concept and performing an intricate balancing act to satisfy the competing requirements of cost, function, power, and performance, while achieving acceptable design yields. This is a daunting task because – in addition to the overall architecture of the design – there are literally tens of thousands of choices that can be considered when it comes to manufacturing processes, third-party IP selection, and the various combinations of these factors.

Until recently, the only tools available to system architects were whiteboards and complex and nested spreadsheets. This meant that there was no robust (fast, efficient, and accurate) or automated way for system architects to comprehend the full impact of various trade-offs and decisions affecting die area, power consumption, performance, functionality, package requirements, and yield.

As illustrated in Figure 4, the wall between the original concept and the system architects was eventually brought down by the unique estimation technology provided by InCyte Chip Estimator.

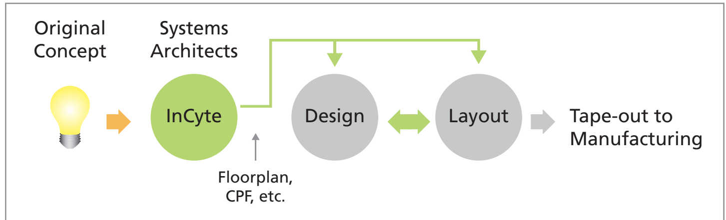

Figure 4. InCyte removes the walls between the concept and the system architects and between architecture and implementation.

The InCyte Chip Estimator allows system architects to quickly and easily evaluate alternative architectural and implementation scenarios and to assess the impact of using various IP blocks, technology nodes, foundry requirements, and power strategies. Even assessing the impacts of using different low-power techniques with regard to IP selection, cost, and overall power consumption can now be considered early on in the process. Once the tradeoffs are considered by the system architects, and decisions are made as to an optimal low power strategy for the design, the InCyte Chip Estimator can automatically generate a Common Power Format (CPF) file, which can be used for all downstream design, implementation, verification, and technology-related power steps in the flow.

CLOSE THE LOOP, MINIMIZE COST, AND MAXIMIZE PRODUCTIVITY

Although the InCyte Chip Estimator provided tremendous productivity and cost-saving advantages, there remained a final challenge in that there was still no easy way for any decisions made by, and actions performed by the design engineers and layout designers to be fed back to the system architects in a programmatic or automatic way, as illustrated in Figure 5.

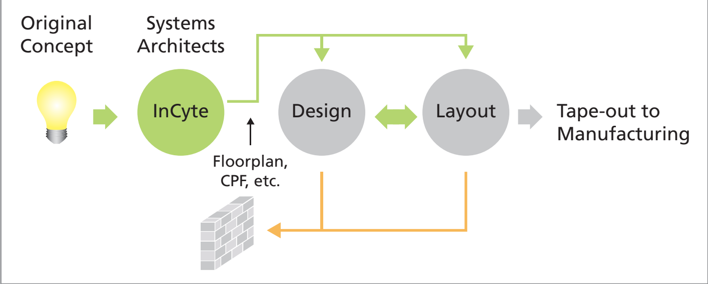

Figure 5. One final wall remained...

An example of where not having this strong linkage between system architecture and implementation can cause issues is in the case significant late-stage design changes. As this is a last-minute request near the end of a project, the implementation team is forced to perform an urgent change to the design without the benefit of complete context of the overall design objectives set by the system architects. This lack of consideration can be the root cause of a failed project.

The solution requires enabling design engineers and layout designers to evaluate their local decisions in the context of global objectives for cost, size, power, performance, yield, and so forth. Furthermore, the design engineers and layout designers need the ability to communicate their actions and suggestions back up the line to the system architects for their consideration in a global context as illustrated in Figure 6.

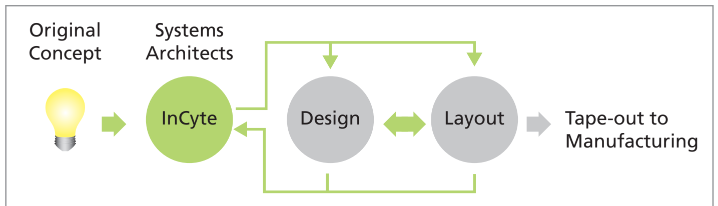

Figure 6. Closing the loop between architecture and implementation.

Cadence now makes this possible through the bringing together of the InCyte Chip Estimator and Encounter Digital Implementation (EDI) System. The combined solution also eliminates guesswork by providing a unique data-driven and holistic approach to the optimization of IP selection and integration through architecture, design, implementation and signoff. This automated approach to

semiconductor design increases visibility at the earliest conceptual stages of the project and throughout the flow, thereby improving the predictability of key metrics from initial design specification through final implementation while reducing overall project risk.

SUMMARY

Early ASIC, ASSP, and SoC design environments had walls between each step in the process. These walls restricted communication between the various domains and limited visibility from one domain to another.

Over the years, these walls have been broken down. The first to go was the wall between the design engineers and the layout designers. The next step was to provide system architects with the tools they needed to quickly and easily evaluate alternative architectural and implementation scenarios, to assess the impact of using various IP blocks and technology nodes, and so forth.

Now, the integration between the Cadence InCyte Chip Estimator and the Cadence Encounter Digital Implementation (EDI) System enables system architects to automatically convey their intent to the implementation portion of the flow.

Furthermore, the design engineers and layout designers gain the ability to close the loop and feed data back into the system architects' domain. This means that the system architects can use real, physical values to evaluate the results of any implementation decisions in the context of their global design goals.

The result is a breakthrough solution that provides design and implementation engineers with complete visibility and predictability of chip cost, performance, area, power consumption, and time-to-market -- all the way from architectural/system-level design and IP selection through final implementation and signoff.

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Cadence Design Systems, Inc.

CORPORATE HEADQUARTERS
2655 Seely Avenue
San Jose, CA 95134
P: +1.800.746.6223 *(within US)*
+1.408.943.1234 *(outside US)*
F: +1.408.943.5001
www.cadence.com

For more information contact Cadence sales at:

+1.408.943.1234

or log on to:

www.cadence.com/contact_us

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